

A Unified Approach in the Analysis of Prescalers and Dual Modulus Prescalers for low-power systems

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Abstract

The paper represents a study of several Prescalers and Dual Modulus Prescalers their power consumption and architecture. Various Prescalers and dual modulus are designed using low power hybrid master slave flip-flop using 180nm technology. As a result, the average power consumption of the all the prescalers, dual modulus prescaler is estimated and a comparison between prescaler and dual modulus prescaler is done. The Clock frequency for prescalers are 20 GHz, 5GHz for 4/5 dual modulus prescalers and other prescaler respectively. This paper discusses the design of divide by 2, divide by 3, divide by 4, divide by 5, divide by 6, divide by 7, divide by 10, divide by 11 prescaler and divide by 4/5, divide by 5/6, divide by 6/7 and divide by 10/11 Dual modulus prescaler.

Keywords: Dual Modulus Prescaler, Frequency divider, Frequency Synthesizer, Hybrid Master Slave Flip-flop, Prescalers.

INTRODUCTION

The high-speed frequency divider is a crucial block in frequency synthesizer for generating any range of frequencies from a oscillator used in wireless communications. Dual modulus prescalers are widely utilized in phase-locked frequency synthesizers to obtain programmable frequency division ratio. A PLL have been typically employed in communication IC's and data interfaces for clock generation. Most PLLs include dividers in order to obtain higher frequencies by means of multiplying the reference frequency. A dual modulus is commonly used in a multi-rate PLL and a fractional-N PLL for frequency synthesis. A dual-modulus prescaler generally comprises of a divide-by-N/N+1 unit and a number of asynchronous divide-by-2 units. The high-speed multi-GHz prescaler usually

devours the largest share of power in the frequency synthesizer because the prescaler is usually executed with digital circuits with large power consumption at GHz range. Flip-flops and clock distribution network mostly account for 30–70% of the total chip power consumption [1, 2]. Flip flops and latches are considered as indispensable components for design of synchronous digital VLSI systems. The highest operating frequency of clocked digital systems is determined by the flip-flops. The correct selection of flip-flop is very much necessary which is done on the basis of factors like high performance, low power, transistor count, clock load, design robustness, power-delay, and power-area tradeoffs are generally well-thought-out before choosing a particular flip-flop design. Master-slave FFs are generally utilized for low power systems whereas other FF like pulse triggered FFs find their use in high speed applications.

HYBRID MASTER SLAVE FLIP-FLOP

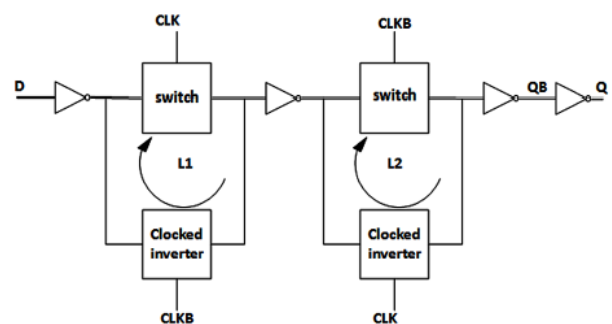


Figure 1. Conventional master-slave FF architecture

In the conventional master slave FF architecture as shown in figure 1, complementary outputs Q and QB are obtained by using two regenerative loops, L1, L2, one each in the master and the slave sections to maintain a static functionality. However, both the loops operate independently and become

functional on complementary clock signals CLK and CLKB respectively. Regenerative loops generally require two cross coupled inverters.

In the traditional design technique, for each loop, one inversion takes place in the forward (critical) path while the other (clocked) inversion takes place in the feedback path and there is no shared component between both the loops.

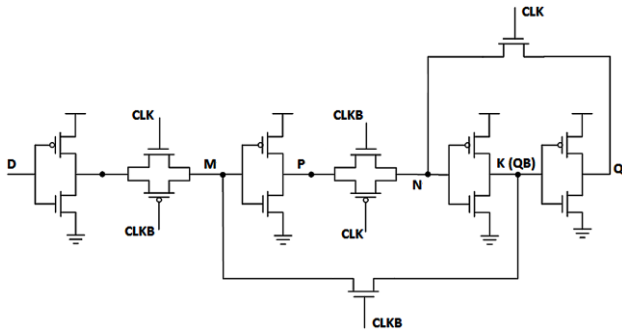


Figure 2. Hybrid Master Slave Flip-flop

In Hybrid Master Slave Flip-flop (HMSFF) pass transistors are used which reduces the power dissipation. Average power consumed is 0.02mW using 180nm.

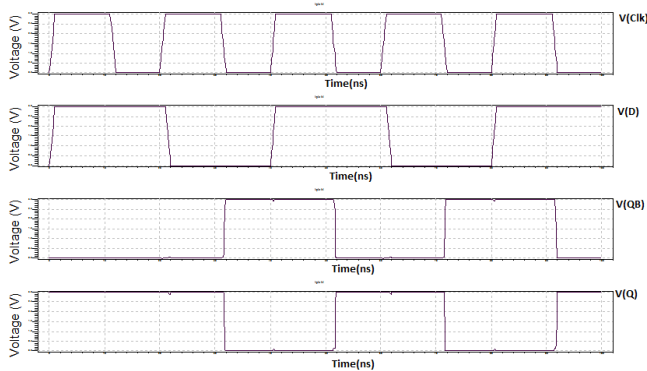


Figure 3. Stimulations result of HMSFF

PRESCALER DESIGNS

Architecture of proposed prescalers along with the gates used for divide-by-2, divide-by-3, divide-by-4, divide-by-5, divide-by-6, divide-by-7, divide-by-10, divide-by-11 prescalers are shown in Figure4(a-o) respectively, along with their simulated waveform where hybrid master slave Flip-flop is used to attain required division results.

The proposed divide-by-N prescaler circuits are presented in the figure ranges from 2 to 7. According to the division ration N, the numbers of the flip-flops and the NOR-gate inputs are determined as K_N and R_N , respectively. The outputs of the R_N consecutive flip-flops from the rightmost flip-flop, Q [$R_N-1:0$], are connected to the inputs of the NOR gate. Let’s explain the divide-by-7 prescaler as an example. It consists of four flip-flops and a two input NOR gate. In every clock cycle, Q[3:1] are shifted to be Q[2:0] while Q[3] is determined by $Q[1 + Q[0]]$. The divider has a circuit style

similar to a linear feedback shift register(LFSR). However, while the typical LFSR uses XOR gates and generated a pseudo-random binary sequence, the divider uses the NOR gate and generates consecutive ‘0’s and consecutive ‘1’s, which may be thought of a clock signal with a long period. In the proposed circuits, the division operation is performed without a reset signal or an initialization circuit. For example Let the divide by 7 prescaler start with any initial state out of the all stages ranging from ‘0000’ to ‘1111’. Although the shift register may go through some transient states, it finally goes into the correct loop, which consists of ‘0000’, ‘1000’, ‘1100’, ‘1110’, ‘0111’, ‘0011’, and ‘0001’. Not only the divide by 7 prescaler but also any divide by N prescaler has its own correct loop, in which the stat of all ‘0’s is always included. Once the output of the flip-flops are all ‘0’s, the leftmost flip-flop will have ‘1’ as the output in the next cycle. Until this ‘1’ is shifted and reaches to the flip-flop whose output is connected to the NOR-gate the leftmost flip-flop will have ‘1’ continuously. If at least one of the NOR-gate inputs is ‘1’, the leftmost flip-fop will have ‘0’ until the outputs of the flip-flop are all ‘0’s. Therefore, a rule can be derived for the number of the flip-flops (K_N) and the number of the NOR-gate inputs (R_N) when the division ratio (N) is larger than one. Here, an inverter is thought of one input NOR gate in the case of divide by 2-4 circuits. As inferred from the above explanation and tabulated in table 1, the number of ‘0’s in the output sequence is the same as K_N and the number of ‘1’s is the same as $K_N - R_N + 1$. Because the sum of the numbers of ‘0’s and ‘1’s is equal to N,

$$2K_N - R_N + 1 = N \tag{1}$$

As shown in the table whenever N increases by three, K_N increases by two and R_N increased by one. Therefore, the relations hip between K_N and N can be derived inductively as shown in below equation

$$K_N = \lfloor \frac{2}{3} N \rfloor \tag{2}$$

$$R_N = 2 \lfloor \frac{2}{3} N \rfloor - N + 1 \tag{3}$$

A division ratio of any natural number greater than one can be supported without cascading dividers whether the division ratio is a prime umber or a composite number[3,4].

Table I. The no. of flip-flops (K_N) and NOR Gate Input (R_N) According to N Division

Division Ratio, N	Output Sequence	# of '0's	# of '1's	K_N	R_N	$K_N - R_N + 1$	Division Ratio, N	Output Sequence	# of '0's	# of '1's	K_N	R_N	$K_N - R_N + 1$
2	0_1	1	1	1	1	1	9	000000_111	6	3	6	4	3
3	00_1	2	1	2	2	1	10	000000_1111	6	4	6	3	4
4	00_11	2	2	2	1	2	11	0000000_1111	7	4	7	4	4
5	000_11	3	2	3	2	2	12	00000000_1111	8	4	8	5	4
6	0000_11	4	2	4	3	2	13	000000000_11111	8	5	8	4	5
7	0000_111	4	3	4	2	3	14	000000000_111111	9	5	9	5	5
8	00000_111	5	3	5	3	3	15	0000000000_111111	10	5	10	6	5

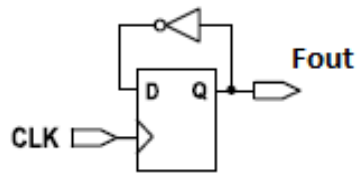


Figure 4. (a) : Divide-by 2 Prescaler

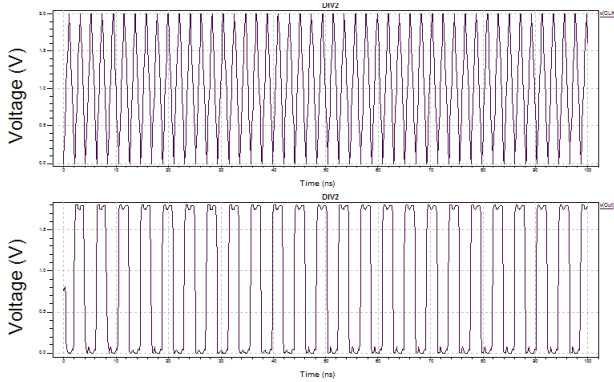


Figure 4. (b) : Divide-by 2 Output Waveform

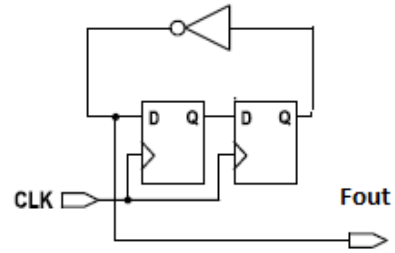


Figure 4. (e) : Divide-by 4 Prescaler

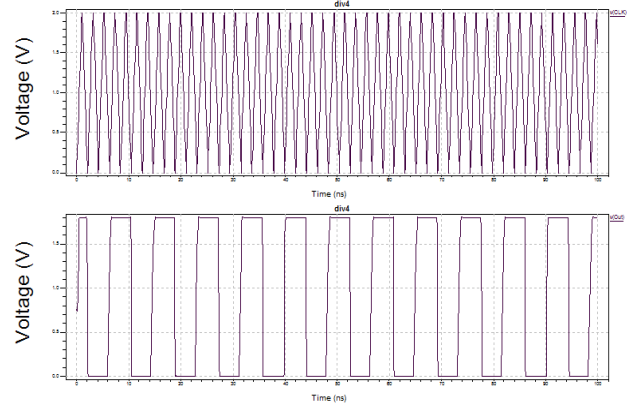


Figure 4. (f) : Divide-by 4 Output Waveform

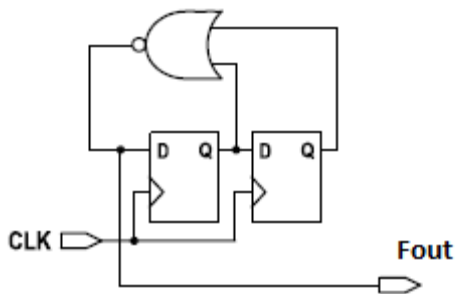


Figure 4. (c) : Divide-by 3 Prescaler

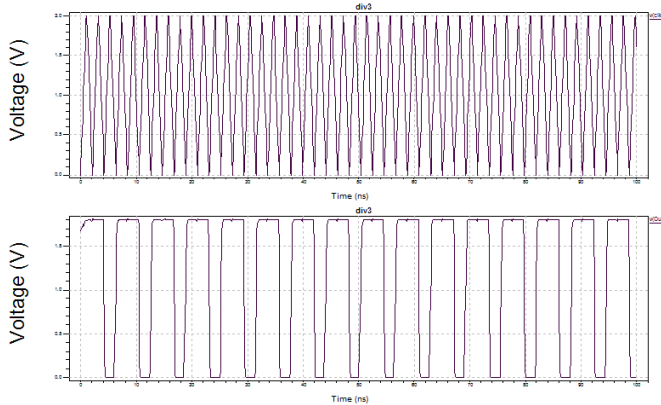


Figure 4. (d) : Divide-by 3 Output Waveform

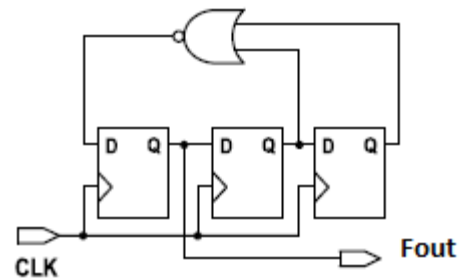


Figure 4. (g) : Divide-by 5 Prescaler

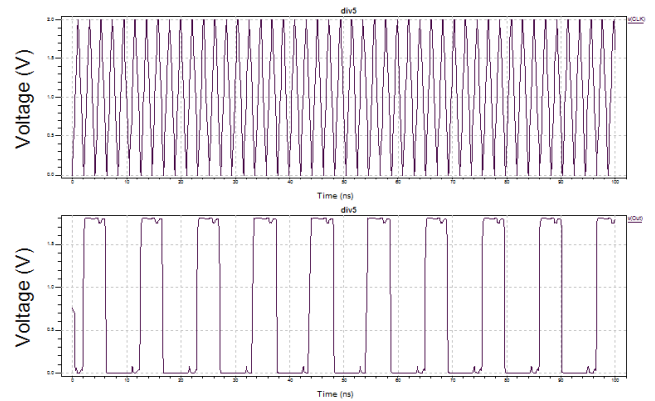


Figure 4. (h) : Divide-by 5 Output Waveform

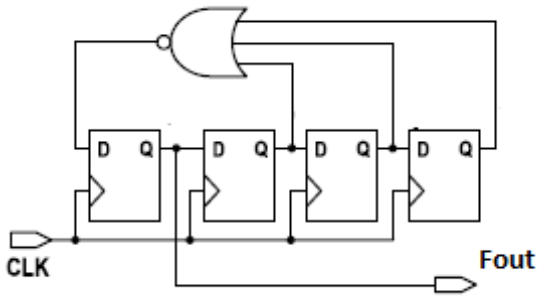


Figure 4. (i) : Divide-by 6 Prescaler

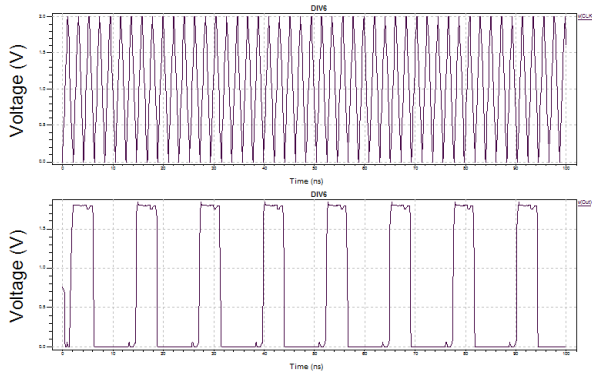


Figure 4. (j) : Divide-by 6 Output Waveform

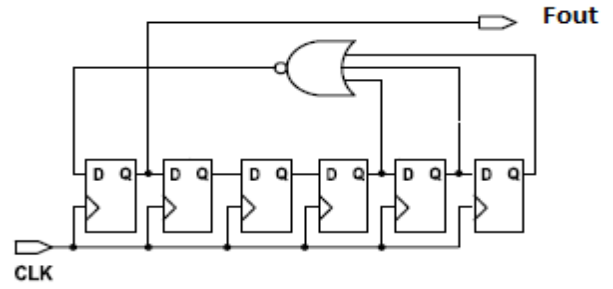


Figure 4. (l) : Divide-by 10 Prescaler

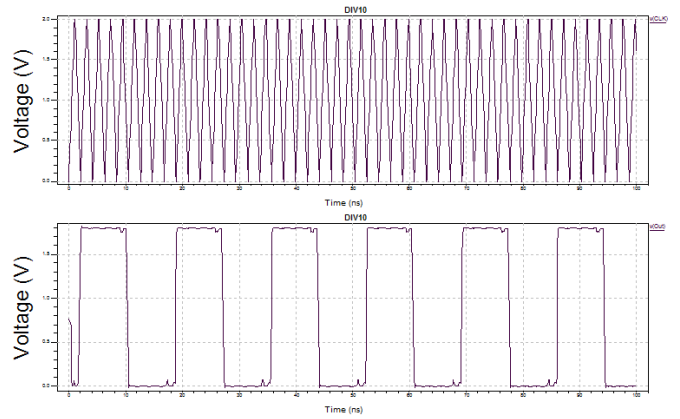


Figure 4. (m) : Divide-by 10 Output Waveform

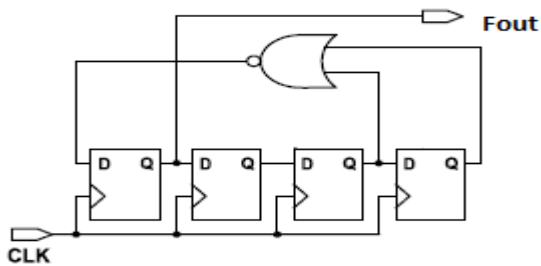


Figure 4. (j) : Divide-by 7 Prescaler

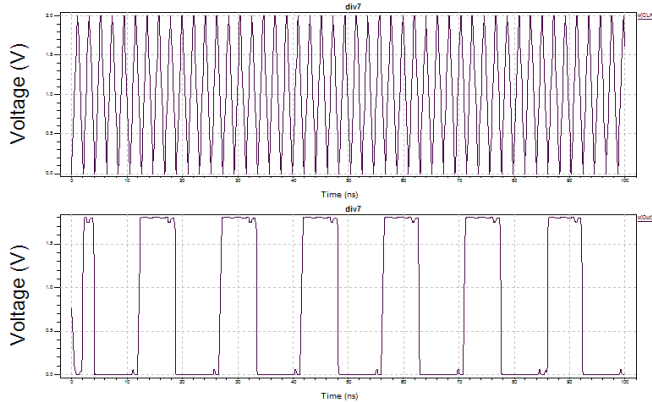


Figure 4. (k) : Divide-by 7 Output Waveform

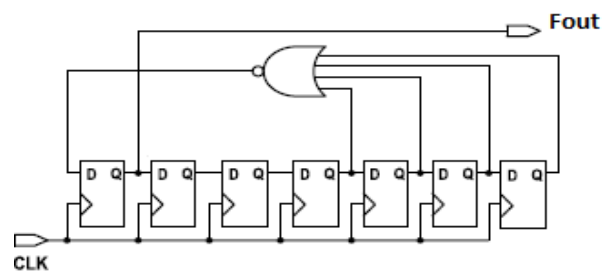


Figure 4. (n) : Divide-by 11 Prescaler

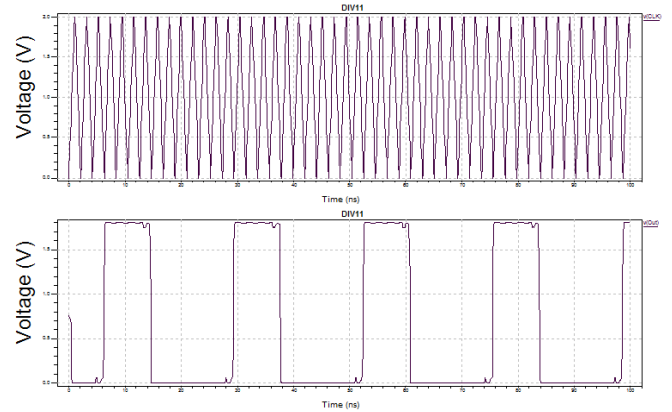


Figure 4. (o) : Divide-by 11 Output Waveform

DUAL MODULUS PRESCALERS

Architecture of proposed dual modulus prescalers where MC stands for mode control of divide-by-5/6, divide-by-6/7, divide-by-10/11, divide-by-4/5 are shown in Figure 5(a-l) respectively, along with their simulated waveform where hybrid master slave Flip-flop is used to attain required division results. A division ratio of any natural number greater than one can be supported without cascading dividers whether the division ratio is a prime number or a composite number.

A divide by $N/N+1$ prescaler can be designed by combining a divide by N prescaler and divide by $n+1$ prescaler. One input of the AND gate is MC, which controls the division ratio. When MC is '0', the division ratio is N . when MC is '1', the division ratio is $N+1$. In the divide by $N/N+1$ prescaler, a rule can be derived for the number of flip-flops ($K_{N/N+1}$), the number of the NOR gate inputs ($R_{N/N+1}$), and the position of the AND gate. First, $K_{N/N+1}$ is determined as the greater or of K_N and K_{N+1} , which are the numbers of the flip-flops in the divide by N and divide by $N+1$ prescaler circuits, respectively. Thus, because $K_N \leq K_{N+1}$,

$$K_{N/N+1} = \max(K_N, K_{N+1}) = K_{N+1} \quad (4)$$

Second, $R_{N/N+1}$ is determined as the greater one of R_N and R_{N+1} , which are the numbers of the NOR-gate inputs in the divide by N and divide by $N+1$ prescaler circuits, respectively thus

$$R_{N/N+1} = \max(R_N, R_{N+1}) \quad (5)$$

Third, the position of the AND gate is determined by whether or not N is a multiple of three. When N is a multiple of three, the AND gate is located at the output of the R_N 'th flip-flop, $Q[R_N-1]$ and \overline{MC} is used. Otherwise, when N is not a multiple of three, the AND gate is located at the output of the rightmost flip-flop, $Q.[5]$

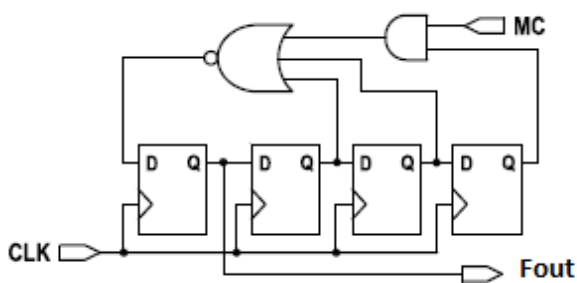


Figure 5. (a) : Divide-by 5/6 Dual Modulus Prescaler

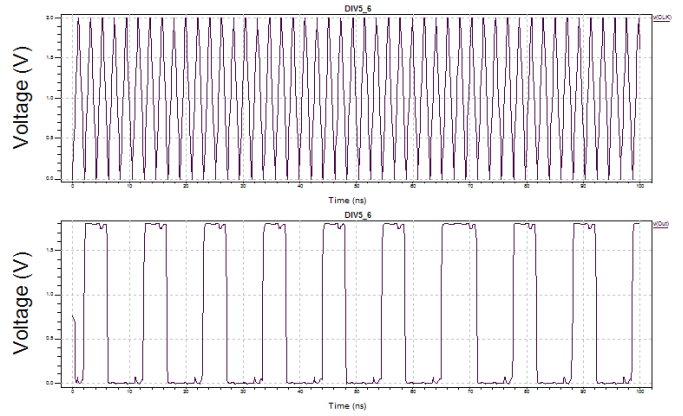


Figure 5. (b) : Divide-by 5/6 DMP Output Waveform when MC=0

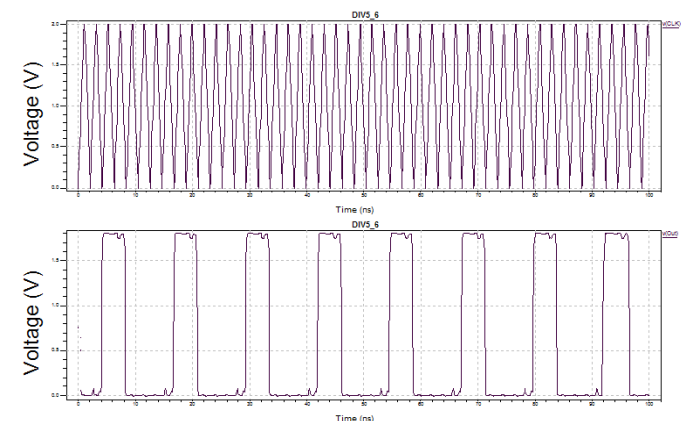


Figure 5. (c) : Divide-by 5/6 DMP Output Waveform MC = 1

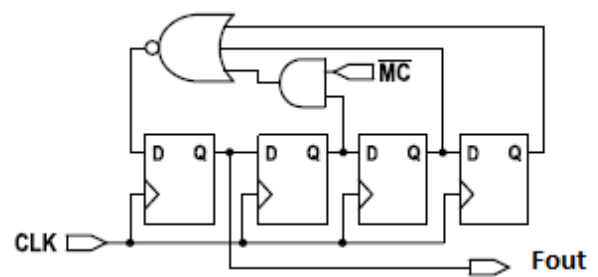


Figure 5. (d) : Divide-by 6/7 Dual Modulus Prescaler

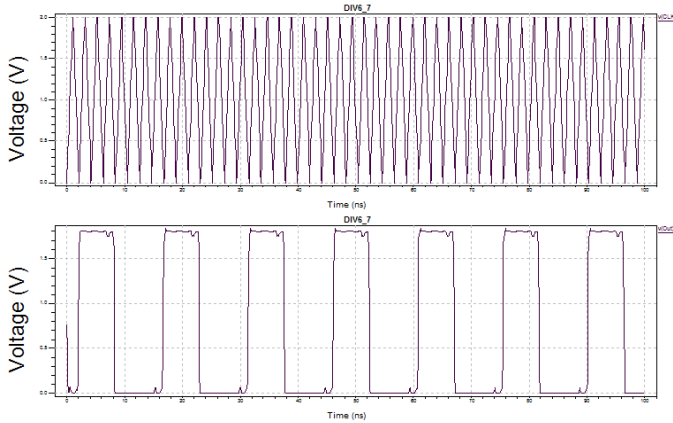


Figure 5. (e) : Divide-by 6/7 DMP Output Waveform When MC=0

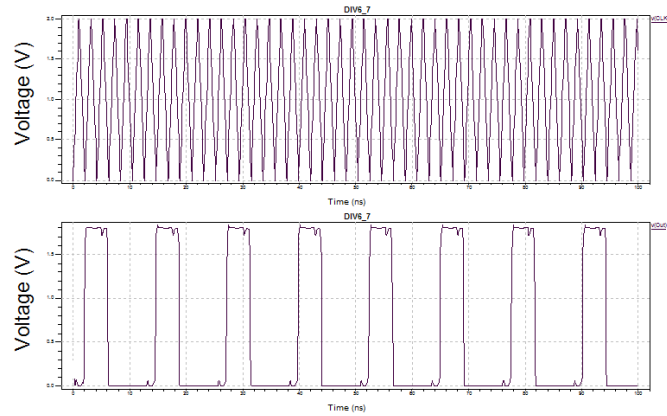


Figure 5. (f) : Divide-by 6/7 DMP Output Waveform MC=1

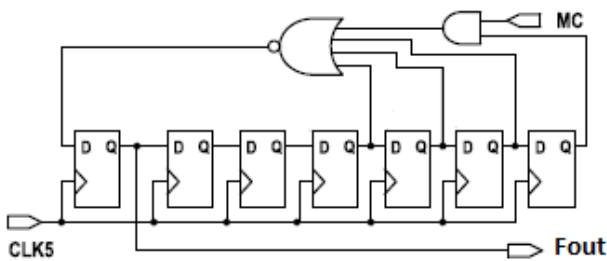


Figure 5. (g) : Divide-by 10/11 Dual Modulus Prescaler

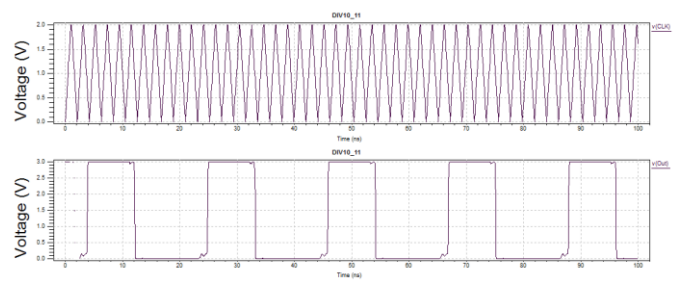


Figure 5. (h) : Divide-by 10/11 DMP Output Waveform When MC = 0

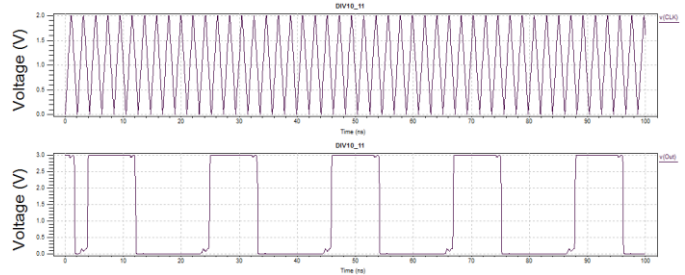


Figure 5. (i) : Divide-by 10/11 DMP Output Waveform When MC = 1

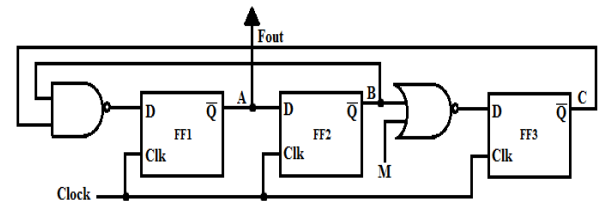


Figure 5. (j) : Divide-by 4/5 Dual Modulus Prescaler[6]

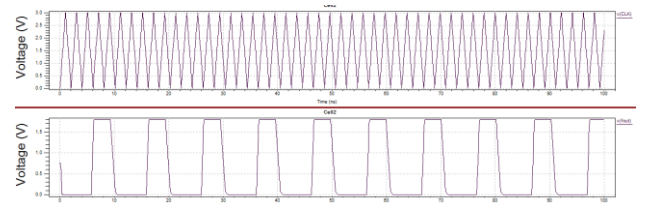


Figure 5. (k): Output Waveform of Dual modulus prescaler for mod 5.

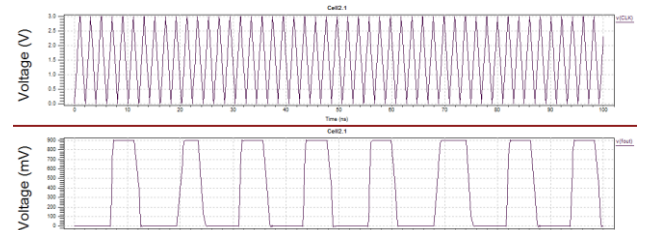


Figure 5. (l): Output Waveform of Dual modulus prescaler for mod 4.

SIMULATION RESULTS

The proposed circuit of dual modulus prescalers and prescalers is implemented with other substitute prescalers to better evaluate the gains of hybrid master slave flip-flop. Keeping $W_p = 2W_n$.

Table II. Performance of Different Prescalers

PRESCALER/DUAL MODULUS PRESCALER	TRANSISTOR COUNT	AVERAGE POWER (mW)
Divide by 4	30	0.12
Divide by 5	46	0.17
Divide by 6	62	0.21
Divide by 7	60	0.19
Divide by 10	90	0.29
Divide by 11	106	0.33
Divide by 4/5	50	0.02
Divide by 5/6	68	0.23
Divide by 6/7	68	0.3
Divide by 10/11	112	2

Table II illustrates the simulation performances of different prescalers using 180nm process. All the prescalers and dual modulus prescalers are simulated at 1.8V at 5 GHz and 4/5 dual modulus was simulated at 0.9V at 20GHz respectively. It is clearly visible from results that instead of using single prescaler, dual modulus prescaler can be used as power consumed is almost relatable. Average power consumed by divide by 2 and divide by 3 is 0.09mW and 0.1mW respectively.

CONCLUSION

In this work, the proposal of a high speed, low power consumption CMOS divide by N prescalers and dual modulus prescalers is presented. The design and optimization of a hybrid master slave flip-flop based prescaler has been carried out by the analysis of the operating frequency and power consumption. An innovative divide by 4/5 unit with minimal power consumption has been offered [7].

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