International Journal of Applied Engineering Research ISSN 0973-4562 Volume 12, Number 11 (2017) pp. 2662-2669
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Noise Modeling and Simulation of DCDMG AlGaN/GaN MODFET

Rahis Kumar Yadav[1], Pankaj Pathak[2], R M Mehra[3]
[1,2,3]Department of Electronics and Communication Engineering, School of Engineering and Technology, Sharda University, Knowledge Park- III, Greater Noida, Uttar Pradesh, 201306, India.

[1]ORCID:0000-0003-3677-7949, [2]ORCID:0000-0003-2642-1500, [3]ORCID:0000-0003-4780-0593

Abstract
This article presents analytical noise equivalent circuit model for analysis and characterization of novel field plated dual channel dual material gate (DCDMG) AlGaN/GaN MODFET first time. Accurate modeling of high-frequency noise for enhanced device structure is indispensable for design and development of low noise amplifiers (LNAs). In this article noise parameters extraction is based on well known PRC and Pospieszalski noise model considering six noise sources in extrinsic and intrinsic parts of device. The device is treated as a black box of noisy two port network for investigation and analysis. The extrinsic and intrinsic elements of noise equivalent circuit model are extracted from two port S-parameters under appropriate cold FET pinch-off biasing using direct extraction methodology. Extracted and simulated noise parameters include minimum noise figure, normalized noise temperature, magnitude as well as phase of source reflection coefficient for the proposed device structure. Device TCAD simulation and previously reported experimental results are also compared with model results to validate accuracy of extracted noise parameters. The proposed device structure has novelty for providing better electric field uniformity, improved suppression of short channel effects, reduction in current collapse, improvements in carrier transport efficiency and enhancement in drain current capability over conventional MODFETs. Thus the proposed device noise model can be very useful for circuit simulations and design of superior performance LNAs.

Keywords: DCDMG-HEMT noise model, noise performance analysis, noise parameter extraction, minimum noise-figure, noise resistance.

INTRODUCTION

Presently a lot of attention is being concentrated on GaN based MODFETs due to their outstanding material properties. Due to presence of wide band gap in compound semiconductor material the GaN MODFETs can withstand high temperature at high power microwave applications [1-7]. Also GaN MODFETs are preferred over GaAs HEMTs due to their higher speed of operation, better current densities and overall improved efficiency. Many research efforts are focused on improved high power and low noise amplifier (LNAs) designs and fabrication as a monolithic circuit thus eliminating the need of receiver protection circuitry [8-14]. Many scientists are working to minimize noise in GaN devices at low as well as high frequency range of operation. In order to bridge gaps between theory and experimental practices many of scientists are continuously working for improvement of small signal equivalent circuit noise models that can be used for computer based simulations tools in semiconductor industries [15-21]. Also compact models can support in design of reliable LNAs and oscillator circuits for microwave range of frequencies [22].

It is well known fact that the device access resistance and intrinsic elements are main cause for limiting the noise performance of device operating in microwave and millimeter range of frequency. Contribution in noise figure by various intrinsic and extrinsic elements of device must be analyzed for obtaing accurate circuit models. For the proposed article modeling methodology primarily differ in choice of circuit topology for novel DCDMG AlGaN/GaN MODFET. Previous research proved that double channel MODFETs can provide increased saturation current, extra output power, reduced differential source access resistance, higher linearity and cutoff frequency [23-24]. For of small signal parameters of proposed device a well known direct parameter extraction approach is applied in order to ensure better accuracy and good consistency with physical device structure as suggested by Minasian [25] that was later modified by Dambrine et al. [26] and Berroth and Bosch [27].

For the full noise characterization of a GaN HEMTs, the determination of minimum noise figure (F_{min}), normalized noise resistance (r_n), optimum source conductance (G_{opt}), and optimum source susceptance (B_{opt}) is necessary. The 'PRC' model by Van der Ziel [28], Pucel [29] , and A. Cappy [30] has emerged as the most accurate and convenient ways to obtain the noise model parameters for GaN HEMTs.

Apart from these pioneering research works, Pospieszalski [31-32] proposed an alternative high-frequency noise model with the aim of dissociating gate noise from the drain noise. PRC and Pospieszalski model are used as basis for noise analysis of novel field plated DCDMG AlGaN/GaN MODFET in this article. These models are well known for thier extraction accuracy and reliability.

MODEL DESCRIPTIONS

Device Structure

The novel device stuctrue proposed for small signal noise modeling is an on-wafer DCDMG $Al_{0.3}Ga_{0.7}N$/GaN MODFET as shown in Figure 1. Our proposed device structure is conceptually an outcome of recent research on GaN MODFETs [23-24] and [33-34]. The epitaxial layers of MODFET were grown by MOCVD on a 2.5-inch sapphire substrate. Drain and source terminal ohmic contacts were formed by Ti/Al/Ni/Au metal stacks, followed by the rapid thermal annealing at 880 ºC for 48 seconds in nitrogen environment. The gate regions made up of dual metals and e-

beam defined with a total gate length of 1µm. For asymmetric structure gate-drain and gate-source spacing defined as 1.5 µm and 1µm respectively. Ni/Au metallization process is applied for making Schottky contacts with dual metal gate and 3nm AlGaN cap layer. PECVD procedure was used for depositing passivation layer of Si_3N_4 film. Formation of via-holes using plasma dry etching was carried out in order to reduce source inductance. Field plate is formed above gate passivation layer to increase E-field uniformity that can suppress current collapse in device [34].

For fabrication of 1x100µm^2 gate area feature size component, a standard gold plated air bridge process was used. The dual metals (M_1 and M_2) together constituted single gate of device. An interface is formed between $Al_{0.3}Ga_{0.7}N$ cap layer and 18nm n-$Al_{0.3}Ga_{0.7}N$ barrier layer followed by 3nm UID $Al_{0.3}Ga_{0.7}N$ spacer layer. Again spacer layer forms interface between 14nm thick UID GaN upper channel layer followed by 21nm n-$Al_{0.3}Ga_{0.7}N$ second barrier layer in which Al mole fraction (m) graded from 3% at the lower to 6% at the upper interfaces for enhancing lower channel functionality. Second barrier layer makes interface between 2.5µm UID GaN layer followed by 3nm AlN nucleation layer to act as back barrier. Sapphire was used as substrate that can withstand higher operating temperature thus making device useful as a high power microwave device.

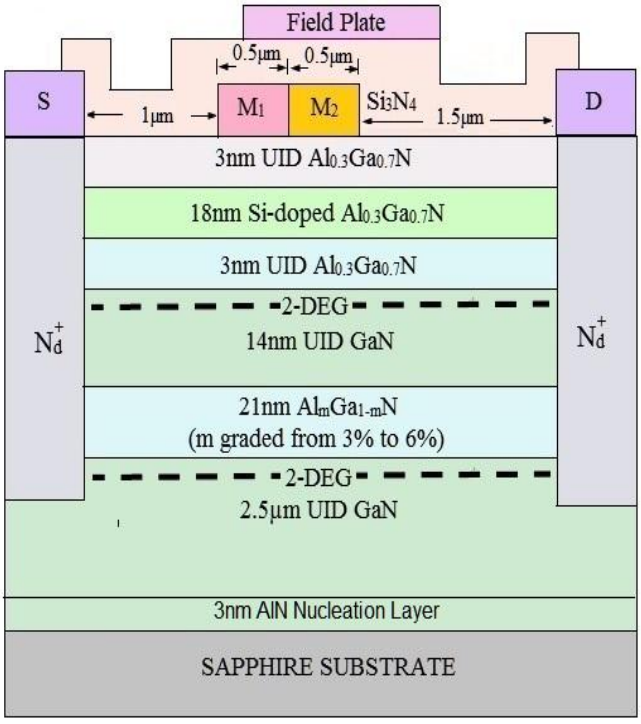

Figure 1: Cross sectional schematic view of asymmetric dual channel dual material gate AlGaN/GaN MODFET epitaxial layers on sapphire substrate, M_1 (Au) with work-function (ϕ_{M1}) =5.1eV, M_2 (Ni) with work-function (ϕ_{M2}) =4.6 eV, gate length=1µm, gate width (W)=100µm.

Small signal noise equivalent circuit model

For the high-frequency characterization of microwave transistors small-signal models are often used to parameterize complicated behaviors with relatively simple equations. A small-signal model is preferably designed so that the model parameters represent something physical in the transistor. This can provide important information to optimize the test structures layout, to perform the simulation of the complete structure using an equivalent circuit, and to study the sensitivity of the device under test (DUT).

Fig.2 shows small signal noise equivalent circuit model for proposed device structure. This circuit has elements representing intrinsic and extrinsic parts of device. R_g, R_s, and R_d, represent parasitic resistances of gate, source and drain respectively. L_s, L_d, and L_g, represent source, drain and gate electrode inductances respectively. C_{pg}, C_{pd}, and C_{pgd}, represent contact pad capacitances between gate-source, drain-source and gate-drain respectively. R_{gs} and R_{gd} are intrinsic input and output channel resistances respectively. C_{gs}, C_{ds}, and C_{gd}, represent intrinsic capacitances between gate-source, drain-source and gate-drain respectively. The symbols g_m, and g_{ds}, represent transconductance and drain conductance of device. The current generator in the output circuit has magnitude of $g_m V_{gs}$ and phase shift of $e^{-j\omega\tau}$ in which V_{gs}, ω and τ represent gate-source voltage, angular frequency and transit time respectively. Five noise sources are represented by $\overline{e_g^2}$, $\overline{e_s^2}$, $\overline{e_d^2}$, $\overline{i_{gs}^2}$ and $\overline{i_{ds}^2}$. In these parameters $\overline{e_g^2}$, $\overline{e_s^2}$ and $\overline{e_d^2}$ represent gate, source and drain noise voltages respectively whereas $\overline{i_{gs}^2}$ and $\overline{i_{ds}^2}$ represent intrinsic channel charging and intrinsic drain noise currents respectively.

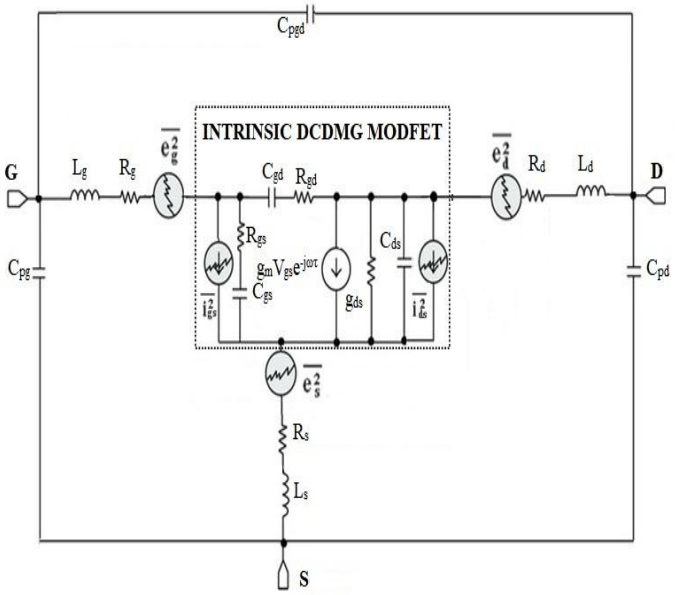

Figure 2: Small signal noise equivalent circuit model

Analytical expressions for extraction of signal parameters

It is established in previous research on GaN HEMT [29] that the intrinsic elements are dependent on biasing and the extrinsic elements are independent of dc biasing. Therefore, Y-parameter matrix of complete device model can be written as:

$$Y = Y_{pad} + \left[Z_{RL} + Y_{\text{int}}^{-1} \right]^{-1} \quad (1)$$

Y_{PAD} represents PAD capacitances of device:

$$Y_{pad} = \begin{bmatrix} j\omega(C_{pg}+C_{pgd}) & -j\omega C_{pgd} \\ -j\omega C_{pgd} & j\omega(C_{pd}+C_{pgd}) \end{bmatrix} \quad (2)$$

Z_{RL} represents extrinsic inductance and resistance part of circuit model:

$$Z_{RL} = \begin{bmatrix} R_g+R_s+j\omega(L_g+L_s) & R_s+j\omega L_s \\ R_s+j\omega L_s & R_d+R_s+j\omega(L_d+L_s) \end{bmatrix} \quad (3)$$

After de-embedding parasitic elements, intrinsic part of circuit can be characterized by Y_{int} matrix:

$$Y_{int} = \begin{bmatrix} j\omega\left(\frac{C_{gs}}{1+\omega^2C_{gs}^2R_{gs}^2}+\frac{C_{gd}}{1+\omega^2C_{gd}^2R_{gd}^2}\right) & \frac{-j\omega C_{gd}}{1+\omega^2C_{gd}^2R_{gd}^2} \\ g_m e^{-j\omega\tau}-\frac{j\omega C_{gd}}{1+\omega^2C_{gd}^2R_{gd}^2} & g_{ds}+j\omega\left(C_{ds}+\frac{C_{gd}}{1+\omega^2C_{gd}^2R_{gd}^2}\right) \end{bmatrix} \quad (4)$$

By obtaining slopes of imaginary Y-parameters, real Z-parameters and imaginary Z-parameters the values of pad capacitances, extrinsic resistances and extrinsic inductances can be extracted. On solving Y_{int} and separating real and imaginary parts intrinsic small signal parameters of proposed device can be extracted. Following table show values of extracted parameters for 1x100µm^2 gate area device at ambient temperature (T_a) =290K. The extrinsic pad capacitances are extracted for frequency 0 to 5GHz under pinch off biasing. For series inductances and resistances higher frequency is used under pinch of biasing. Intrinsic Y-parameters (Y_{int}) are extracted using forward biasing after de-embedding of extrinsic parameters.

Table1: Extracted small signal and noise parameters of device

Extrinsic Parameters	Value	Intrinsic Parameter	Value
L_g	43pH	C_{gd}	1.61fF
L_s	4.9pH	C_{gs}	0.22fF
L_d	53.4pH	C_{ds}	0.90fF
R_g	8.5Ω	R_{gd}	180Ω
R_d	10Ω	R_{gs}	2.8Ω
R_s	4.70Ω	g_{ds}	429mS/mm
C_{pg}	21pF	g_m	645mS/mm
C_{pd}	21pF	τ	2.91pS
C_{pgd}	2pF	$\overline{i_{gs}^2}$	3.58x10^{-24} A^2/Hz
		$\overline{i_{ds}^2}$	2.89x10^{-24} A^2/Hz

Analytical expressions for noise parameter

Fig.2 shows small signal noise equivalent circuit model for proposed DCDMG AlGaN/GaN MODFET comprising of extrinsic and extrinsic parts along with six noise sources. Two correlated intrinsic noise sources $\overline{i_{gs}^2}$ and $\overline{i_{ds}^2}$ are characterized by mean quadratic value in their band width Δf centred on the frequency (f). As per Pucel et al. [29] model (also called PRC model), the short-circuit noise currents at gate and drain are modeled by:

$$\overline{i_{gs}^2} = 4kT_a\frac{\omega^2C_{gs}^2R}{g_m}\Delta f \quad (5)$$

$$\overline{i_{ds}^2} = 4kT_a g_m P\Delta f \quad (6)$$

The cross correlation between $\overline{i_{gs}^2}$ and $\overline{i_{ds}^2}$ can be expressed

$$\overline{i_{gs}^* i_{ds}} = 4kT_a\omega C_{gs}C\sqrt{PR}\Delta f \quad (7)$$

Where P and R are the drain and gate noise model parameters, and C is the correlation coefficient. T_a is ambient temperature and symbol k (=1.38x10^{-23}J/K) is Boltzmann's constant. For the condition C_{gs} << 1, the coefficients R, P, and C can be written in terms of gate and drain temperature of the Pospieszalski model [31-32] as

$$\mathrm{Im}(C) = -\sqrt{\frac{R}{P}} \quad (8)$$

$$R = g_m R_{gs}\frac{T_g}{T_a} \quad (9)$$

$$P = R + \frac{T_d}{g_m R_{gs} T_a} \quad (10)$$

Where T_g and T_d represent the temperatures of the intrinsic gate-source resistance (R_{gs}) and output conductance (g_{ds}) respectively. Noise behavior of the extrinsic access resistances R_g, R_d and R_s is represented by following analytical expressions

$$\overline{e_g^2} = 4kT_a R_g\Delta f \quad (11)$$

$$\overline{e_s^2} = 4kT_a R_s\Delta f \quad (12)$$

$$\overline{e_d^2} = 4kT_a R_d\Delta f \quad (13)$$

Noise model parameter derivations

For noise performance analysis and modelling, the DCDMG AlGaN/GaN MODFET, can be treated here as a black box of a noisy two port network. Noise behavior of a linear noisy two-port network can be characterized by the four noise parameters as minimum noise figure (F_{min}), noise resistance (R_n), optimum conductance (G_{opt}) and optimum susceptance (B_{opt}). On the basis of these the noise factor (F) can be modeled as

$$F = F_{\min} + \frac{R_n}{G_s}\left[\left(G_s+G_{opt}\right)^2\left(B_s+B_{opt}\right)^2\right] \quad (14)$$

where G_s and B_s are real (conductance) and imaginary (susceptance) parts of source admittance (Y_s) and represented as:

$$Y_s = G_s + jB_s \quad (15)$$

Similarly optimum admittance (Y_{opt}) has real (G_{opt}) and imaginary (B_{opt}) parts and represented as:

$$Y_{opt} = G_{opt} + jB_{opt} \quad (16)$$

In terms of source reflection coefficient Γ_s, noise factor (F) can also be modeled as:

$$F = F_{\min} + \frac{4R_n}{Z_0}\frac{\left|\Gamma_{opt}-\Gamma_s\right|^2}{\left|1+\Gamma_{opt}\right|^2\left(1-\left|\Gamma\right|^2\right)} \quad (17)$$

Where $|\Gamma_{opt}|$ and $\angle\Gamma_{opt}$ are magnitude and phase of source reflection coefficient. Also normalized noise resistance (r_n) is represented as

$$r_n = \frac{R_0}{Z_0} \quad (18)$$

Noise parameter extraction setup

The procedure used for experimental determination of noise parameters of MODFETs can be a tuner-based, 50Ω noise figure measurement method. Extraction of parameters also possible using device simulation environment using extract commands. The measurement of the noise parameters is carried out by obtaining the variations of measured noise figure as a function of the source impedance. For good accuracy a minimum of four independent measurements are required. For very higher accuracy in results it is important to take more than four measurements. After measurement curve fitting approaches are utilized to obtain noise parameters of the device under test.

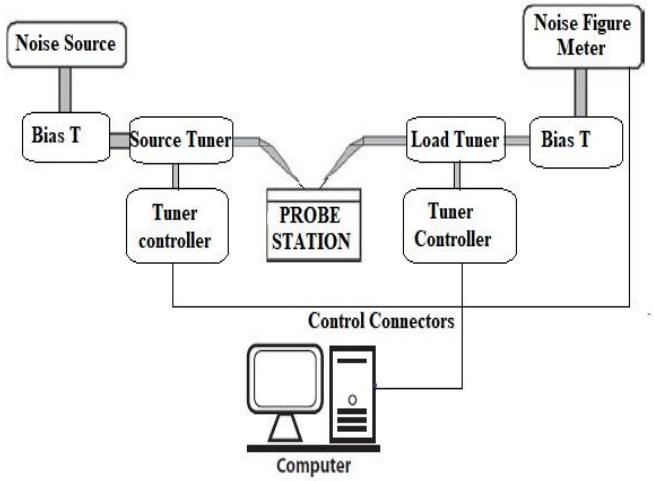

Figure 3: Block diagram for noise setup

By analyzing the variation of measured noise figure as a function of the source impedance the noise parameters can also be extracted. Figure 3 shows block diagram of computer and tuner based noise parameters extraction setup used for parameter extraction of semiconductor devices. It is true that the tuner based technique gives accurate results but it has negative point that it is time consuming and requires expensive automatic broadband microwave tuners that need complex calibration procedures before we can start accurate measurement. Some researchers proposed improved methods of using the equivalent transistor noise model to provide additional information to reduce complexity in the measurement procedure.

Scalable model derivation

A large gate area MODFET device can be treated as of n elementary cells where n is an integer with the same gate width connected in parallel. If we consider that elementary cell gate width is W^c, then the total gate-width can be obtained as nW^c. On the basis of the noise correlation technique, the admittance noise correlation matrix for large gate width size MODFET device can be expressed as

$$C_y = nC_y^c \quad (19)$$

Also the noise model relationship between large gate width MODFET device and elementary cell can be expressed as

$$P = P^c \quad (20)$$

$$R = R^c \quad (21)$$

$$C = C^c \quad (22)$$

Here we use scaling rules of the noise parameters for intrinsic elements of device as, minimum noise figure F_{min} remains unchanged, noise resistance (R_n) is inversely proportional to number of the elementary cells, optimum source conductance G_{opt} and optimum source susceptance B_{opt} are proportional to number of the elementary cells as follows

$$F_{\min} = F_{\min}^c \quad (23)$$

$$R_n = \frac{1}{n} R_n^c \quad (24)$$

$$G_{opt} = nG_{opt}^c \quad (25)$$

$$B_{opt} = nB_{opt}^c \quad (26)$$

RESULTS AND DISCUSSIONS

The proposed device is simulated using Silvaco TCAD ISE as a device simulation environment [36]. Numerical modeling is done using MATLAB software. The simulated device structure contour depicting device epitaxial layers, field plate, electrodes and dual material gate structure with Si_3N_4 passivation layers is shown in Fig.4. The magnified view of layers is also added for the purpose of clarity and better readability of device contour. Fig.5 shows logarithmic potential contour depicting potential profile of device. The modeled and simulated S-parameters (S_{11}, S_{12}, S_{21} and S_{22}) of the proposed device are shown and compared in Fig.6. It is clear that S_{11} and S_{22} follow capacitance circles and approach towards matching points with rise in frequency up to 120 Ghz. Similarly S_{12} and S_{21} follow inductance circles and approach towards matching points. From smith plot it is clear that device stable for microwave range of frequency up to 120 GHz.

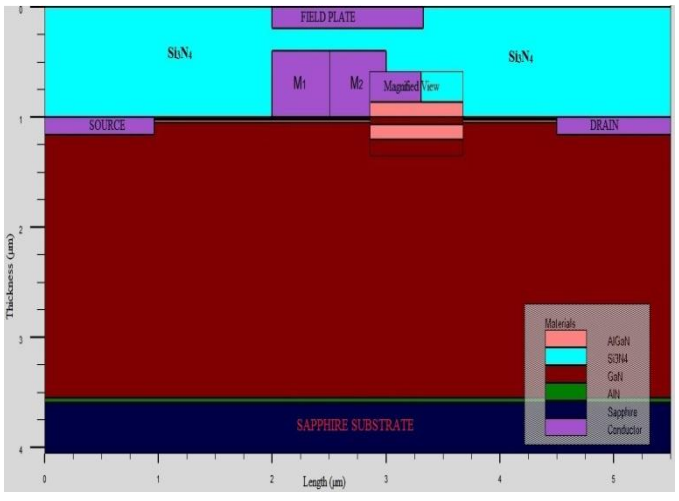

Figure 4: Simulated structure contour of device

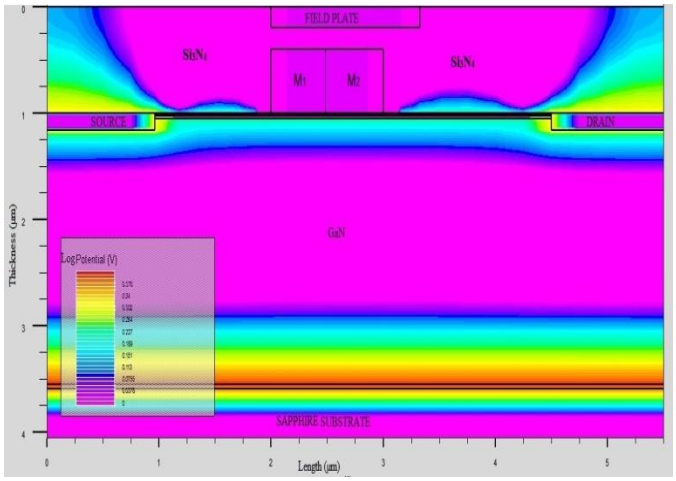

Figure 5: Simulated potential contour of device

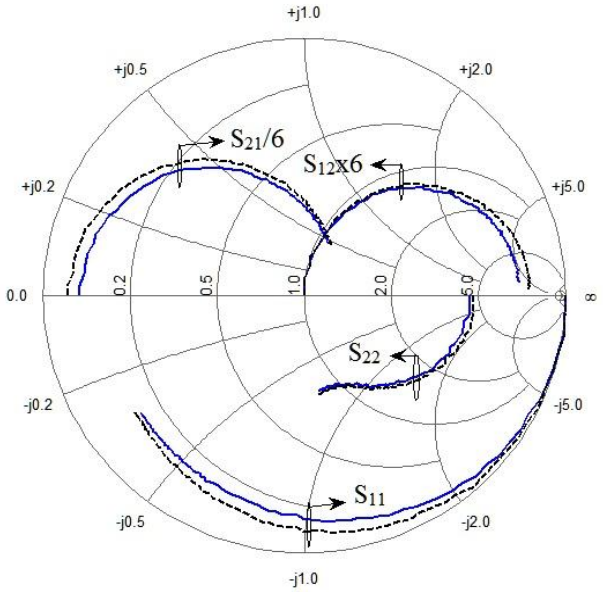

Figure 6: Comparison of modeled and simulated S-parameters of proposed device

Fig.7 shows extrinsic inductances (L_s, L_g and L_d) versus frequency plot depicting effects of frequency on parasitic inductive elements of the model. It is clear that inductances are almost same with rise in frequency up to 120 GHz. Fig.8 depicts variations of intrinsic capacitances versus frequency for modeled and simulated structure. It is clear from the plot that minor dip occurs at higher frequency keeping intrinsic capacitance almost constant for whole the microwave range of frequency thus proving superior performance of intrinsic part of device.

Fig.9 shows noise model PRC parameters versus drain current plot for device. These parameters are increasing slightly with drain current depicting increment in noise figure with rise in drain current. Fig.10 shows NF_{min} versus operating frequency plot up to 12 GHz, It is clear that a minimum noise figure of 0.52 dB was obtained at 1 GHz where as it rises to 1.65dB at 12 GHz of operating frequency. From the plot it is clear that DCDMG AlGaN/GaN MODFET can be used for LNA design with superior noise performances in comparison to conventional MODFETs. The accuracy of model is validated with simulated and experimental results [22].

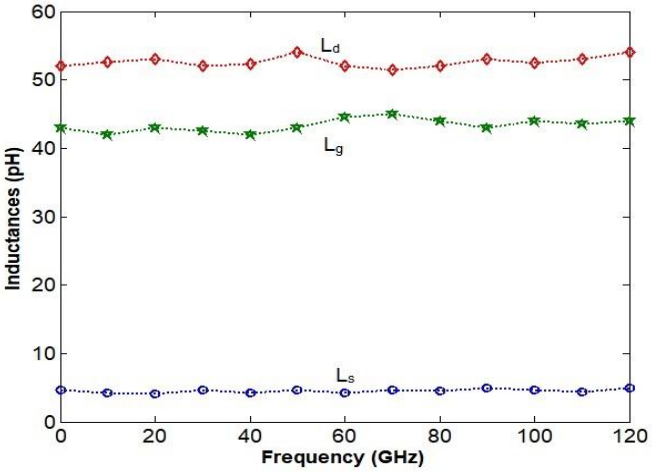

Figure 7: Extrinsic inductances versus frequency plot

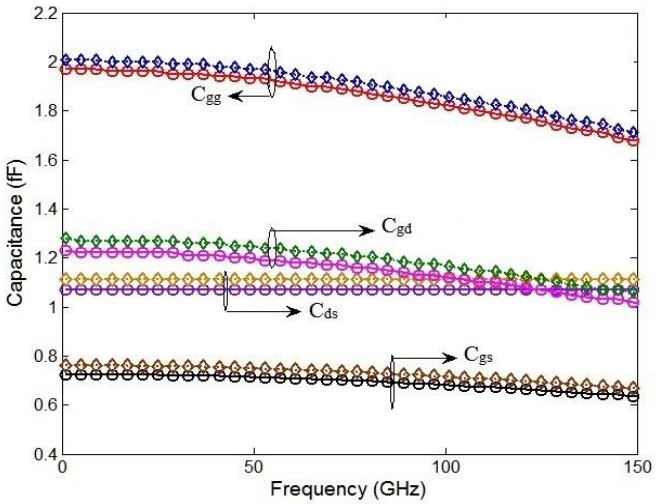

Figure 8: Intrinsic capacitances versus frequency plot model (diamond with dashed lines) simulated (circle with solid lines)

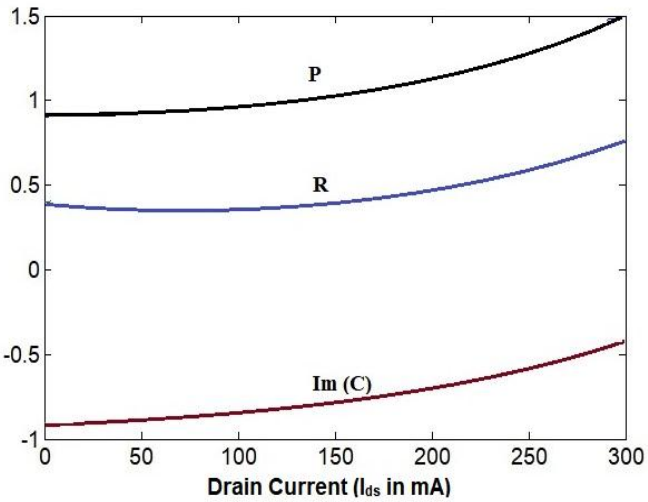

Figure 9: Noise model PRC parameters versus drain current plot

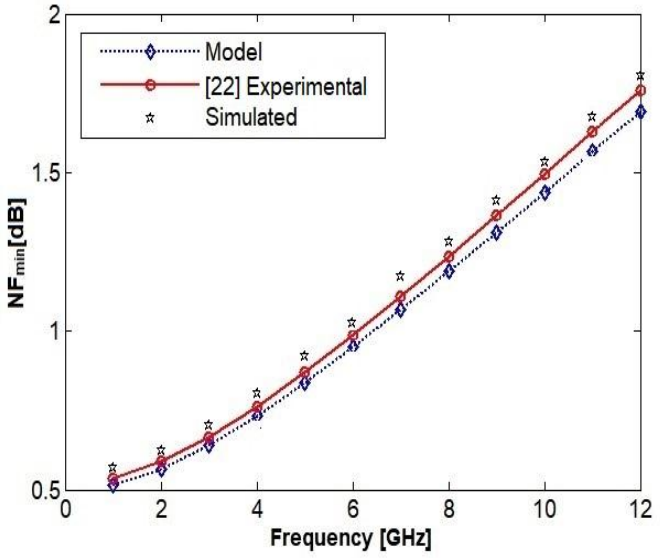

Figure 10: Minimum noise figure NF_{min} versus frequency curve

Fig.11 shows plot between normalized noise resistance and operating frequency for model, simulation and closely similar device experimental results [37]. It is clear from plot that normalized noise resistance decreases with rise in operating frequency. Fig.12 represents magnitude of source reflection coefficient versus frequency for model, simulated and experimental results. Magnitude of source reflection coefficient found to decrease with rise in frequency from 0.83 to 0.63. Fig.13 shows phase of source reflection coefficient that changes from 4 degrees at 1GHz to 58 degrees at 12 GHz of frequency. A comparison is done in the figure between simulated and reported experimental results. Figure shows that model results are in close conformity with simulation and experimental results thus validating model accuracy and reliability for proposed novel device structure.

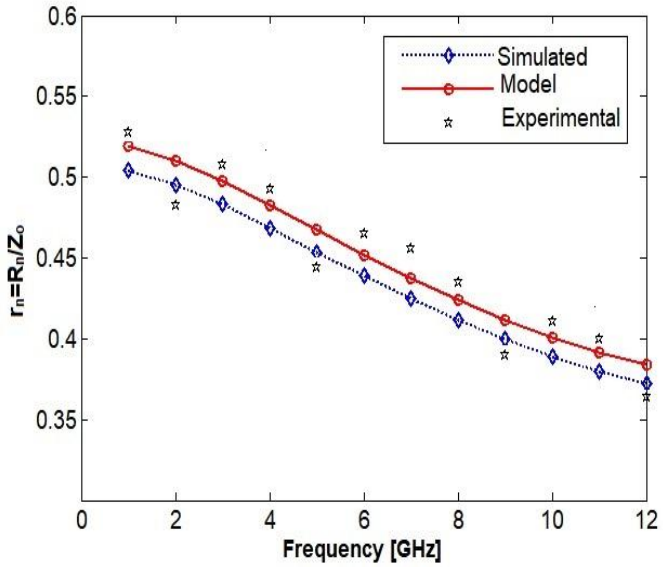

Figure 11: Normalized noise resistance versus frequency plot

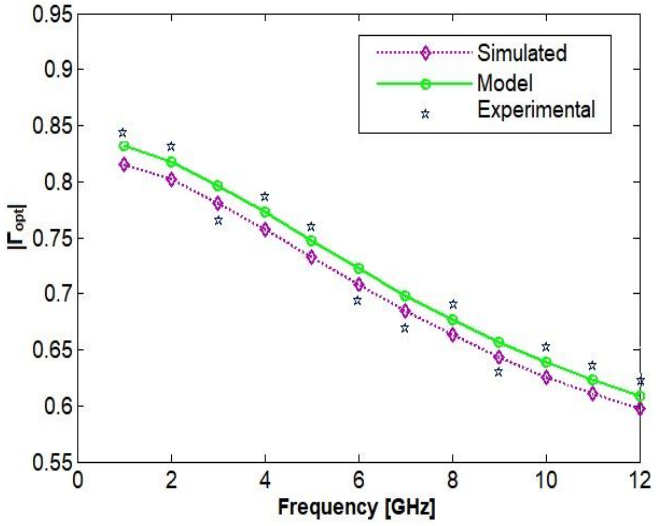

Figure 12: Magnitude of source reflection coefficient versus frequency

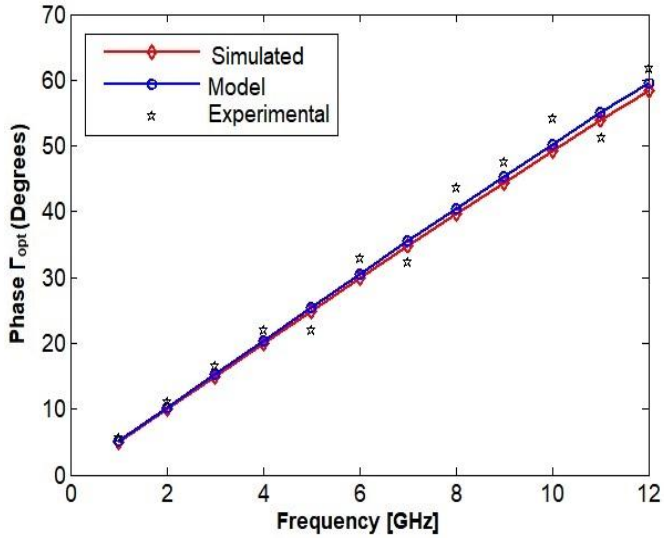

Figure 13: Angle of source reflection coefficient versus frequency plot

CONCLUSION

In this article we extracted noise parameters and modeled novel field plated DCDMG AlGaN/GaN MODFET in order to characterize device for noise performances and to predict device suitability as an improved low noise amplifier. As discussed above we obtained minimum noise figure NF_{min}=0.52dB at 1GHz and NF_{min}=1.65dB at 12 GHz from simulated as well as from modeled results. We also simulated and modeled normalized noise resistance, magnitude and phase angle of source reflection coefficient for the proposed device. On the basis of modeled and simulated results and further analysis of reported experimental results it can be concluded that proposed device has superior noise performance in comparison of conventional GaN MODFETs. The proposed device can be used for design of high power low noise amplifier operating in microwave range of

frequency. The noise parameters extracted from the proposed circuit model are validated with recently published results of closely similar GaN MODFETs.

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AUTHOR'S PROFILE

Rahis Kumar Yadav, was born in Uttar Pradesh, India. He received AMIE degree in Electronics and Communication Engineering from "The Institution of Engineers (India)" in 1995 and M.Tech degree in Electronics Design and Technology from Tezpur University, Assam, India. He also completed post graduate diploma in embedded system and VLSI design from Centre of Development of Advanced Computing and Cadence VLSI Certification Program from Cadence Design Systems. He served in Indian Air Force and has 10 years of experience as faculty of electronics and communication engineering in reputed engineering institutions and universities. Presently he is part time research scholar in the department of electronics and communication engineering, School of Engineering and Technology, Sharda University, Gr.Noida, India. He has authored and pulished nine research articles for peer reviewed journals and authored four research articles for national and international conferences. His research interests include modeling and simulation of semiconductor devices, VLSI design and embedded system design using fine mechanics. He is life corporate member of "The Institution of Engineers (India)" and life member of Indian Society of Technical Education.

Pankaj Pathak, was born in India. He received B.Sc. Physics and M.Sc. Physics specialization in electronics, all from Rohilkhand University, India in 1992 and 1994 respectively. He received his Ph.D. degree in electronic Science from University of Delhi in 2000. He also completed a postgraduate level course from Institution of Electronics & Telecommunication Engineers, Delhi. He is currently Director (R&D) with Kadenza Infosolutions Pvt. Ltd., India and adjunct faculty in school of engineering and technology, Sharda University. He was with department of electronic science, University of Delhi as Research Scholar/Lecturer from 1996 to 2000. He is life corporate member of Institution of Electronics & Telecommunication Engineers and member of Semiconductor Society of India. His research interests include semiconductor devices, wireless communication & microwave systems, VLSI and embedded system design. He has authored eight research papers in international journals, conferences and had two patents in IT industry.

R.M. Mehra, was born in New Delhi, India on January 17, 1945. He received B.Sc., M.Sc. and Ph.D. in Physics from University of Delhi, India in 1965, 1967 and 1973, won JSPS Fellowship. He has 38 years of academics and research experience with department of electronic science, University of Delhi, India. He has Supervised 42 Ph. D. research scholars and published 172 research papers in SCI journals with more than 2000 citations with *h- index 24* (SCOPUS). His area of interest is electronic materials and devices. He has written various review articles, mainly on amorphous semiconductors, which have been widely accepted and recognized by international research community. Currently, he is Chief Editor of Invertis Journal of Renewable Energy, Journal of Scientific and Technology Research, Sharda University and member of Advisory Editorial Board of Materials Science, Poland. He executed more than 16 research projects sponsored by national (DRDO, UGC, DST, CSIR, MNRE, IUAC) and international (NSF, USA & JSPS, Japan) agencies. He has widely traveled abroad for research, teaching and consultancy assignments to universities in USA, Japan and Europe. He has also chaired Semiconductor Society (India).