A Survey on ADPLL Components and their effects upon Power, Frequency and Resolution

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Abstract

The All Digital Phase Locked Loop consists of full digital components which are used in advanced communication systems like frequency synthesizer, Carrier and clock recovery, modulator/demodulator etc. Hence the performance analysis of ADPLL becomes very necessary when designing these equipments. The ADPLL contains phase detector, loop filter and Digital controlled oscillator. The performance of ADPLL depends on various factors like combination of different components, power consumption, frequency resolution, frequency locking speed etc. At present, the different combinations of components ADPLL are used to achieve fine resolution and fast lock-in time and it is appropriate for system-on-chip applications. In this paper the effects of various combinations of the internal components on the important parameters of ADPLL like frequency range, power, and algorithms used have been compared.

Keywords: Phase Locked Loop (PLL), Voltage Controlled Oscillator (VCO), Loop filter (LF), Digital PLL (DPLL), All Digital PLL (ADPLL), Digital Controlled Oscillator (DCO)

Introduction

The Phase Locked Loop (PLL) is an extremely versatile circuit used in electronic communication systems like modulator, demodulator, carrier & clock recovery, frequency generator and frequency synthesizer [20, 1, 2]. Edward Appleton introduced the first PLL in 1923 that used Automatic Synchronization of triode oscillators which were basic elements of radio communications [20, 4, 5]. In 1970, Digital PLL [20, 6] was developed using digital phase detector. The first ADPLL consisting of digital components was reported in 1980 [20, 8].

Phase Locked Loop is a control system based on closed loop used for the purpose of synchronization of the phase and frequency to the incoming signal. For this faster and efficient operation of PLL is very much desired [2]. There are two types of PLL widely used at present: Analog phase-locked loop and Digital phase-locked loop [3]. Due to the development of new techniques for the improvement of performance, speed and reliability, and the simultaneous reduction in size and cost of integrated circuits, the designers have shown a strong interest in the digital domain implementation of control and communication systems. However, due to the advances in integrated circuit (IC) fabrication and the growth in improving the overall system performance, all-digital components of PLLs have become more popular. The all-digital implementations present the opportunity to achieve a low-voltage operation, low-power consumption, scalability and less sensitivity to the noise [7]. Complexities involved in the design of system on a chip (SoC) can be reduced by ready to use IP cores.

Basics of PLL

Phase-Locked Loop (PLL) is a closed loop feedback system that locks the output signal phase or frequency by adjusting the input reference signal frequency [1][9][20]. The registers and flip flops of a circuit suffer clock skew problem, which can be solved by Phase Locked Loop. The input signals to the PLL are sinusoidal signal or clock signal.

There are three important building blocks or components in PLL—the Phase detector, Loop filter and Voltage controlled oscillator.

1. Phase/Frequency detector: It acts as a comparator and compares the phase of external input signal to the phase of VCO output signal and locks when both phases are equal. In unlock condition an error signal is generated which is equal to the phase difference between two signals [9][23]. There are two types of Phase detectors as follows:

Sinusoidal phase detector is an analog phase detector [21][23]. A zero memory device, a non-linear and output signal is proportional to the input signal amplitude and it is used in modulation demodulation techniques. Alternatively Sequential Phase detector is a digital phase detector containing sequential logic circuits like memory. These detectors provide fast synchronization with an input signal and better accuracy compared to sinusoidal phase detectors. Many phase detectors have been used with different combinations of components to realise certain features. For example, Chao-Ching Hung et. al[14] found that Bang bang
phase detector gives robustness, reduction in locked time and low power consumption. Abhisek das et al [15] have realized phase detection system by generating an analytical signal using a compact implementation of Hilbert transform and instantaneous phase computation using CORDIC algorithm.

2. Loop filter: It is used to suppress noise and high frequency of the phase detector output and provides a dc controlled signal for VCO [20, 1, 5, 6]. The low pass filter (LPF) is used as a loop filter and it filters the phase error voltage. There are four different topologies of loop filter-passive filter, active filter, digital loop filter and sequential filter. Among these filters sequential filter used along with phase/frequency detector produces no ripples. Manoj kumar et al [17] has concluded that loop filter based on K-counter removes high frequency parts of phase error signal. Abhisek das et al [15] have designed the loop filter using PI controller which has low pass behaviour and was used to discard the higher order harmonics.

3. Voltage Controlled oscillator: It generates a clock signal by controlling a frequency with in voltage. The generated signal is feedback to the input of the phase detector and compared with input reference signal [23]. The phase comparison is continued until both the phases will be locked. The important requirements of VCO are good stability in the phase, large frequency variation, linear relationship between frequency and control voltage [23]. The voltage controlled oscillator can be classified as

Tuned VCO (Harmonic oscillators based): It consists of a feedback selective network to send the selected frequency to the input. The advantage of these oscillators is their excellent jitter performance.

Non-Linear VCO (Ring Based and Relaxation based): Voltage controlled ring oscillators are used in designing low jitter and clock recovery circuits while PLL relaxation oscillator is used when non-sinusoidal output such as square wave or saw tooth is required.

Different types of PLL exist—namely linear, digital, all digital and software, out of which All Digital PLL is characterised by the full digital circuit operation which ensures low power consumption and high speed. The two important key parameters that differentiate the performance of PLL are Lock-in-range and capture range. In this paper we have analysed only the lock-in-range parameter.

Digital PLL

The important drawbacks of analog PLL are low operating speed, larger chip area, worse jitter performance and high power consumption [21][23]. These are overcome by Digital PLL where the analog phase detector is replaced by its digital counterpart.

Digital PLL allows faster lock time to be achieved and generates a clock signal for high performance microprocessor [22].

All Digital PLL

It is a modified form of Digital PLL. It consists of only Digital blocks. All Digital PLL provides high performance, better phase jitter performance, larger lock in range, speed, reliability and decrease in size and cost.

Contributions based on lock-in range

Manojkumar et al [17] used ripple reduction techniques with Ex-or phase detector, K-counter loop filter and digital controlled oscillator to get better lock-in range. The ADPLL frequency range is 11KHz to 216 KHz.

Xin-chen et al [13] used feed forward compensation algorithm with phase frequency detector, Digital loop filter, modified frequency control and a ring type Digital controlled oscillator. This combination gives good lock-in range and the maximum frequency range of this ADPLL is 416 MHz.

Chao-ching hung et al [14] achieves good lock-in range with a modified bang-bang phase detector, digital loop filter and LC based digital controlled oscillator and the frequency of ADPLL is 40 GHz.

Inferences:
The modified bang bang detector reduces lock-in time and the inductor added along with the LC based DCO increases tuning range [14].

ADPLL with ripple reduction technique shows better lock-in range (11 KHz to 216 KHz) than ADPLL without ripple reduction technique (0 KHz to 199 KHz) with centre frequency of 100 KHz and hence it can be used for high frequency applications [17].

The feed forward compensation technique used in ADPLL gives fast locking and good lock-in range, since the frequency divider is fully reused [13].

The ADPLL designed using frequency estimation algorithm achieves good lock-in range with less lock-in time [10].

Contributions based on Power consumption

Liangge Xu et al [11] designed an ADPLL for the frequency of 2GHz with variable phase accumulator, digital loop filter and time to digital converter by utilizing low power consumption. The clock gating used in time to digital converter also saves power.

Anitha babu et al [22] designed a low power ADPLL with D-flip-flop phase detector, digital loop filter and digital controlled oscillator with controller. Modified D-flip-flop used in the Phase/Frequency Detector has low power consumption and lock-in time is also reduced.

J. choi et al [5] designed a low power wide range ADPLL for clock generation with power consumption of 16. 2 mW at 2.16 GHz with delay locked loop, pulse generator and pulse combiner. The Delay Locked Loop consists of D-flip-flop based phase detector, loop filter and voltage controlled delay line.

Xin chen et al [13] designed an ADPLL consisting of phase frequency detector, digital loop filter, Ring oscillator and a modified frequency control with feed forward compensation techniques with low power consumption of 11. 39 mW.

Chao-ching hung et al [14] describes a 40 GHz ADPLL with a modified bang-bang phase detector, digital loop filter and LC based digital controlled oscillator with power consumption of 46 mW.
Inferences:
The bang-bang phase detector gives robustness, low power consumption and it also reduces lock-in time but at the same time it gives slow frequency tracking and this is considered as a drawback for this phase detector. The ADPLL designed using bang-bang phase detector generating 40 GHz with power consumption of 46 mW [14].

The time to digital converters are constructed by a series of tapped constant delays and the drawback is phase accuracy depends on accuracy and temperature stability of delays [16]. In double edge triggered D-flip-flop power dissipation is less and it achieves the locked state with less lock-in time. Modified D-flip-flop (D value always remains high) used in phase/frequency detector has low power consumption [22]. By adding certain functions in ADPLL we can reduce power. For example, the clock gating used in the time to digital converter saves power. We can also reduce the power consumption by setting a mode selection for DCO [22].

Contributions based on frequency resolution
Chao-ching hung et al [14] designed an ADPLL with modified bang-bang phase detector, digital loop filter and LC based digital controlled oscillator and achieves good frequency resolution and the frequency of ADPLL is 40 GHz. Liangge Xu et al [11] designed an ADPLL with variable phase accumulator, digital loop filter and time to digital converter and achieves good frequency resolution and the frequency of ADPLL is 2 GHz. Stefo. R et al [24] designed an ADPLL based clock generator with phase frequency detector, loop filter, digital controlled oscillator and generates a high resolution clock signal and the maximum frequency achieved is 40 GHz.

Inferences:
The frequency resolution of Digital Controlled Oscillator can be improved by implementing the feedback path between Digital Controlled Oscillator and the phase/frequency detector using the reprogrammable fractional frequency divider [24]. Ring voltage controlled oscillator has many ways to control the frequency and the frequency tuning range is also wide and the drawbacks are high phase noises and poor stability at high frequencies. ADPLL designed using Ring voltage controlled oscillator has a wide tuning frequency range of 4MHz to 416 MHz with power consumption of 11. 394 mW [13].

LC voltage controlled oscillator has low phase noise and good stability at high frequencies and the drawbacks are narrow tuning range and large layout area. The inductor added along with the LC based DCO improves narrow tuning range of an obtained frequency 40 GHz [14].

The frequency estimation algorithm used in Digital controlled oscillator gives an 8. 8 ps resolution with a frequency range of 28-446 MHz [10]. The frequency resolution of digital controlled oscillator can be improved to 5 ps by adding a fine tuning delay cell consist of AND-OR-INV or OR-AND-INV to the tuning system of Digital control oscillator. The above mentioned information is summarized in table I and table II.

Design Parameters Of ADPLL
The important design parameters are

1. Stability: ADPLL is stable if poles of characteristic equation lie within the unit circle.
2. Errors in ADPLL: There are two types of errors in ADPLL. (i) Phase error (ii) Frequency error. The selected ADPLL components should minimise the errors. Deok-soo kim et al [12] has proved that phase frequency detector based time to digital converter can detect phase error and also frequency error.
3. Power consumption: In ADPLL power consumption reduces up to 20% because charge pump based detectors, current controlled oscillators and voltage to current converters are not used. Chao-ching et al [14] has suggested that phase frequency detector reduces power consumption less than a phase detector.
4. Jitter reduction: Jitter is the deviation of signal from its ideal position with respect to time. The main source of jitter is the internal circuitry of PLL. Deepika Ghai et al [20] mentioned that when PLL is used in clock recovery circuit it reduces the jitter in voltage controlled oscillator.

Table I: Different Combinations of Components

<table>
<thead>
<tr>
<th>Sl. No</th>
<th>Target Parameters</th>
<th>Phase detector</th>
<th>Loop filter</th>
<th>VCO</th>
<th>Techniques</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Lock-in range [17]</td>
<td>Ex-OR</td>
<td>K-counter</td>
<td>Digital controlled oscillator</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>Lock-in range [13]</td>
<td>Phase frequency detector,</td>
<td>First order digital loop filter</td>
<td>Ring oscillator DCO with a modified freq control</td>
<td>Feed forward Compensation</td>
</tr>
<tr>
<td>3</td>
<td>Lock-in range [14]</td>
<td>Modified bang bang phase detector</td>
<td>Digital loop filter</td>
<td>LC based DCO</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>Less Lock-in time [10]</td>
<td>Phase frequency detector</td>
<td>Digital loop filter</td>
<td>Digital controlled oscillator</td>
<td>Frequency estimation algorithm</td>
</tr>
<tr>
<td>5</td>
<td>Low Power consumption [11]</td>
<td>Variable phase accumulator,</td>
<td>Digital loop filter</td>
<td>LC based DCO</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>Low Power consumption [22]</td>
<td>D flip-flop</td>
<td>Digital loop filter</td>
<td>Digital controlled oscillator with controller</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>Low Power consumption [13]</td>
<td>Phase frequency detector</td>
<td>First order digital loop filter</td>
<td>Ring oscillator DCO with a modified freq control</td>
<td>Feed forward Compensation</td>
</tr>
</tbody>
</table>
Multiple methods of clocks synchronization are used in various applications. Phase frequency detector is used for clock synchronization because it is not sensitive to edges and phase detector eliminates the limitation in number of bits. The linear phase detector produces a digital output proportional to the input phase and slow pull in process but the drawbacks are not sensitive to edges and phase detectors are sensitive to edges. JK-flip-flop phase detectors are sensitive to edges therefore gives good reliability of data. Flip-flop counter phase detector eliminates the limitation in number of bits. In phase frequency detector, a large phase tracking range can be achieved and there is no chance of occurrence of ripples. In double edge triggered D flip-flop, less power dissipation and very fast lock state can be achieved. For applications on data and clock recovery, EX-OR phase detector is used because it is not sensitive to edges and phase frequency detector is used for clock synchronization and frequency synthesis. Since Phase frequency detector is sensitive to edges, it is not suitable for data & clock recovery [23]. Loop filter acts as a control circuitry for VCO. UP/Down counter loop filter is used with any type of phase detector and the important advantage of this combination is design part and the circuit is very simple. The K-counter based Loop filter can be operated with only EX-or or JK-flip-flop and is not suited for other detectors. Nowadays Digital loop filters combined with phase frequency detectors are used in ADPLL. Depending upon the output of loop filter, the oscillator will change its frequency. Divide by N counter DCO is a simple structure but it doesn’t offer jitter design criteria and the increment decrement counter provides good control over hold range and lock in range.

Bang-bang phase detector (non-linear) is preferred for the design of ADPLL because of its good robustness and the low power consumption Ring voltage controlled oscillator offers a wide frequency range due to its multiple methods of controlling the frequency and generation of clock.

Tables I and II give the details of comparison on different combinations of components, techniques, power consumption, lock-in range and frequency resolution of ADPLL and the conclusion on the basis of the table should be given.

### Conclusions

The research papers detailing the design parameters with different components of ADPLL were compared and the conclusions are given on the basis of the advantages of different components Vs suitability of components for various applications. The linear phase detector produces a digital output proportional to the input phase. For higher resolution, it requires analog circuitry. But it increases the overall design complexity. The non-linear phase detector consists of only logic gates and is the simplest and most robust. The Ex-or phase detector gives an error pulse based on both the edges and slow pull in process but the drawbacks are not sensitive to edges.

**Table II: Comparisons of Different ADPLLs**

<table>
<thead>
<tr>
<th>Work</th>
<th>Technique</th>
<th>Frequency</th>
<th>Power consumption/Dissipation</th>
<th>Area</th>
<th>Process</th>
<th>Peak to peak jitter</th>
<th>Advantages</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>[5]</td>
<td>Programmable DLL-based Clock generator for high multiplication factor</td>
<td>1.2 GHz (Input frequency) 120 MHz to 2.16 GHz (Output frequency)</td>
<td>16.2 mW at 2.16 GHz (Consumption)</td>
<td>0.051 mm²</td>
<td>0.18 µm</td>
<td>19 ps</td>
<td>Less jitter problem and tackle harmonic locking problem</td>
<td>Multiple clock signals with high multiplication factor</td>
</tr>
<tr>
<td>[7]</td>
<td>ADPLL for high speed Clock generation</td>
<td>45 MHz to 510 MHz (Output frequency)</td>
<td>100 mW at 500 MHz (Dissipation)</td>
<td>0.71 mm²</td>
<td>0.35 µm</td>
<td>70 ps</td>
<td>Smaller area, low power consumption than cell based, shorter lock in time</td>
<td>Suitable for On-chip applications</td>
</tr>
<tr>
<td>[11]</td>
<td>Delay based technique to reduce power dissipation</td>
<td>12 MHz (Input Frequency) 2.4 GHz (Output frequency)</td>
<td>12 mW (Consumption)</td>
<td>0.24 mm²</td>
<td>65 nm CMOS</td>
<td>-</td>
<td>Wide frequency range and good phase noise performance with low power consumption</td>
<td>Suitable for ISM band applications</td>
</tr>
<tr>
<td>[17]</td>
<td>ADPLL with ripple reduction technique</td>
<td>11 KHz to 216 KHz (Output frequency)</td>
<td>-</td>
<td>-</td>
<td>0.65 nm</td>
<td>-</td>
<td>Good locking range and capture range</td>
<td>High frequency circuits</td>
</tr>
<tr>
<td>[10]</td>
<td>Freq. Estimation algorithm (FEA) for fast locking</td>
<td>220 KHz to 8 MHz (Input frequency) 28 to 446 MHz (Output frequency)</td>
<td>-</td>
<td>0.075 mm²</td>
<td>0.18 µm CMOS</td>
<td>70 ps</td>
<td>Fast lock in time, low power and good frequency resolution</td>
<td>ADPLL is suitable to be integrated with various designs</td>
</tr>
<tr>
<td>Reference</td>
<td>Title</td>
<td>Authors</td>
<td>Journal/Vol/Year</td>
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