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A 0.9-V 176-nW Curvature-Compensated Voltage Reference in 0.35-μm CMOS Technology

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Abstract

A curvature-compensated CMOS voltage reference, which uses subthreshold MOSFETs without BJTs, is presented in this paper. The curvature compensation is achieved by utilizing the exponential characteristics of subthreshold MOSFETs to compensate the high-order temperature dependence of an MOSFET gate-to-source voltage. The proposed voltage reference, designed in a 0.35-μm CMOS technology with V_{thn} = 0.63 V and $|V_{thp}|$ = 0.79 V, can operate down to a 0.9 V supply. Simulation results show that the designed reference circuit generates a reference voltage of 326 mV and consumes 176 nW. A temperature coefficient of 26.4 ppm/℃ in a range of -30 to 75 ℃ and a line regulation of 0.73 %/V are achieved. The circuit layout occupies 0.78 mm x 1.1 mm.

Keywords: Voltage Reference, Curvature Compensation, Temperature Compensation, CMOS, Subthreshold MOSFETs.

INTRODUCTION

Reference circuits are essential in implementing most analog and digital systems to generate precise reference signals insensitive to Process, supply Voltage and Temperature (PVT) variations. Analog circuits operating with low supply voltages are in great demand due to their usage in low-power low-voltage systems such as portable devices, wearable biomedical devices and wireless sensor nodes.

Conventional CMOS bandgap references (BGR) exploit parasitic BJTs in CMOS technology and generate an output voltage of about 1.2V, which might not meet the low-voltage constraints for low-voltage and low-power applications. Sub-1V operation is possible in current-mode bandgap references [1, 2]. However, they still use BJTs to achieve temperature compensation, and thus the minimum requirement of about 0.6V base-emitter voltage (V_{BE}) limits the lower bound of supply voltage.

In conventional BGR circuits based on first-order temperature compensation, the temperature coefficient (TC), one of the major BGR performance parameter, is limited between 20 and 100 ppm/℃ [3], and the theoretical minimum TC over temperature range of 100℃ is approximately 21 ppm/℃ [4]. This nonideality is mainly due to the higher-order temperature dependence of V_{BE} . In order to overcome the limitation, many high-order temperature compensation approaches have been developed, such as quadratic temperature compensation [5], utilizing a non-linear current generated by using an extra BJT [6, 7], exponential temperature compensation [8], piecewise-linear curvature correction [9, 10, 11], based on temperature-dependent resistor ratio with high resistive poly resistor and a diffusion resistor [12], and piecewise-nonlinear curvature correction [3]. Most curvature-compensation

techniques require additional components and power consumption.

Recently, a sub-μW BGR circuit [4] has been proposed that has inherent curvature-compensation property while having relatively low circuit complexity and low current consumption. In this circuit, the curvature-compensation is achieved by utilizing the exponential characteristics of subthreshold CMOS transistors to compensate the BJT base-emitter voltage high-order temperature dependence. However, this technique may be undesirable due to mismatch between two different devices, MOSFET and BJT. In addition, they still use BJTs to achieve curvature compensation, and thus the minimum supply voltage is greater than 1 V.

In this paper, a curvature-compensated CMOS voltage reference is proposed. Sub-1V operation is possible by using subthreshold MOSFETs without BJTs, and curvature compensation is achieved by utilizing the exponential characteristics of sub-threshold MOSFETs to compensate the high-order temperature dependence of an MOSFET gate-to-source voltage (V_{GS}). The proposed circuit is designed in a 0.35-μm CMOS technology.

PROPOSED VOLTAGE REFERENCE CIRCUIT

The idea of the proposed curvature-compensation technique is illustrated in Fig. 1. Assuming that all the PMOS transistors operate in the subthreshold region and are saturated ($V_{SG} >> V_T$), their drain current is given by

$$I_{SD} = \mu C_{ox}(n-1)V_T^2 \frac{W}{L}\exp\left(\frac{V_{SG}-|V_{th}|}{nV_T}\right) \quad (1)$$

where μ is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, n is the subthreshold slope parameter, $V_T = kT/q$ is the thermal voltage (k is the Boltzmann constant, q is the elementary charge and T is the absolute temperature), W/L is the transistor aspect ratio, V_{SG} is the source-to-gate voltage, V_{th} is the MOSFET threshold voltage.

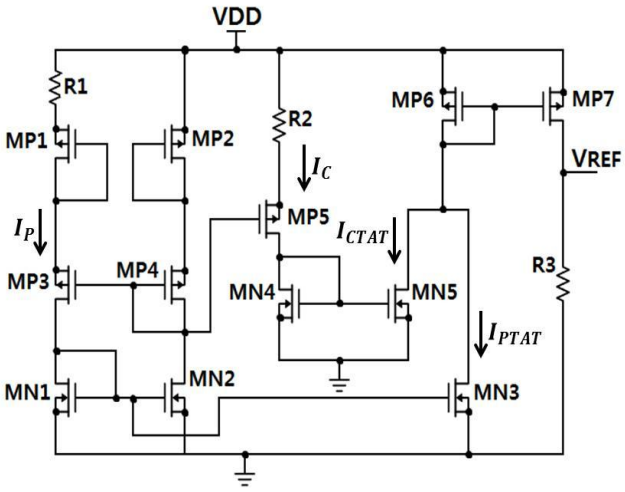

Figure 1: Simplified schematic of the proposed voltage reference circuit.

A PTAT (Proportional To Absolute Temperature) current is generated by MP1, MP2, and R1. Neglecting the mismatches between components and the short-channel effects of the MOS transistors, the PTAT current I_P can be expressed as

$$I_P = \frac{V_{SG2}-V_{SG1}}{R_1} = \frac{nV_T\ln(K)}{R_1} = \frac{kn\ln(K)}{qR_1}T \quad (2)$$

For the PMOS transistor MP2 with a PTAT drain current, the source-to-gate voltage V_{SG2} with respect to the temperature can be expressed as [13,14]

$$V_{SG2} = A_0 + A_1T + A_2T\ln T \quad (3)$$

where the constants A_0, A_1, A_2 are dependent on the process technology. It can be rewritten as

$$V_{SG2} = a_0 + a_1T + a_2T\ln\frac{T_R}{T} \quad (4)$$

where $a_0 = A_0$, $a_1 = A_1 + A_2\ln T_R$, $a_2 = -A_2$, and T_R is the reference temperature.

A CTAT (Complementary To Absolute Temperature) loop is formed by MP2, MP4, MP5, and R2. It can be seen from the loop that

$$V_{SG2} + V_{SG4} = V_{SG5} + R_2I_C \quad (5)$$

$$I_C = \frac{V_{SG2}}{R_2} + \frac{V_{SG4}-V_{SG5}}{R_2} \quad (6)$$

Assuming $(W/L)_4 = (W/L)_5$ and $V_{th4} = V_{th5}$, we have

$$I_C = \frac{1}{R_2}\left(V_{SG2} + n V_T \ln\frac{I_P}{I_C}\right) = \frac{1}{R_2}\left(a_0 + a_1 T + \underbrace{a_2 T \ln\frac{T_R}{T} - n V_T \ln\frac{I_C}{I_P}}_{Nonlinear terms}\right) \quad (7)$$

The high-order temperature dependent term of V_{SG2} (the third term) can be offset by the fourth term that is the ΔV_{SG} of subthreshold MOSFETs, MP4 and MP5.

By using Talyor series, $\ln(x) \approx x - 1$ for $x \approx 1$. Therefore, if both T_R/T and I_C/I_P are approximately equal to one within a certain range of temperature, the nonlinear terms can be written as:

$$I_{C,NL} = \frac{1}{R_2}\left[a_2 T \ln\frac{T_R}{T} - n V_T \ln\frac{I_C}{I_P}\right] \approx \frac{V_T}{R_2}\left[\frac{q}{k} a_2\left(\frac{T_R}{T} - 1\right) - n\left(\frac{I_C}{I_P} - 1\right)\right] = \frac{V_T}{R_2}\left[\frac{q}{k} a_2\left(\frac{T_R}{T} - 1\right) - n\left(\frac{I_R - I_P}{I_P} - 1\right)\right] \quad (8)$$

If the higher-order temperature dependence of the CTAT current is compensated, I_C is also first-order temperature-dependent, and $I_P + I_C$ is constant at all temperature. Then, $I_P + I_C$ can be expressed at $T = T_R$ as

$$I_P + I_C = 2I_P(T_R) = 2\frac{kn\ln(K)}{qR_1} T_R \quad (9)$$

By substituting (9) into (8),

$$I_{C,NL} = \frac{V_T}{R_2}\left[\frac{q}{k} a_2\left(\frac{T_R}{T} - 1\right) - n\left(\frac{2I_P(T_R) - I_P}{I_P} - 1\right)\right] = \frac{V_T}{R_2}\left[\frac{q}{k} a_2\left(\frac{T_R}{T} - 1\right) - n\left(\frac{2T_R - T}{T} - 1\right)\right] = \frac{V_T}{R_2}\left[\left(\frac{q}{k} a_2 - 2n\right)\frac{T_R}{T} - \left(\frac{q}{k} a_2 - 2n\right)\right] \quad (10)$$

the nonlinear terms become almost zero. As a result,

$$I_C \approx \frac{1}{R_2}(a_0 + a_1 T) \quad (11)$$

Thus the output reference voltage becomes

$$V_{REF} = R_3(I_P + I_C) = \frac{R_3}{R_2}\left[a_0 + a_1 T + \frac{R_2}{R_1} n V_T \ln(K)\right] \quad (12)$$

Therefore, a temperature-independent V_{REF} can be achieved by setting

$$\frac{R_2}{R_1} = \frac{-a_1 T}{n V_T \ln(K)} = \frac{-q a_1}{kn\ln(K)} \quad (13)$$

and V_{REF} becomes

$$V_{REF} = \frac{R_3}{R_2} a_0 \quad (14)$$

CIRCUIT DESIGN AND SIMULATION RESULTS

The proposed voltage reference circuit is designed in a 0.35-µm CMOS technology with V_{thn} = 0.63 V and $|V_{thp}|$ = 0.79 V. The schematic including a start-up circuit is shown in Fig. 2. To increase the output resistances of the simple current mirrors (MN1-MN2-MN3, MN4-MN5, and MP6-MP7) in Fig. 1, composite transistors [15] operating in subthreshold region are employed. By using the composite transistors, the output impedance of the current mirror becomes comparable to that of a cascade current mirror without affecting its output-voltage swing and without requiring any additional power dissipation. To further improve the VDD sensitivity performance, an operational amplifier (op-amp) is added to make the voltage at nodes A and B to be approximately the same. The op-amp schematic is shown in Fig. 3. Bulk-driven technique (MP3, MP4) and composite transistors (MN1-MN3, MN2-MN4) are also employed for low-voltage operation. The designed op-amp has a dc gain of 76 dB and consumes 53 nA from a 0.9 V power supply.

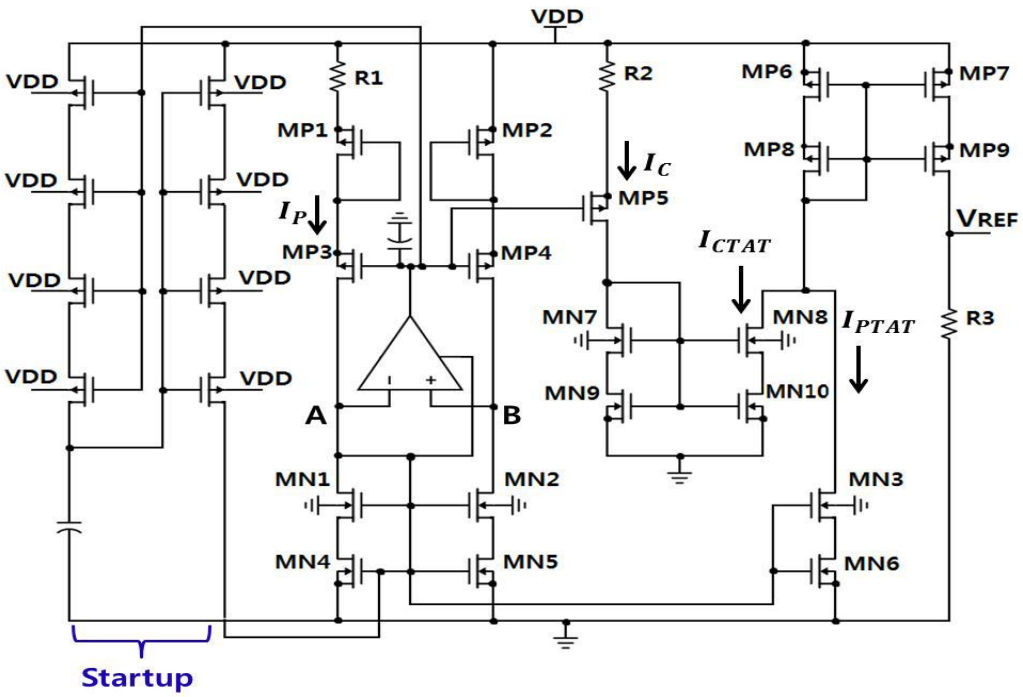

Figure 2: Schematic of the designed voltage reference circuit.

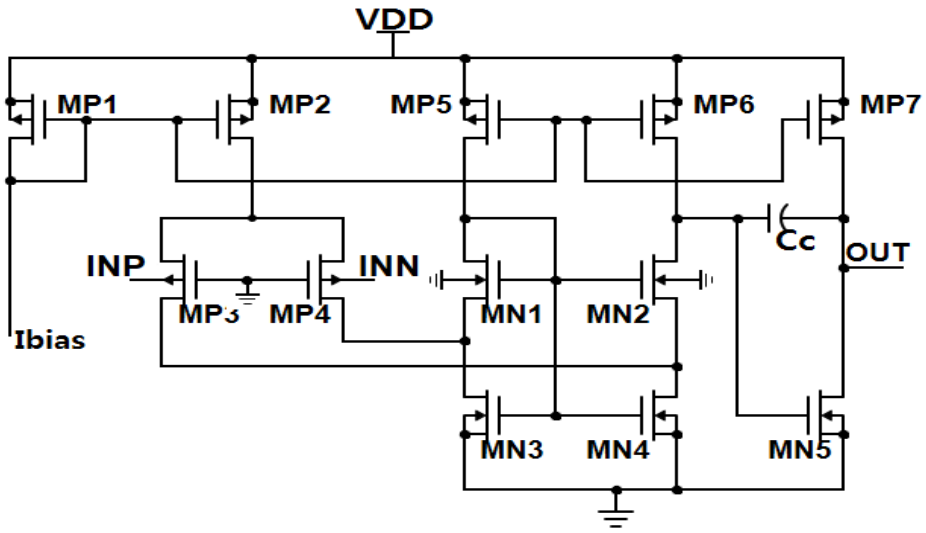

Figure 3: Schematic of the designed op-amp with bulk-driven input stage.

The output voltage variation with temperature when VDD = 0.9 V is shown in Fig. 4. The output reference voltage is 326 mV, and the temperature coefficient is 26.4 ppm/℃ in the temperature range of -30 to 75 ℃. The temperature dependence of the reference voltage for different power supplies is also shown in Fig. 5. The supply voltage dependence of the reference voltage with respect to power supply for three different temperatures is shown in Fig. 6. This plot shows that the minimum power supply voltage for this reference circuit is 0.9 V.

Table 1 compares the proposed circuit with some other low-voltage curvature-compensated reference circuits available in the literature. The designed reference circuit has the lowest power consumption and the lowest operating voltage compared to other curvature-compensated circuits. Therefore, the proposed circuit has a good potential for low-voltage low-power applications. Fig. 7 shows the layout of the designed circuit of which the core area is 0.78 mm x 1.1 mm.

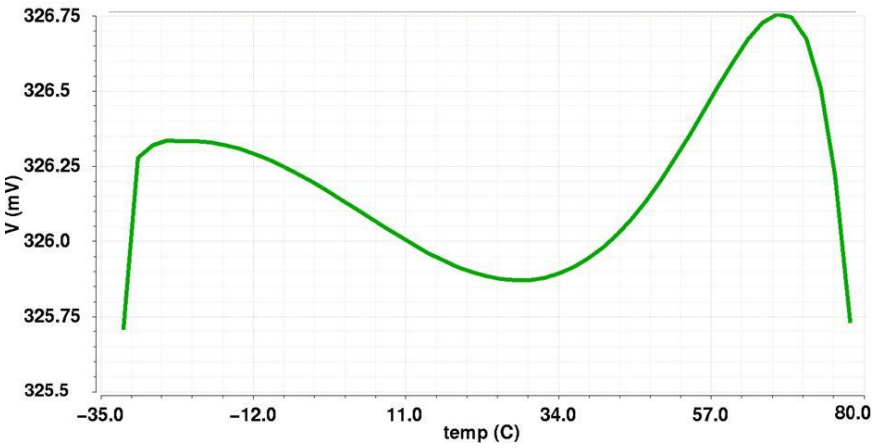

Figure 4: Variation of the output voltage with temperature.

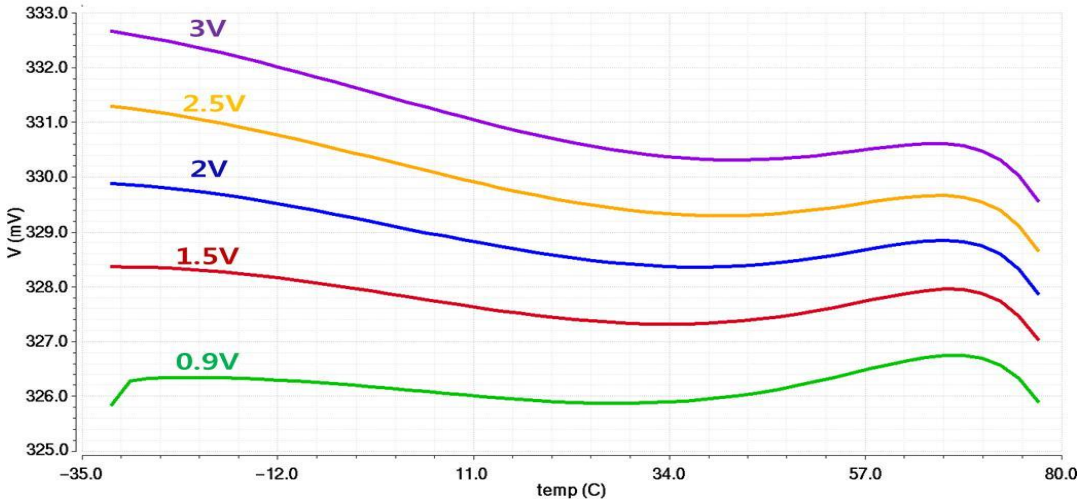

Figure 5: Temperature dependence of the reference voltage with different power supplies.

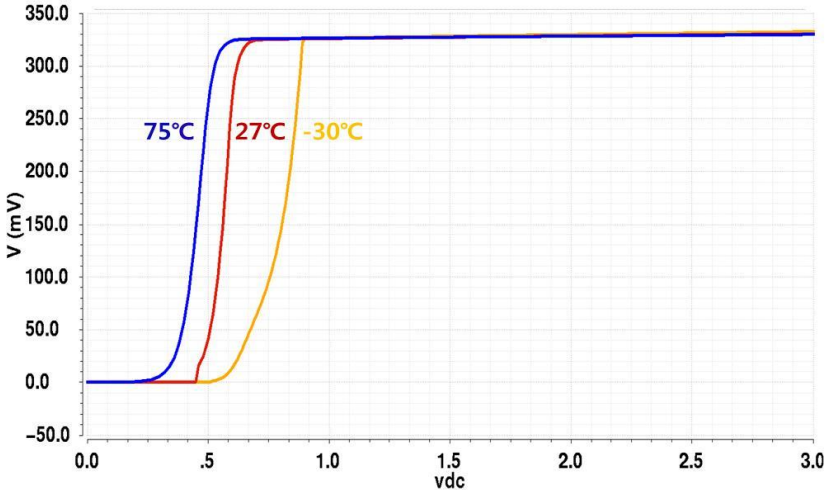

Figure 6: Supply voltage dependence of the reference voltage with different temperatures.

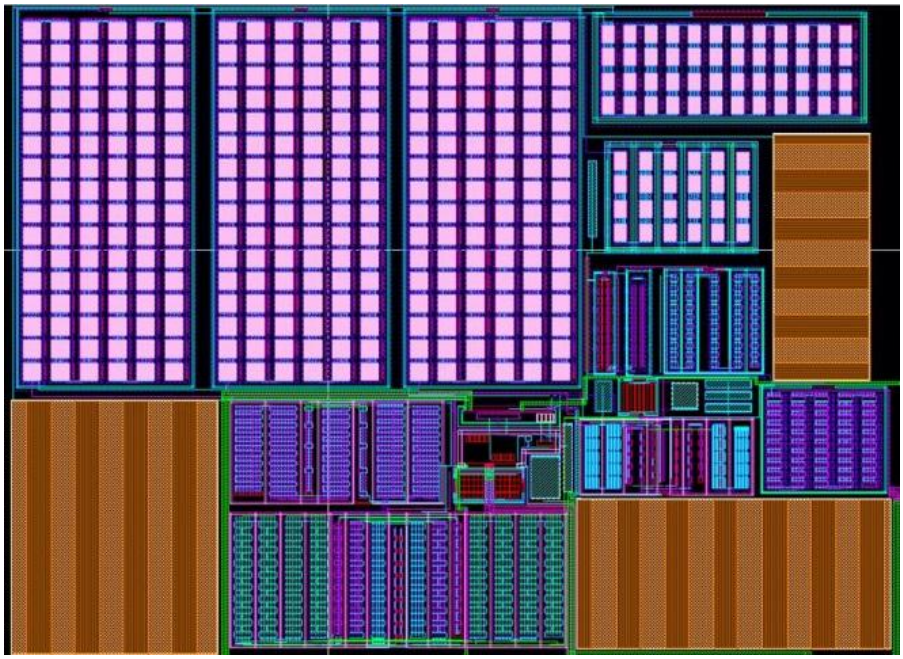

Figure 7: Layout of the designed voltage reference circuit.

Table 1: Comparison between curvature-compensated reference circuits.

	[7]	[12]	[10]	[4]	This work
Process	0.8 µm BiCMOS	0.6 µm CMOS	0.5 µm CMOS	90 nm CMOS	0.35 µm CMOS
VDD_{min} (V)	1	2	1.2	1.15	0.9
V_{REF} (V)	0.54	1.14	0.49	0.72	0.326
Power consumption (µW)	92	46	48	0.58	0.176
VDD sensitivity (%/V)	0.02	0.13	0.24	0.3	0.73
Temp. range (℃)	0 ~ 80	0~100	-40~110	0~100	-30~75
TC (ppm/℃)	7.5	5.3	8.9	43.5	26.4
Area (mm^2)	3	0.057	0.096	0.028	0.86
Year	2001	2003	2011	2015	2016

CONCLUSION

A sub-1V curvature-compensated CMOS voltage reference circuit using subthreshold MOSFETs without BJTs has been presented. The proposed circuit has been designed in a 0.35-µm CMOS technology. Simulation results show that the designed circuit achieves a temperature coefficient of 26.4 ppm/℃ in a range of -30 to 75 ℃ and a line regulation of 0.73 %/V. It consumes only 176 nW from a 0.9 V power supply. The proposed reference circuit has the lowest power consumption and the lowest operating voltage among published curvature-compensated reference circuits which

makes it a good candidate for low-voltage low-power applications.

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