

Design of Dynamic Voltage Restorer For The Mitigation of Voltage Swell / Sag In Distribution Network Using Space Vector Modulation Technique

N.Nirmal^{#1} and S. Mohamed Ghouse^{#2}

PG-Scholar^{#1}, Assistant Professor^{#2},

^{1,2}SEEE, SASTRA University, Thanjavur, Tamil Nadu-613401, India

¹nagarajannirmal@gmail.com, ²ghouseee@eee.sastra.edu

Abstract

Dynamic Voltage Restorer (DVR) is an important power electronic equipments to minimize power quality problems such as voltage sag/swell in power systems. The role of DVR is to supply injection voltage at the transmission line which maintain constant voltage profile across the load. This paper deals with the enhancement of voltage stability in transmission line using DVR. The DVR consists of a three phase multilevel inverter , injection transformer and an energy storage device. The DVR design is based on the implementation of Space Vector Modulation(SVM) technique for a three phase multilevel inverter. The control strategy based on SVM is investigated using MATLAB/SIMULINK. The simulation result shows the effectiveness of the DVR in mitigating voltage swell/sag during wide range of system disturbances.

Keywords: Dynamic Voltage Restorer (DVR), Multi-Level Inverter (MLI), Space Vector Modulation (SVM), Voltage sag/swell.

Introduction

The equipments used in process industries and manufacturing industries are high sensitive devices which cannot work effectively during power system disturbances such as voltage swell /sag , supply harmonics, flicker, impulse transient and frequent interruptions[1]. The problems such as voltage sag & swell may cause distortions sinusoidal waveform of the sources voltage. In order to mitigation such problems various customer oriented power devices are used. In this work Dynamic Voltage Restorer (DVR) is used for improvement of power quality. The power devices categorized as series connected compensated, shunt connected compensated and combination of series and shunt connected compensators[2]. The DVR is a series

connected compensator which used to minimize the power quality related problem such as voltage swell, sag and harmonics in the system voltage.

DVR used in the distribution network is implemented in series with the 3ϕ load in order to inject real and reactive power requirement by the load during voltage sag/swell problems. In this paper Space vector modulation technique is used for the control of DVR. SVM technique implemented on a multi level inverter generate sinusoidal voltage with less harmonic content the performs of DVR in mitigating voltage sag a swell problems under varying system disturbances.

Proposed Model of DVR

The basic schematic of a DVR connected between an AC sources and a 3ϕ load is given in Fig. 1. DVR detects the voltage swell / sag which occurs in transmission system and inject a balance voltage with the help of an injection transformer. This can be done by suitable obese ring or injecting the required active and reactive power to the load. The proposed DVR consist of a multi level inverter energized with help energy storage devices an injection transformer. A multilevel inverter converts the DC voltage fed by energy storage devices to a balanced three phase AC supply. Insulated Gate Bipolar Transistor (IGBT) is used as switching devices in the design of multi level inverter.

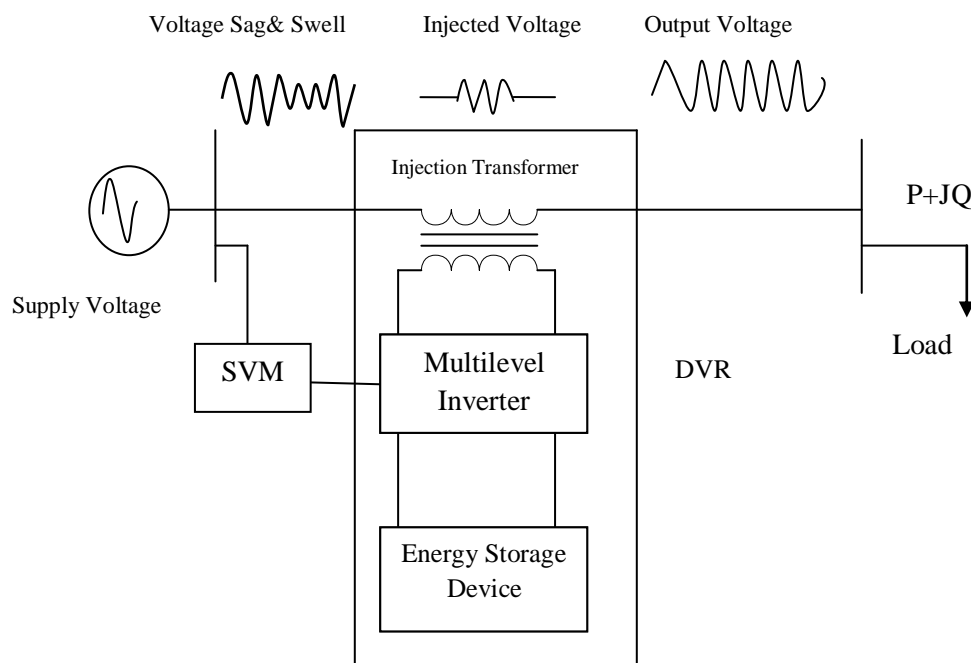


Figure 1: Schematic Diagram For The Grid

The role of the injection / booster transformer is to inject required compensating voltage to maintain constant AC supply across the 3ϕ load. The injection transformer primary is connected with distribution line in series fashion and the secondary

winding is connected to the multilevel inverter it also isolate the DVR circuit from distribution network.

When distribution network voltage is stable that i.e. without any disturbances system the DVR are injecting very small voltage to compensate the device loss but during disturbances voltage sag swell created system and restorer the system to normal state the DVR will inject a controlled three phase Ac supply in series with the Ac system voltage with a particular magnitude in order to maintain in the voltage profile constant across the load.

Equivalent Circuit

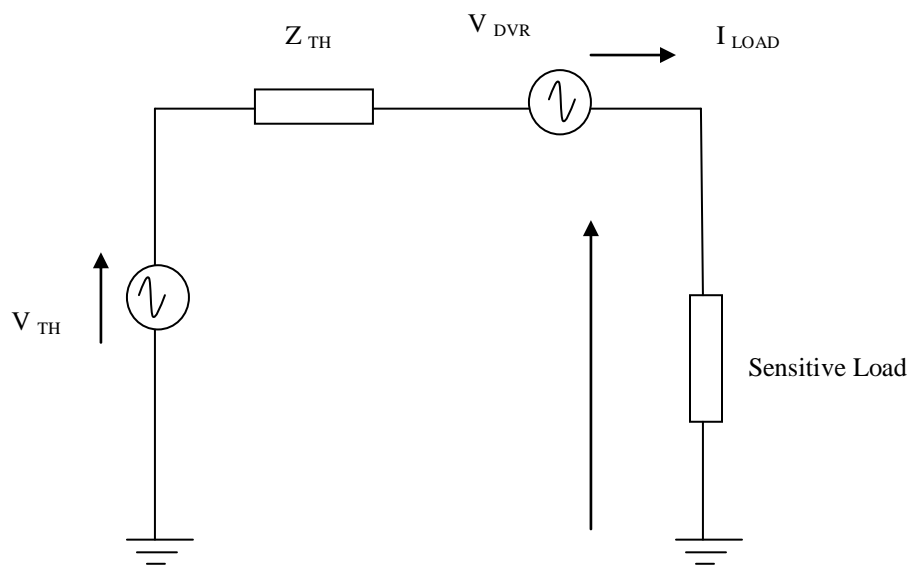


Figure 2: Equivalent circuit of DVR

Fig. 2. shown in Thevenin equivalent circuit of the Dynamic Voltage Restorer(DVR) is designed to inject a compensation voltage V_{DVR} with help of booster transformer in order to maintain the Voltage load V_L . The injected series voltage by the DVR (V_{DVR}) can be expressed as

$$V_{DVR} = V_L + Z_{TH} I_L - V_{TH} \quad (1)$$

Where

V_L - Desired load voltage

Z_{TH} - Thevenin equivalent impedance, I_L - Load current

V_{TH} - Voltage during fault. The expression for the load current is given by

$$I_L = [P_L + jQ_L] / V \quad (2)$$

The power factor angle θ is given by

$$\theta = \tan^{-1} (Q_L / P_L) \quad (3)$$

The apparent power injected by DVR is given by

$$S_{DVR} = V_{DVR} I_L^* \quad (4)$$

From the above equation, it is clear that when the injected voltage V_{DVR} is in quadrature with the I_L , DVR generate the reactive power. Other phase relationship between V_{DVR} and I_L requires active power injection which may be supplied by battery or other storage devices.

Proposed Control Unit of DVR

The objective of the proposed work is to develop a control technique using Space Vector Modulation technique SVM technique can be effectively implemented with the help of advanced digital processor. SVM technique for switching of power devices used in three phase power inverter many research work report that inverter design using SVM technique generate lesser harmonics distortion and compare to conventional sinusoidal modulation technique. SVM technique much advances computational technique among all PWM technique a typical a 3 ϕ PWM shown in Fig.3. There are totally eight Space Vector switch state and corresponding space voltage vector shown in Fig.4.

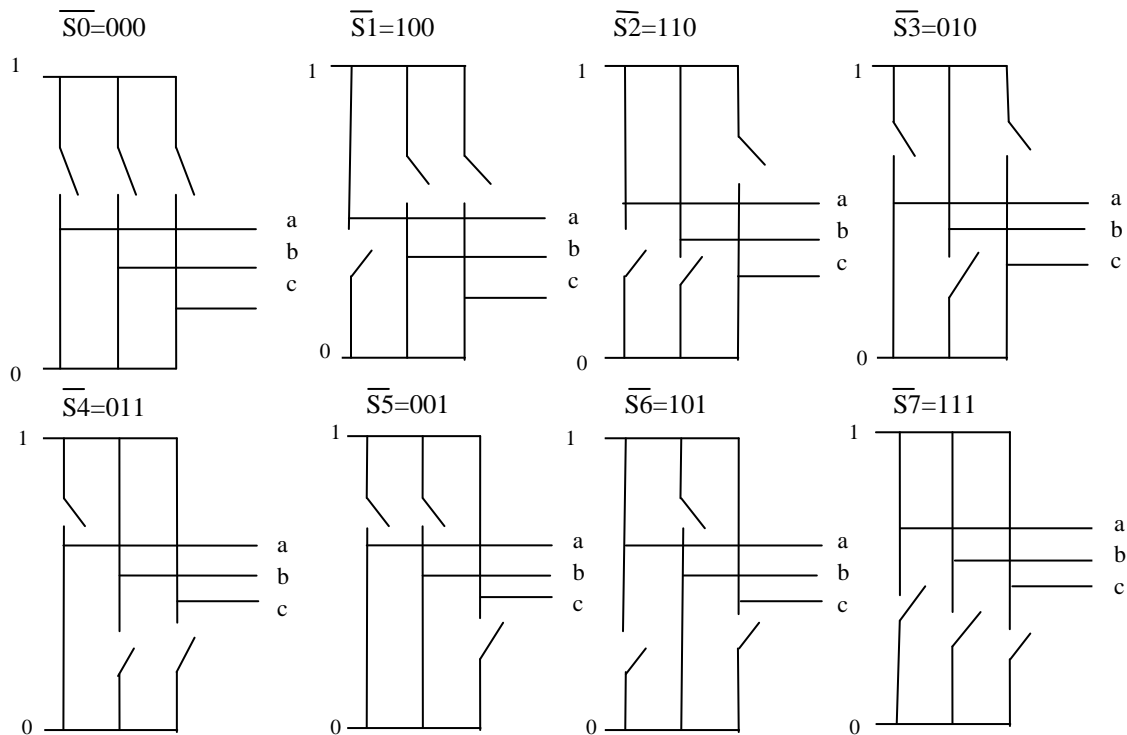


Figure 3: Space Vector Eight Switching State

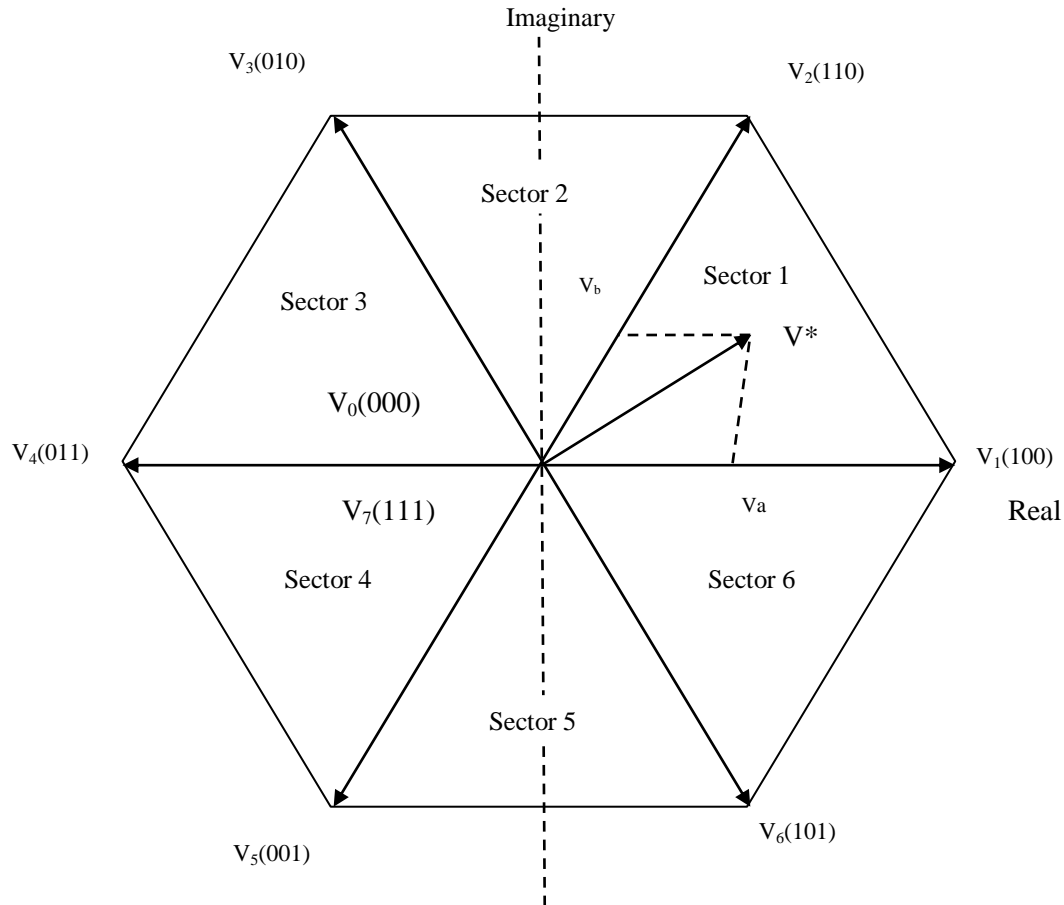


Figure 4: Voltage Space Vector

There are totally eight voltage vectors $V_0=[000]$ to $V_7=[111]$ which corresponds to the switch states S_0 to S_7 . For the vectors V_1 to V_6 the length considered are unity and lengths of V_0 and V_7 are zero. The voltage vector space can be divided into 6 sectors. The operation rules are considered in the given vector space is given by.

$$\overline{V}_1 = -\overline{V}_4; \overline{V}_2 = -\overline{V}_5; \overline{V}_3 = -\overline{V}_6; \overline{V}_1 + \overline{V}_3 + \overline{V}_5 = 0$$

Output voltage vector corresponding it's on sample interval is given by

$$\overline{V}(t) = \frac{t_0}{T_s} \overline{V}_0 + \frac{t_1}{T_s} \overline{V}_1 + \dots + \frac{t_7}{T_s} \overline{V}_7$$

Multilevel Inverter Topology

Multilevel inverter has emerged recently in the area of high power medium voltage applications due to their improved output wave form and modular structure. The basic

two or three levels power inverter cannot eliminate the unwanted harmonics completely. In the proposed inverter terminals $2N+1$ phase voltage levels are considered where N is the number of DC link voltages. A separate DC link capacitor is provided for each cell and the voltage across the capacitor is different for different cells. The total number of DC link capacitors depends upon the number of phase voltages. The power circuit of the inverter is shown in Fig. 05.

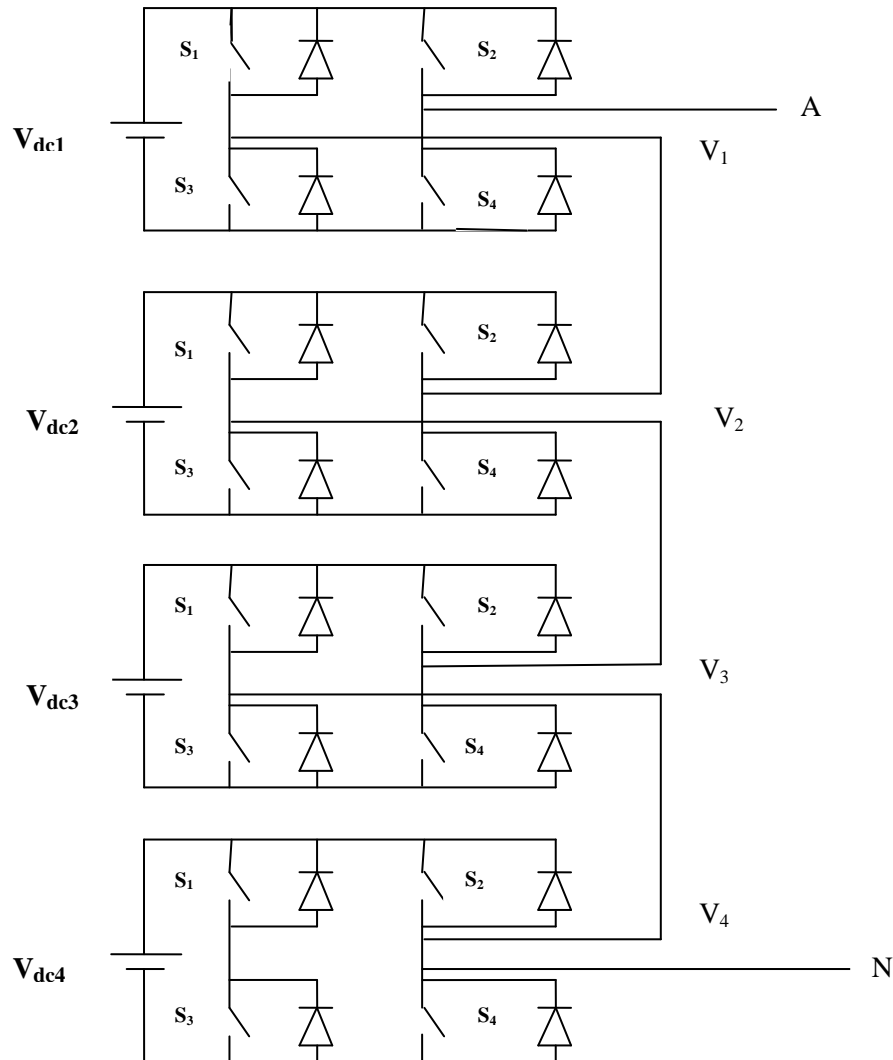


Figure 5: Seven Level Multi Inverter

The cascaded H-bridges multilevel inverter configuration can be achieved by connecting multiple H-bridge inverters in series. This topology develops pure sinusoidal voltages with low dv/dt . The size of the filter used can be reduced because of the low THD output waveform. The resulting phase voltage is synthesized by adding the voltage generated by different cells. The resultant output is a staircase waveform which is nearly sinusoidal. In order to decrease the switching losses and

improve system efficiency the switching frequency of the H bridge cell its limited to 1.3KHz.

Simulation Model and Results

The system consist of three phase supply ,series injection transformer and a three phase sensitive load. This system is modeled with help MATLAB/Simulink environment. A 10KVA 0.8p.f linear load is consider. The power system simulation model first studied without the implementation of DVR as shown Fig.06.

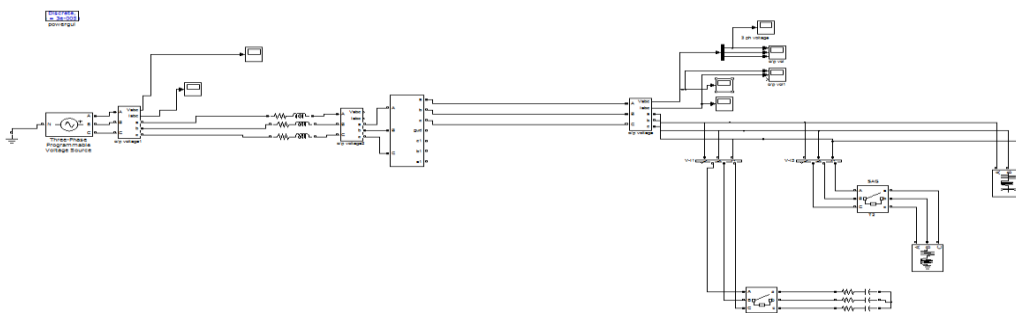


Figure 6: Simulation Model of Grid Without Connected DVR

The proposed control algorithm using SVM for DVR is modeled using MATLAB/Simulink is show in Fig.07. The SVM controller is used to generate gate signal for the IGBTs of the multilevel inverter. The performance of the DVR and different fault conditions are studied.

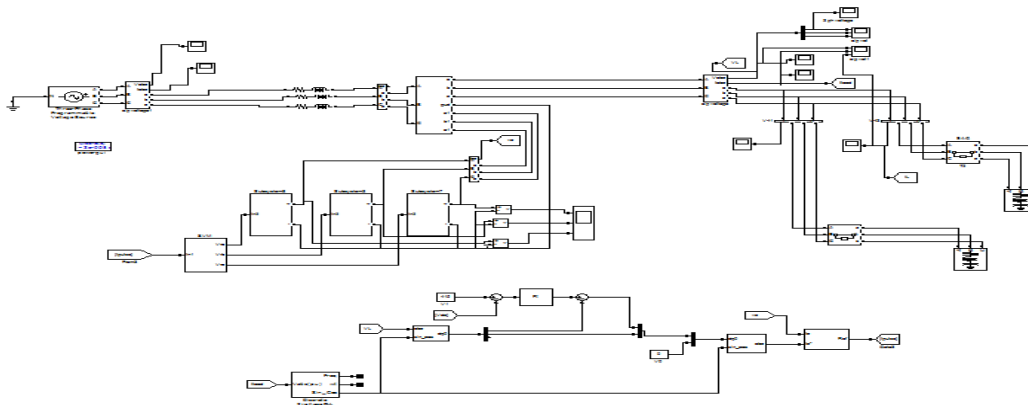


Figure 7: Simulation model of grid with connected DVR

Simulation Results and Discussions

Supply voltage disturbances such as voltage sag and swell created by properly switching ON and OFF the sensitive load. Fig.08 shows the voltage sag created at

0.1sec and 0.3sec respectively. A voltage sag of magnitude 80V from the peak observed without the implementation of DVR.

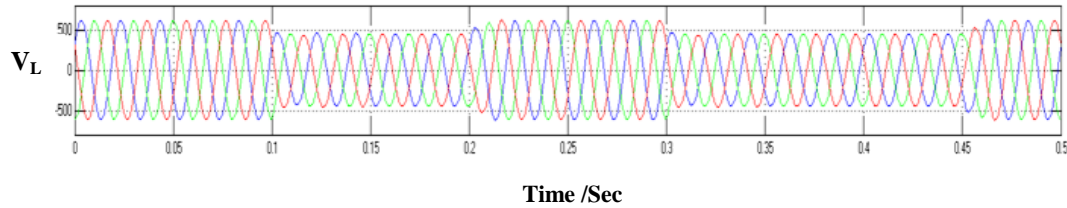


Figure 8: Simulation Output of Sag Voltage

Fig.09 shows the swell creation in the system voltage for the same time duration. A voltage swell of 110V from the peak is observed for the system with out DVR.

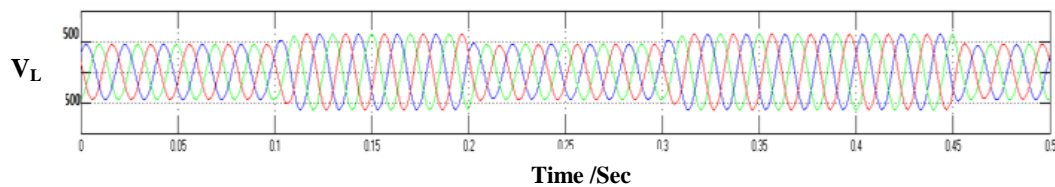


Figure 9: Simulation Output of Swell Voltage

The proposed DVR scheme is implemented and performances are analyzed for the same sag and swell condition in the distribution network. The sag and swell voltages are sensed and proper control signal are generated using SVM controller. The proper injection voltage is developed using DVR an injected in series with the distribution line using injection transformer. The output of the DVR is show in Fig. 10.

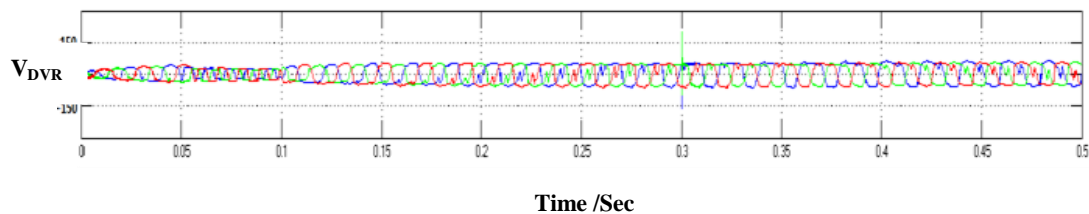


Figure 10: Simulation output DVR Voltage

The references function of the regular SVM is shown in Fig. 11. It represents the duty ration each inverter leg to sampling period for given switch. It is a mathematical function with variation between 0 and 1.

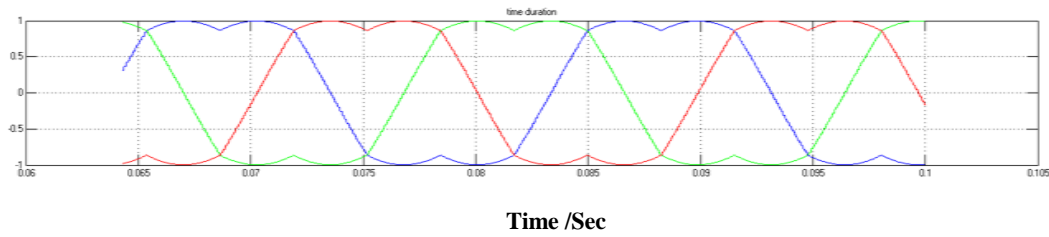


Figure 11: Simulation output SVM

The output of seven multilevel inverter is shown in Fig. 12.

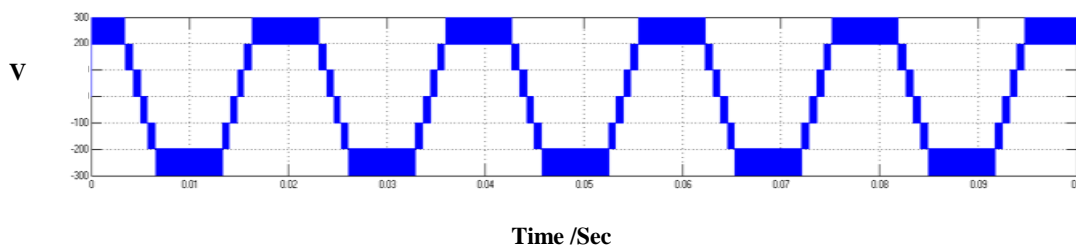


Figure 12: Simulation Output For Seven Level Inverter

The responses of DVR during voltage sag and swell is analyzed by observing the line voltage at the 3 ϕ load side. During both voltage sag and voltage swell condition the proposed DVR effectively restore the system voltages and hence improve the power quality. The output waveform at the load side with DVR is shown in Fig.13&14.

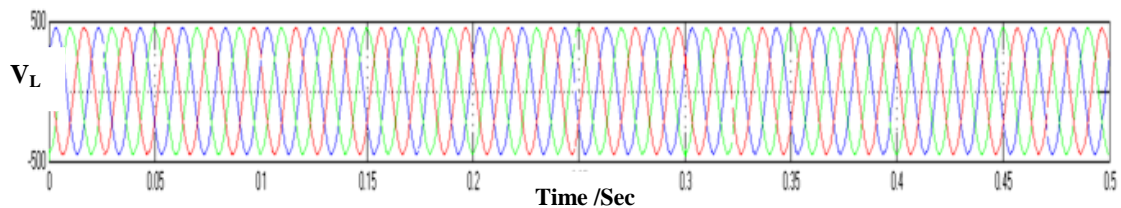


Figure 13: Simulation Output of Compensated Sag Voltage

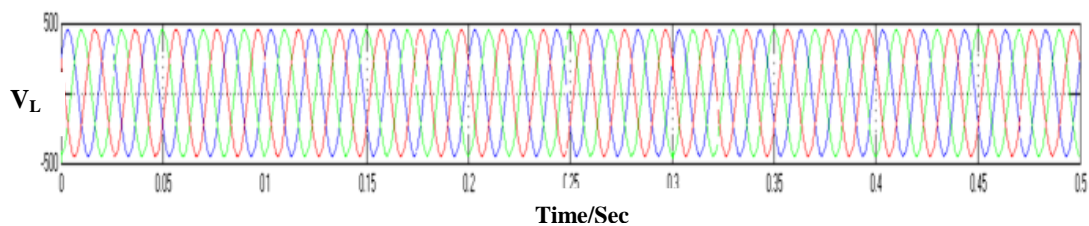


Figure 14: Simulation output of compensated Swell Voltage

By proper injection of voltage by DVR during voltage sag and swell with a particular phase and magnitude restore the system voltage. From the result clear that the swelled and sagged load terminal voltage is restore thus maintaining a balanced constant voltage across the sensitive load.

Fig. 15&16 THD shows the during FFT analysis with and without DVR . It is observed that the THD (Total Harmonics Distortion) value of the system is reduced to a great extent by the implementation of DVR. The THD for system without DVR is about 5.35% and for the system with DVR the value of THD is around 0.2%.

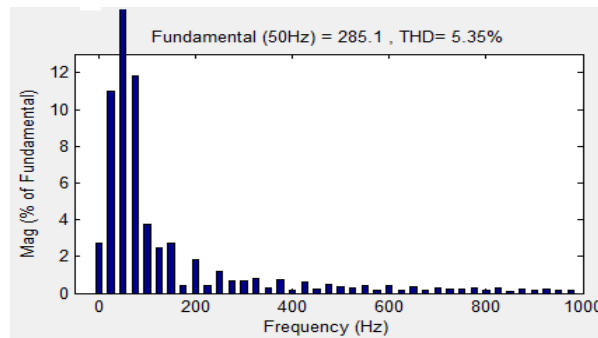


Figure 15: Without DVR for THD

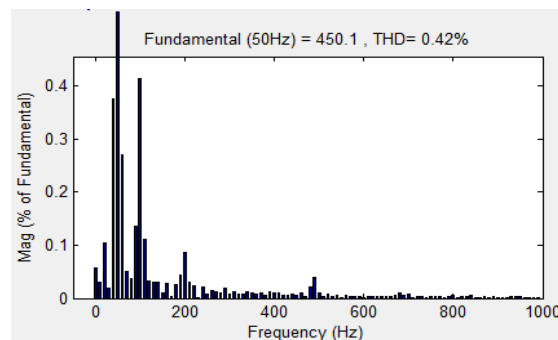


Figure 16: With DVR for THD

Conclusion

This work deals with the role of Dynamic Voltage Restorer in mitigating power quality related problems such as voltage swell/ sag. Space vector Modulation based DVR is proposed and simulation modeling is carried out. System disturbance is simulated by creating voltage swell / sag in the load voltage side. The load voltage wave form with and without DVR is analyzed during disturbances. The results of the simulation work clearly demonstrates the effectiveness of the DVR implemented using SVM technique. The improvement in the power quality of the system is verified by THD measurements. The proposed system with DVR capable of restore ring load voltage during disturbances with reduced harmonic distortions.

Acknowledgment

The authors of this work greatly indebted to Prof. R.Sethuraman, Vice-Chancellor, SASTRA University for the unwavering support and motivation extended during the course of the project work. The authors are also grateful for the motivation and support extended by Dr. B. Viswanathan, Dean/SEEE, SASTRA University.

Reference

- [1] M.H.J Bollen "Understanding Power Quality problems : Voltage sag and Interruption " New York IEEE Press ,1999.
- [2] A. Ghosh and G. Ledwich, power quality Enhancement Using Custom Power Devices. London ,U.K.: Kluwer, 2002.
- [3] V.Jayalakshmi "Implementation of Discrete PWM Control Scheme on Dynamic Voltage Restorer for the Mitigation of Voltage Sag" 2013 978-1-4673-6150-7/13/\$31.00 ©2013IEEE Transactions on Industry Applications, Vol. 50, No. 2, March/April 2014
- [4] S.K. Tiwari and Gupta. " Effect of Load Power Factor on DC Storage Capacity of DVR For Power Quality Improvement in Power Systems" 2012 IEEE International Conference on Power Electronics, Drives and Energy System December 16-19, 2012, Bangalore, India 2012
- [5] P. Ananthababu, "Performances of Dynamic Voltage Restorer (DVR) Against Voltage Sag and Swell Using Space Vector PWM Technique" Article Code: pqa_3266 2009.
- [6] S. Galeshi, H. Iman-Eini, "Dynamic Voltage Restorer Using Multilevel Cascaded Inverter and Capacitor as Energy Sources". IEEE Transactions on Power Delivery, Vol. 14, No. 3, July 2012.
- [7] N. SwagataSinghaRoy "Application of Dynamic Voltage Restorer in Electrical Distribution System for Voltage Sag Compensation". The International Journal of Engineering and Science (IJES).
- [8] M.David Solomon George and R. Baiju."Space Vector Based Random Pulse Width Modulation Scheme for a 3-level Inverter in Open-end Winding Induction Motor Configuration"978-1-4673-0158-9/12/\$31.00 ©2012 IEEE.
- [9] N. RosliOmar and A Rahim"Implementation and Control of a Dynamic Voltage Restorer Using Space Vector Pulse Width Modulation (SVPWM) for Voltage Sag Mitigation", the International Conferences paper 2012.
- [10] A. Ghosh and G. Ledwich, "Compensation of distribution system voltage using DVR," IEEE Trans. Power Del., vol. 17, no. 4, pp. 1030–1036, Oct. 2002.
- [11] A. Ghosh and A. Joshi, "A new algorithm for the generation of reference voltages of a DVR using the method of instantaneous symmetrical components," IEEE Power Eng. Rev., vol. 22, no. 1, pp. 63–65, Jan. 2002.

- [12] J. G. Nielsen and F. Blaabjerg, "A detailed comparison of system topologies for dynamic voltage restorers," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1272–1280, Sep./Oct. 2005.
- [13] D. M. Vilathgamuwa, H. M. Wijekoon, and S.S. Choi, "A novel technique to Compensate voltage sags in multiline distribution system—The interline dynamic voltage restorer," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1603–1611, Oct. 2006.
- [14] P. Singh, B. Kothari, S. Jayaprakash "Control of Reduced -Rating Dynamic Voltage Restorer with a Battery Energy Storage System", 2014.IEEE Transactions on Industry Applications, Vol. 50, No. 2, March/April 2014.