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Read/Write Stability Improvement Of Ultralow Voltage CAM Using Schmitt Trigger

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Abstract

In this paper, we proposed a differential sensing Schmitt trigger based Content addressable memory (CAM) for ultra low voltage. The Schmitt trigger is one which give the better stability for both read/write operation. The Schmitt trigger is used because of their feedback mechanism leakage power is minimized, process variation tolerance. It is fast, high performance, delay is reduced. Due to scaling we face challenge in leakage of power as a main concern. The comparison of different ST based 6T CAM and ST based 8T is designed by varying the parameter in 250nm technology.

Index terms:- Low voltage CAM, Schmitt trigger(ST), Matching lines, Stability, Power consumption, TANNER EDA.

I. INTRODUCTION

The electronic memory devices store and retrieve data by specific memory location. As a result, the path become limiting factor on fast access only. So the time required to store data in the memory is reduced by specifying the address directly. A memory that access in such manner is called content Addressable memory(CAM). To achieve some function such as data searching, the data comparison of CAM is implemented in parallel operation structure. However due to parallel process characteristics, power consumption is an important problem in designing the CAM circuitry. The content addressable memory is one which compare an input word to all the content of the memory and return the address of matching location in a single clock cycle.

A CAM architecture is shown in Fig.1.This figure shows a CAM which consist of 4 words, each word containing 3 bits arranged horizontally to it. There is match line corresponding to word line. Feeding in to match line sensing amplifiers (MLSAs), and there is a differential search line corresponding to each bit line of search line. CAM search operation is begin by loading the search data word in the

search data register by precharging all match line high, putting all temporarily in match state.

Next, the search line drivers broadcast the search word on the differential search lines, and Cam core cell compare its stored bit with the corresponding search lines. Match line on which the bits are match remain in the precharged high state. Match line some bits are mismatches or miss that are discharge to ground. The MLSA detect that weather match line is in match or mismatch condition. Finally, the encoder maps the match line on the matching location to its encoder address.

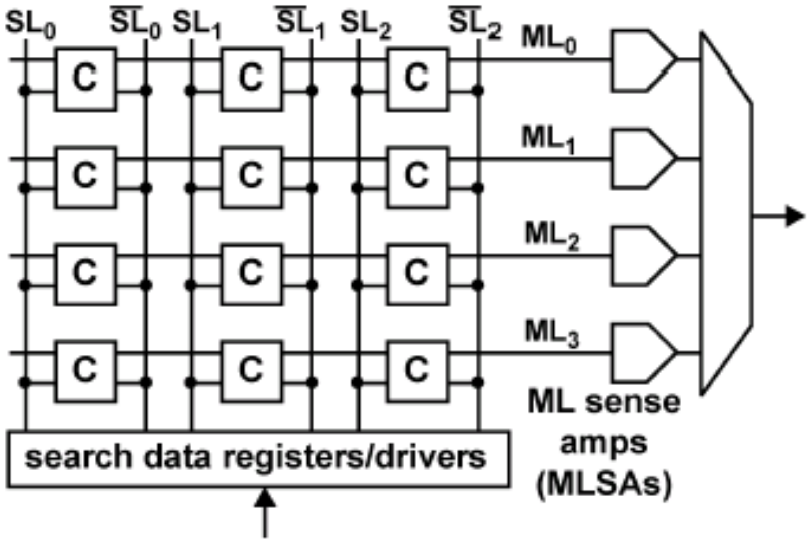

Fig 1.Block diagram of CAM Architecture

Whenever the search data matches a word the match line remains the high and discharges to ground during mismatch. The major portion of the power is consumed during the searching operation where the search line is charged and discharge during the precharge and evaluation phase respectively. During this process the match line also consume power in charging and discharging. In this process the stability is also not maintained properly. To maintain the stability and power consumption the Schmitt trigger concept is implemented. The Schmitt trigger is one which is applied in various type to obtain the better stability and power consumption. The major drawback of cam is that it need more power and it has large delay. So, that Schmitt trigger is implemented to reduced the power and delay.

II. SCHMITT TRIGGER (ST*)*

In order to resolve the conflicting problem in read versus write design requirements in the conventional 6T bitcell, we apply Schmitt trigger. The Schmitt trigger principle is one which is made up of cross coupled inverter pair. A Schmitt Trigger is used to modulate the switching threshold of an inverter based on the direct proposed on of the

input transition. In the existing ST SRAM bitcells, the feedback mechanism is used only in the pull-down path, as shown in the fig. 2.During 0->1 input transition, the feedback transition (NF) tries to preserve the logic "1" at output (Vout) node by raising the source voltage of pull-down nMOS (N1).Since it has a read failure it is initiated by 0->1 in the input transition storing logic "1,".This results in higher switching threshold of the inverter with very sharp transfer characteristics.

In 1->0 input transitions, the feedback mechanism is not present.This results in smooth transfer characteristics for write operation. The Schmitt trigger is used to improve the both read and write stability. In the existing they are of two types ST-1 based SRAM and ST-2 based SRAM.

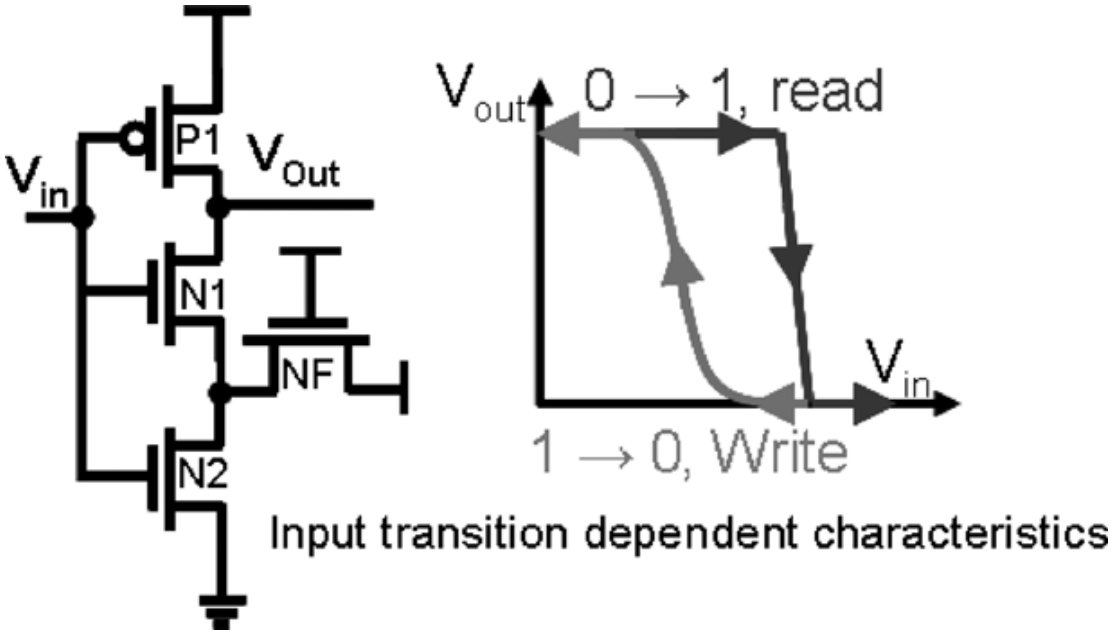

Fig 2. Schmitt trigger (ST) schematics

III. EXISTING ST-2 BITCELL

In Fig.3 shows the schematics of the ST-2 bitcell utilizing differential sensing with 10T, two word-lines (WL/WWL), and two bitlines (BL/BR). The WL signal is assigned during read as well as the write operation, while WWL signal is assign during the write operation. During the hold-mode, both WL and WWL are OFF. In the ST-2 bitcell, feedback is provided by separate control signal (WL) while in the ST-1, The feedback is provided by the internal nodes. In the ST-1 bitcell, the feedback mechanism is effective as well as the storage node voltage is maintained. Once the storage nodes start transferring from one state to another state, the feedback mechanism is lost. To improve the feedback mechanism, the separate control signal WL is used for achieving stronger feedback. Detailed operation of ST-2 bitcell is explained in the previous work[6].

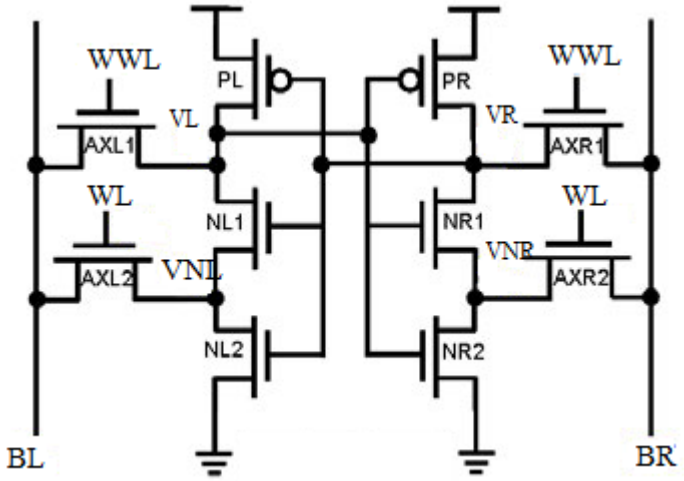

Fig.3.Schmitt trigger (ST-2) bitcell Schematics

IV. CAM AND RAM CELL

The RAM has two major operation one Read and second is Write. The RAM is one in which the user supplies the memory address and data stored in that address is returns. A CAM has three major operation they are Read, Write and Search. In which the user supplies the data word Cam will go through it entire memory. If the data word is found cam will return it address where the data is stored. There are two types of CAM they are Binary CAM(BCAM) and Ternary CAM(TCAM). The BCAM is one which store 0's and 1's. The TCAM stores 0's 1's and don't care. CAM is used in various applications such as IP Packets in network router, data base engine, Artificial neural networks, data compression hardware, Broad ATM communication system, etc..,

A.CAM cell structure and operation

The CAM cell is based on the static memory cell. The static memory cell is one which is made up of cross coupled inverters. The data will be stored in that cross coupled inverters. In this process two nMOS transistors are used they are called as access transistor. The access transistor is one which is controlled by using a wordline(WL). This is used in CAM cell to write the values. Then, in this process the four additional transistors are used. Which are used for matching process. The CAM is one which is same as SRAM(Static Random Access Memory). It is made up of 6transistors. But, the major difference in CAM is matching operation. So, the CAM can perform Read, Write and Matching operation.

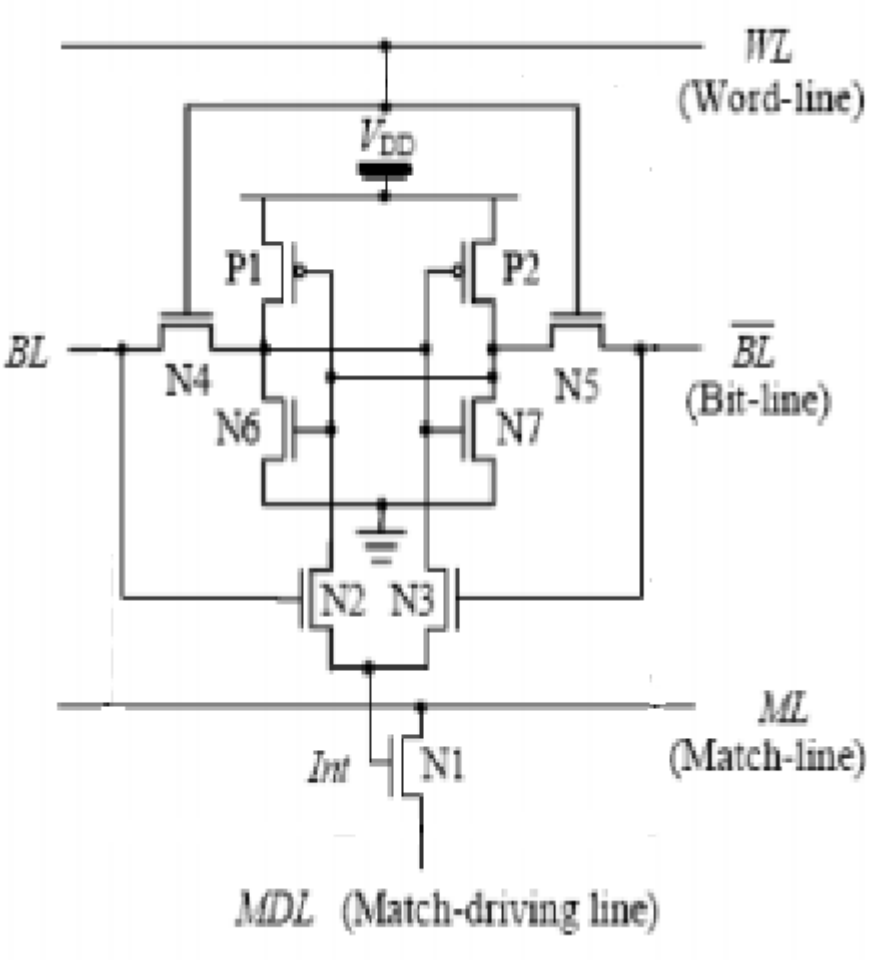

Fig.4.Block diagram of CAM cell

B. CAM Operation

In CAM cell some operation are performed they are, Stand by, Read, Write and Matching.

i. STAND BY:-

Standby is a process in which the Word line is not assign in the beginning. The access transistor N4&N5 is also disconnected from the cross coupled inverter. The cross coupled inverter P1, N2-P2, N3 will continue to reinforce the value as long as they are disconnected from the outside.

ii. READ:-

In Read operation consider, the data stored in Q is 1. The Read Precharging the both bit line by logic 1. The Read cycle starts, at the same time assign word line (WL) also as 1. So, the access transistors are enable. The next will be start when the value from Q is transferred to the bit line. The value in the bitline precharge and discharge N4

and P1 by the logic 0. On the other side BL is connected to P2 and N3 are pull the BL towards the VDD by a logic 1.If the content of the memory is 0. The same process will be performed but in the opposite direction.

iii. WRITE:-

The Write operation is one which is start by applying the value to the bitline. So, the bit line we can apply either 0 or 1 . It is same as a reset pulse to latch. If we give 1 in BL at Qbar we get 0. Similar, if we give 0 in BL bar in Q we get 1. But, the advantage in that is over write will not occur because of using Schmitt trigger in it.

iv. MATCH:-

The matching process is one it will be begin by precharging the nMOS by using VDD. If the data given to the match line matches the Q or QBAR there will be output. Otherwise, it will connect to ground.

V. PROPOSED SCHMITT TRIGGER (ST) BASED CAM

Fig.5. is the proposed Schmitt trigger based CAM. The circuit is made by using SRAM, Schmitt Trigger alone with matching transistor. In this process two word line transistor are used (WL/WWL), 2 bit line (BL/BR).The WL is assign during both the operation Read & Write. But, the WL is assign during the write operation alone.In this the feedback signal is provided by the additional transistor WL in ST-2.

In this three operation are performed read, Write and match.

During, the read operation q will be storing ‘0’ and qbar will be storing ‘1’.In that time WL will be turned ON. But, WWL is turned OFF. The voltage in the Q rise from the ground. So, no current flow through WWL transistor .For the inverter storing ‘1’ is provided by WWL access transistor. Comparing to normal CAM the ST-2 CAM improve the Read operation. In this process the bit line pre-charge the bit line. So, the value stored in the Q is transferred to bit line. The bitline charge and discharge the AXL1 and PL by logic ‘0’. On the other hand BL is connected to PR and AXR1are pull the VDD towards the logic1. If the content 0 in memory it will perform in opposite direction.

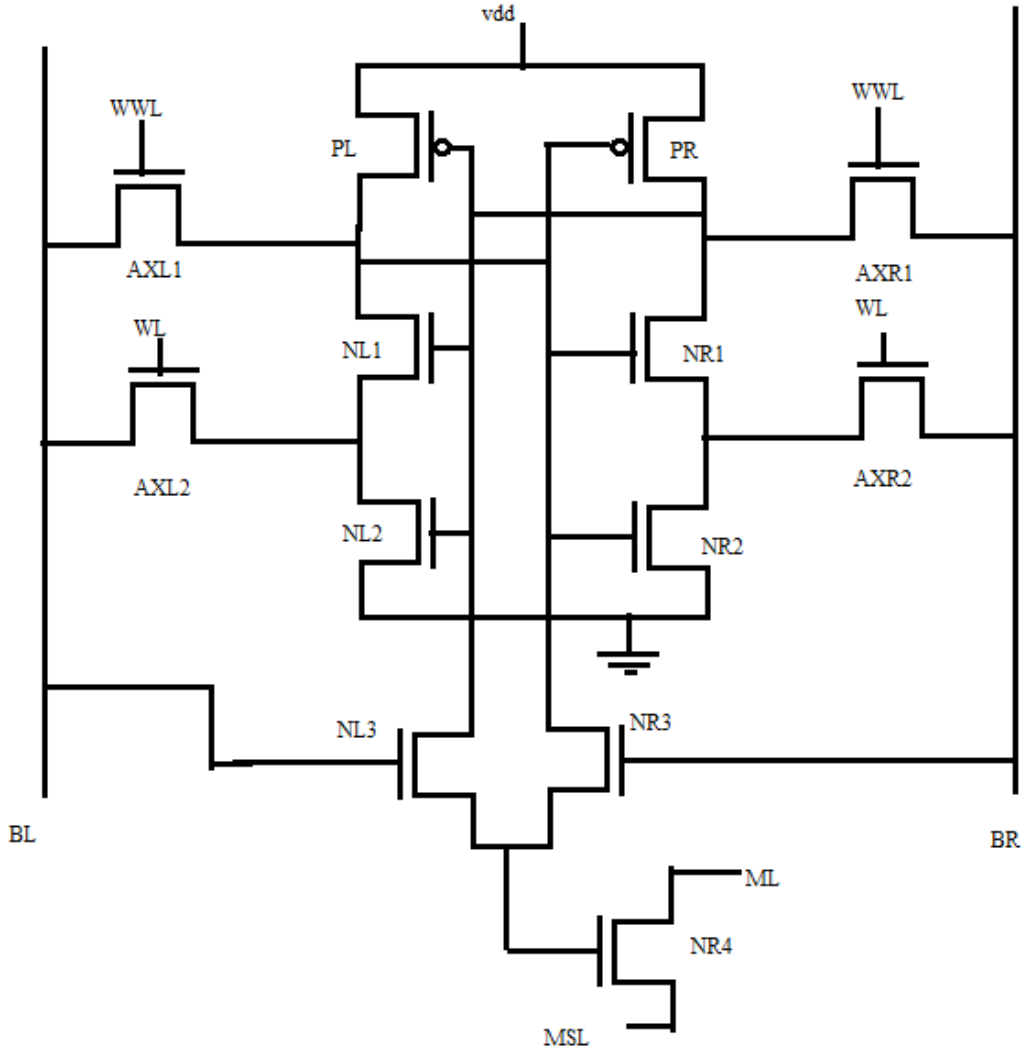

Fig5.Schmitt Trigger-2 Based CAM

During the Write operation, we assign that Q as 0and Qbar as 1by applying value to the bit line it may be either 0 or 1, as same as latch reset pulse. But, in this both the WL & WWL are turned ON. In this we have discharge in right hand side due to AXR2.But, we have stronger pull path in right hand side. By using this ST-2 the stability of the cell is improved.

During matching operation the 3 additional nMOS transistor are used. In this two transistor are connected to BL and BLbar. The output of that is connected to another transistor. The input given to that transistor is ML and MSL. If the input given to the MSL mismatches the data stored in CAM cell is connected to ground otherwise, the input find the match the address in which the data present that address will be displayed.

VI. SIMULATION RESULT AND ANALYSIS

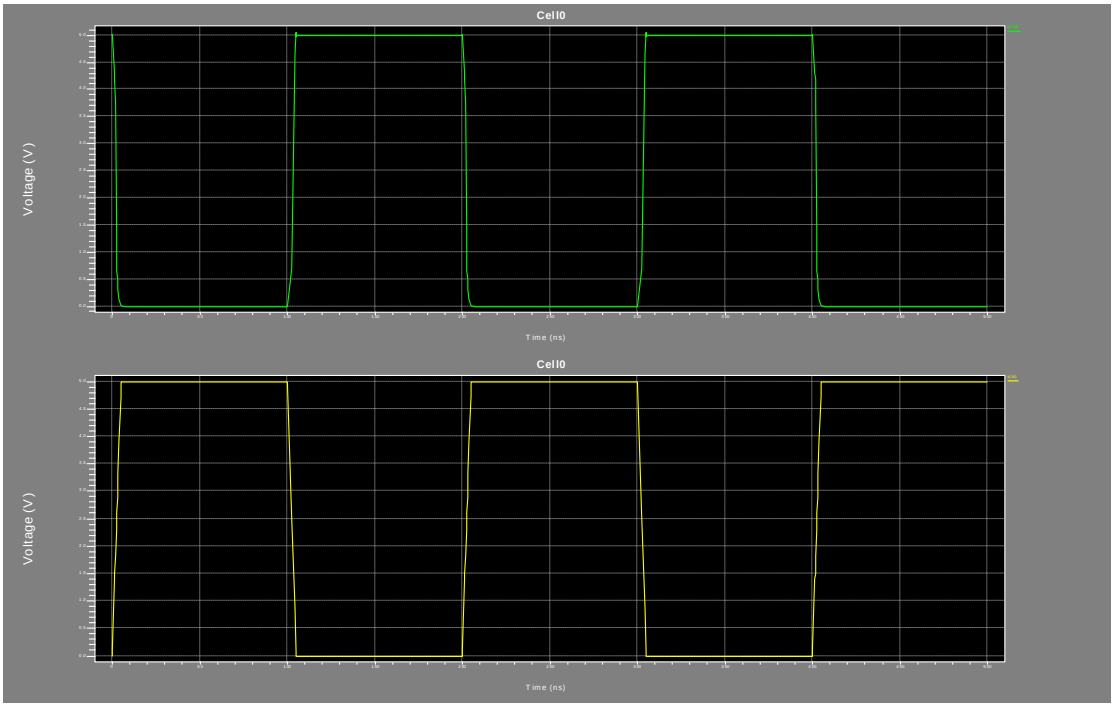

Fig.6 Waveform of Schmitt trigger in W-Edit

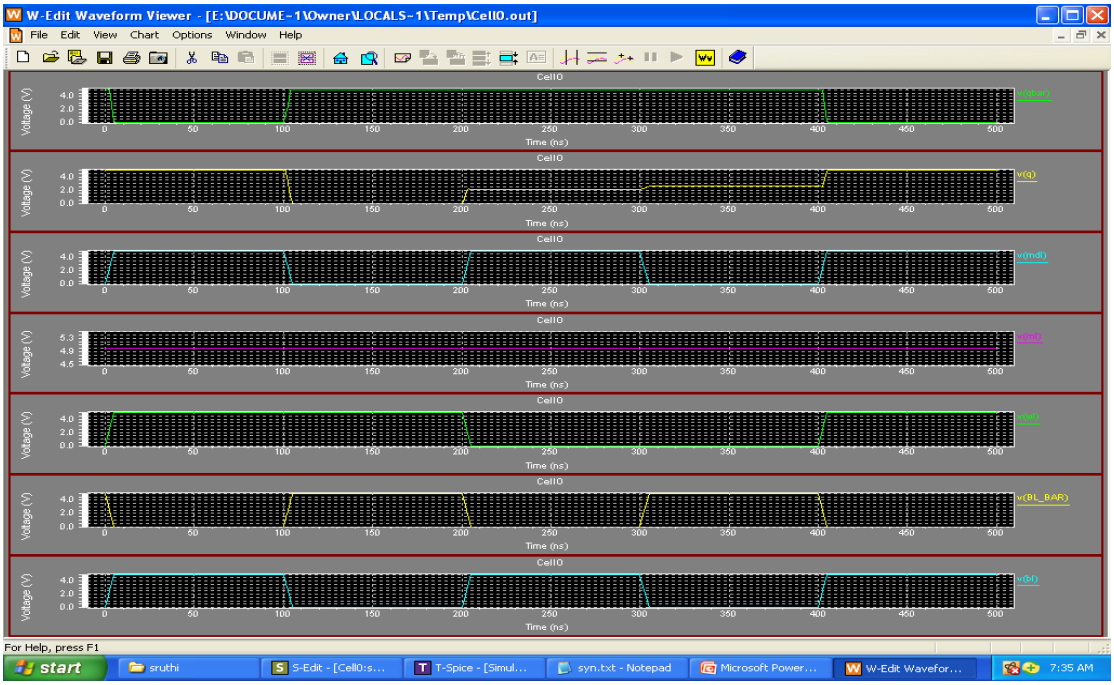

Fig.7 Waveform of CAM in W-Edit

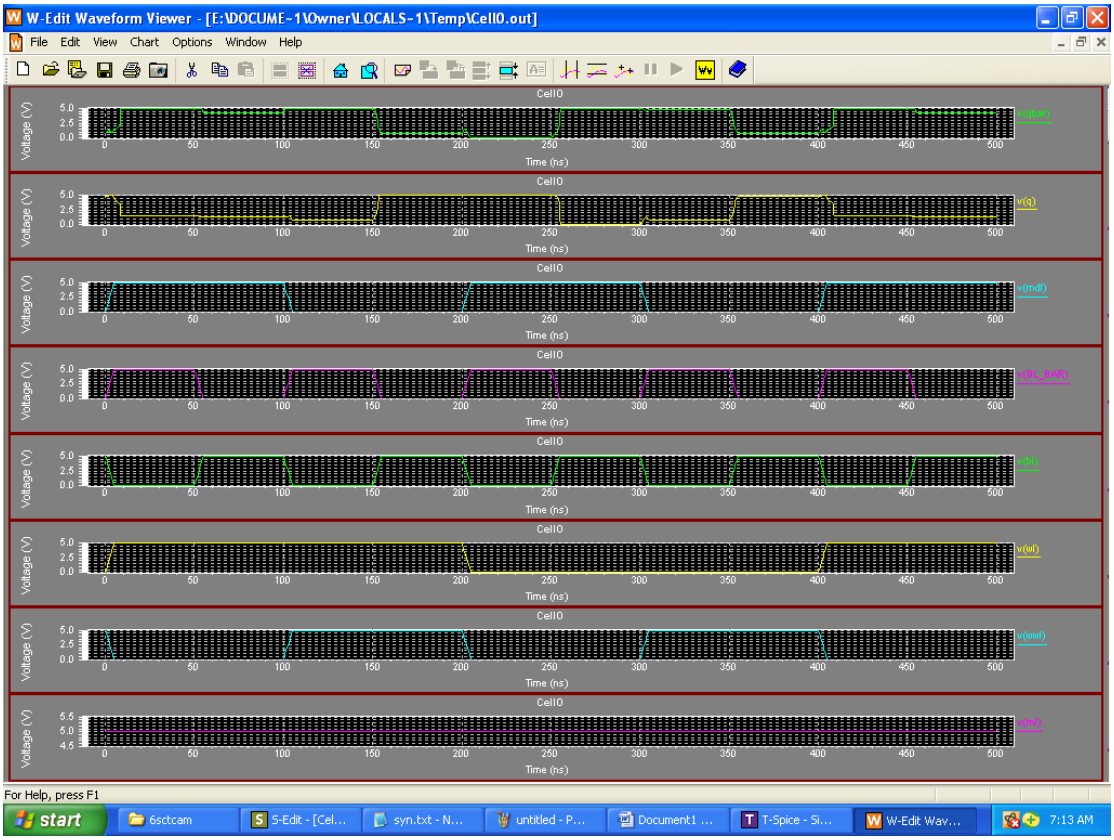

Fig.8 Waveform of ST-2 based CAM W-Edit

TABLE 1.1 Comparison of power dissipation and delay

TYPE	POWERDISSIPATON	DELAY
ST-SRAM	7.7mW	9.86e-9
CAM	6.6mW	9.85e-9
ST-CAM	5.9mW	9.81e-9

VII. CONCLUSION AND FUTURE WORK

In this paper, we have design Schmitt trigger based CAM to improve the stability and reduce the power consumed by it. By modify the architecture in 65nm technology. In future by using this Schmitt trigger concept in NOR, XOR CAM CELL can be designed.

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