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Design Of Level Shifter Using Dual Cascode Voltage Switch For Low Power Application

Priya.P. A[1] , Mohammad Abbas.A[2], Kuppusamy.P.G[3]

PG scholar[1],Assistant Professor[2´3],
Vel Tech Multi Tech Dr.Rangarajan Dr.Sakunthala Engineering College.

ABSTRACT

In this paper, a new ratioed logic style, Dual Cascode Voltage Switch Logic(DCVSL) is presented for high performance and low power VLSI.It feature a built-in short circuit current reduction which increase speed and reduce the power consumption . Level Shifter allow for effective interfacing between voltage domain supplied by different voltage level.The level shifter makeas use of multi threshold design technique thereby providing give more design flexibility, especially in low power system. In this proposed design, level shifter is used for different circuit (i.e) resistor, diode, voltage level shifter and enable/disable feature, allowing for power saving when the level shifter is idle. The level shifter using DCVS has been designed in 180nm CMOS technology using cadence virtuoso.

KEYWORDS: Level Shifter, cascade voltage switch logic, ratioed logic, threshold voltage, leakage current, power consumption.

I.INTRODUCTION

Level conversion has always been an issue for system that need to deal with two or more power domain. This problem is more serves in sub-threshold circuits. Since the drive strength of the devices are mostly limited to sub-threshold operation and have a corresponding exponential dependency on voltage, several intermediate voltage are typically required to up-convert to I/O voltage level[1]. But in this work, enable/disable of transistor has been done only for Nmos. It has the advantage of low static power consumption and small propagation delay due to the cross coupled latch structure. The drawback is that converting from ultra-low input voltage require large transistor [2-7].Single supply diode voltage-limited buffer and half-latch level conversion are other options used for dual supply system, here a modified diode-voltage limited level shifter has been discussed that takes the advantages of the input

level conversion independent pull-up devices comparsion has been made for circuit with the conventional approach in terms of power comsumption, area, delay.

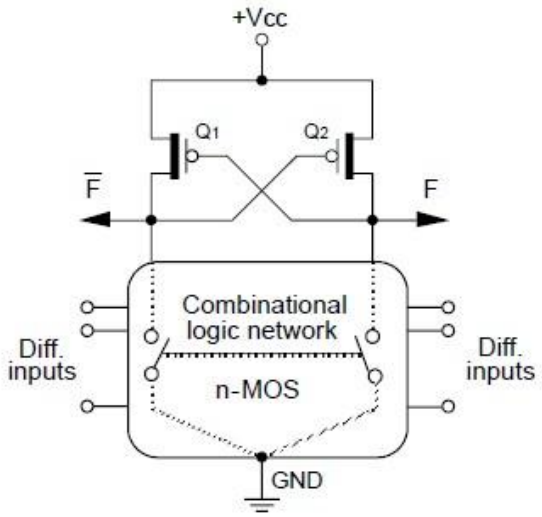

Fig 1: CASCODE VOLTAGE SWITCH LOGIC

The level converter thus becomes an indispensable circuit to interface between different power domain. Robust level coversion from the sub-to-super-threshold voltage is crucial because the sub-threshold signal by which to drive the super threshold circuit are very weak[2]. Time –critical domain run at higher power supply voltage(VDDH) to maximize the performance, whereas non-critical section work at lower power supply voltage (VDDL) to improve power efficiency[3]. Ultra- low voltage design has been proofed to be effective solution since supply voltage is quadratic function of energy. however the high-voltage has 0.5v and VDDH is 1,8v in CMOS technology in multi-voltage supply[4].

However, high-vt transistor (hvt) may still be insufficient to limit the Nmos current. some structure that stack diodes in a suppress the current sourced from VDDH, Nmos transistor usually require low-vt transistor to increase the driving strength. However the minimum VDDL that can be converted depends on the threshold voltage of the HVT and LVT the transistor sizing and circuit structure may not be applied to different technologies.

II.CONVENTIONAL APPROACH

Fig.1 show the circuit diagram of a DCVS-type level shifter, the circuit operates on the basis of connection between pull-up and pull-down devices. In order for the output to switch, the Nmos drive strength has to be sufficiently greater than Pmos drive strength.

The diode-connected and off-biased Pmos transistors are used to limit the drive strength of the pull-up network. Moreover, the multi-threshold CMOS design

technique is applied to tradeoff speed and power consumption. However, owing to the presence of the always off-biased Pmos transistor, maximum of Nmos transistor can be used. Since the greater size to increase the pull up speed at the output nodes.

III.PROPOSED APPROACH

The proposed level shifter using dual cascade voltage switch logic been designed in 180nm process using cadence virtuoso by utilizing multi-threshold voltage CMOS design technique. Low-threshold transistor are placed where leakage current can be reduced at the expense of speed. In addition to low and high transistor a standard threshold transistor is trade-off between Leakage and speed. The use of multi-vth transistor enables to find a good tradeoff between static power consumption, dynamic power consumption and propagation delay.

(A) VOLTAGE LEVEL SHIFTER.

A sub-threshold to above threshold is presented in[5]. The schematic of this VLS is shown in fig2. there are two main stage of the topology. The first stage uses a cross coupled different inverter with a diode-connected Nmos transistor at the top. The second stage is just a cross coupled differential inverter for achieving rail-to-rail swing. The second stage design is not good for achieving high speed.

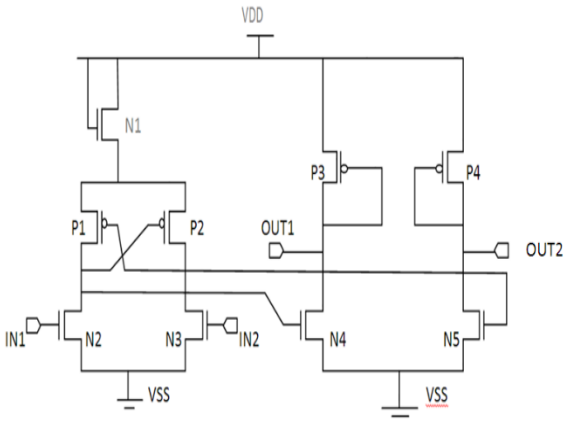

Fig 2: VOLTAGE LEVEL SHIFTER

(B) DIODE BASED VOLTAGE LEVEL SHIFTER

The sub-threshold logic application is shown in fig 3. It achieves high speed by employing diode connected Pmos transistor. The diode connected Pmos transistor. The diodes p1 and p2 are meant to limit the pull up strength of p3 and p4. The use of the diodes limits the negative impact of the short circuit current on the speed. It features to limit the short circuit current itself will certain enhancement in the high speed advantages of this VLS while reducing its power consumption.

$$\beta=(Vdd-Vth-V)$$

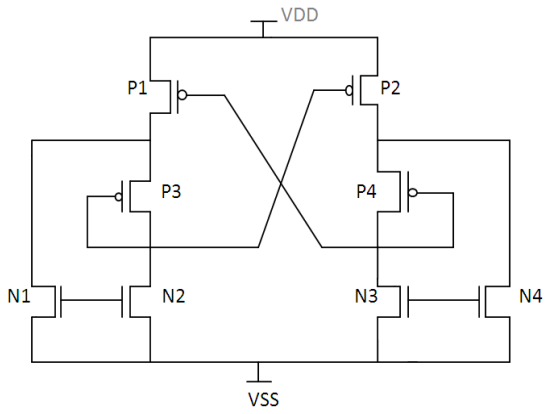

Fig 3: DIODE BASED VOLTAGE LEVEL SHIFTER

(C) LEVEL SHIFTER WITH RESISTOR

We introduce the technique for limiting the short circuit. This technique is shown in fig 4. In this circuit, Pmos latch is slightly modified by the addition of resistor r1 and r2. It blocks the short circuit current from flowing into transistor(mn2 or mn2).

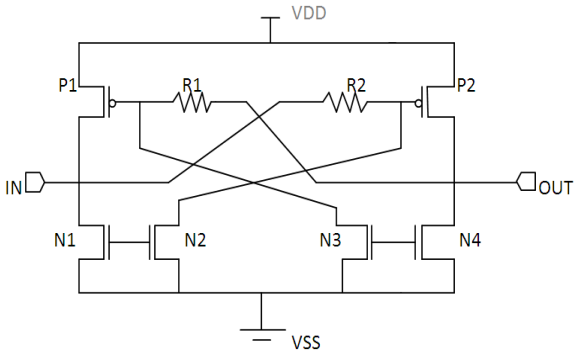

Fig 4: LEVEL SHIFTER WITH RESISTOR

Since the gates of Pmos transistor are very quickly pulled does the Pmos transistor need not be of greater size to increase the pull up speed at the output node. It turns out that these resistance can be very conveniently resistance can be very conveniently realizes by two Nmos transistors as shown in fig.5. This implemention of resistor has two major advantages (1) reduction in area (2) required automatic behavior of the resistance value is achieved.

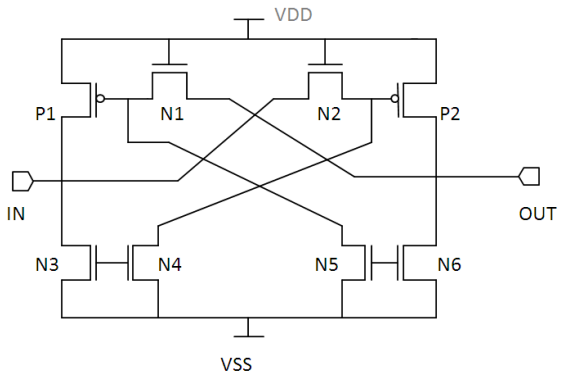

Fig 5: IMPLEMENTATION OF RESISTOR

(D)HYBRID VOLTAGE LEVEL SHIFTER

The circuit was simulated for a range of input voltage values rangings from 0.5v to 1.5v. The output voltages swing is from 0 to 1.8volts. This shown the advantages of this proposed scheme in speeding up the VLS operation. As the input amplitude increase the speed increases.

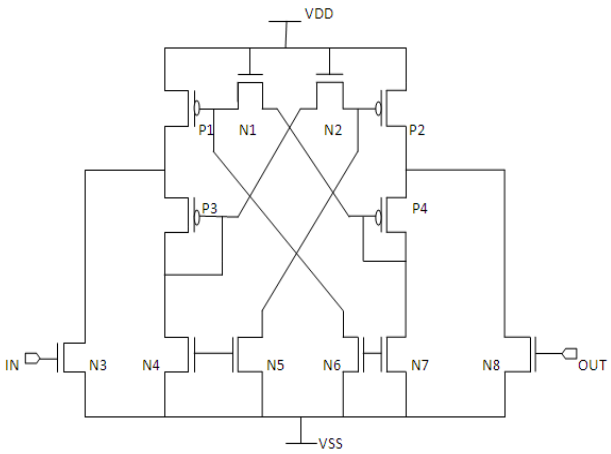

Fig 6: HYBRID VOLTAGE LEVEL SHIFTER

The proposed level shifter has been designed in two version to safisty the needs of both high speed and low power operations taking sub-threshold operation into consideration.

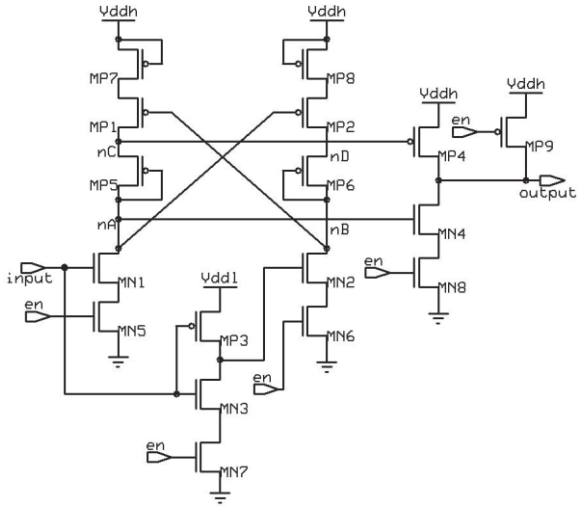

Fig 7: LEVEL SHITER USING DUAL CASCODE VOLTAGE SWITCH.

IV.SIMULATION

We present the Simulation result focusing around the following design parameter: delay, power and leakage current. These design parameter are put in context with scaling of the lower supply voltage. Fig7 energy consumption as a function of vddl for DCVSHS and DCVSLP. However, further reduction of Vddl gives rise to current due to increasing contention between pullup and pull-down transistors, thereby increasing the dynamic power consumption. The decrease in propagation delay confirms the level shifters ability to work at higher operational frequencies as the lower supply voltage increases. The average power consumption is increased with an increase in Vddl as a result of increased dynamic (switching) power consumption in the above threshold region.

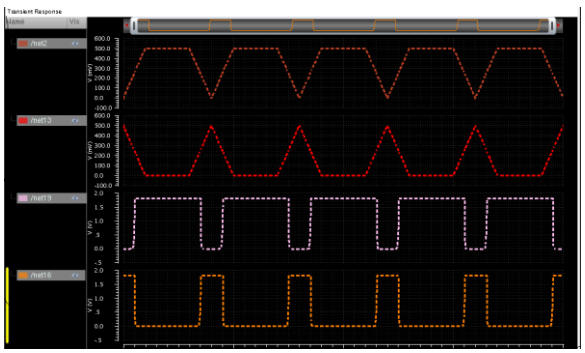

FIG 8 : OUTPUT FOR PROPOSED SYSTEM.

TABLE 1: COMPARATIVE RESULT

	Tech (nm)	Vddh(V)	Vddl (V)	Delay (ns)	power	Leakage current
DCVS	180	1.5	0.5	2.52	2.260µA	-36.02nA
VLS	180	1.8	0.9	6.01	4.050ns	-
DVLS	180	1.8	0.9	6.99	6.6nW	-
LSR	180	1.5	0.5	-	-	-
IR	180	1.5	0.5	6.52	6.4nW	-
PROPOSED	180	1.5	0.5	5.92	6.41ns	16.54ns

V .CONCLUSION

A ratioed logic circuit is Implemented in dual cascade voltage switch are proposed. This technique reduce delay and power of level shifter by blocking the Pmos current from flowing into Nmos transistor. This way, the pull down strength of Nmos transistor is efficiently utilized which reduce power consumption for given delay of level shifter. For application requiring voltage level shifting from sub-threshold voltage to above threshold voltage, the proposed level shifter may serve as a good solution.

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