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Design of An Efficient Carry Select Adder

C. Yuvaraj[1] R. Saravanan[2]
[1]M. Tech, VLSI Design, School of Computing, [2]Assitant Professor, School of Computing,
SASTRA University, India. SASTRA University, India.
Email: yuvi118@gmail.com Email: saravanan_r@ict.sastra.edu

Abstract

High performance digital adder is an important design constraint for advanced processors.Adder is the main component of arithmetic unit. The carry propagation from input to output limits the speed of operation of such adders. An efficient CSA is created for advanced processors to perform fast arithmetic operations.In this paper the delay is reduced by replacing BECwith D-latch. The results are compared for delay and power. The design is simulated using Modelsim-Altera 10.1d and synthesized in Xilinx ISE 8.1i.

Key words: CSA, D-Latch, Delay

Introduction

Area and power reduction are the prime region of research in Very Large Scale Integration. High speed adders are integral specification for high speed processors. They are also used in many other functions such as multipliers. For better system performance the adder circuit has to be executed effectively. The limitation in speed is due to the carry propagation in the addercircuit.

Carry Select Adder (CSA) offers better speed than RCA. Multiple carries are generated and then the actual sum is selected in CSA. They have less propagation delay than an RCA. Several attempts have been made to reduce the use of RCA in a CSA design. Kim and Kim [3] used one RCA and one add one circuit using multiplexers instead of using another RCA block. CSA based on Common Boolean Logic is also proposed [4] .Ramkumar and Kittur suggested a CSA using Binary to Excess one convertor[5]. It occupies less number of logic gates than a conventional CSA. An efficient carry select adder is designed with D-latch. It reduces the delay thereby making it a high speed carry select adder.

Regular SQRT CSA:

The full adder waits for the arriving carry till the carry out of the previous adder is calculated in RCA. This can be eliminated in carry select adder by pre-calculating i.e., evaluating the result in advance for both possible values of Cin. Regular CSA is made up of dual blocks of RCA. The first block is used to develop carry and sum forCin=0. The second block generates the same forCin=1.

The structure of 16-bit SQRT CSA is shown in Fig.1. SQRT CSA is used to obtain better delay performance. Number of groups and size of each group is determined by the size of the adder. Designing a 16-bit CSA involves five groups. Group 1 consist of 2-bit RCA.

From group 2 it involves three levels i.e., in the first level RCA calculates carry and sum with Cin =0, the second level RCA calculates carry and sum with Cin=1 and the third level consist of multiplexer to select the carry and sum depending upon the actualCin.

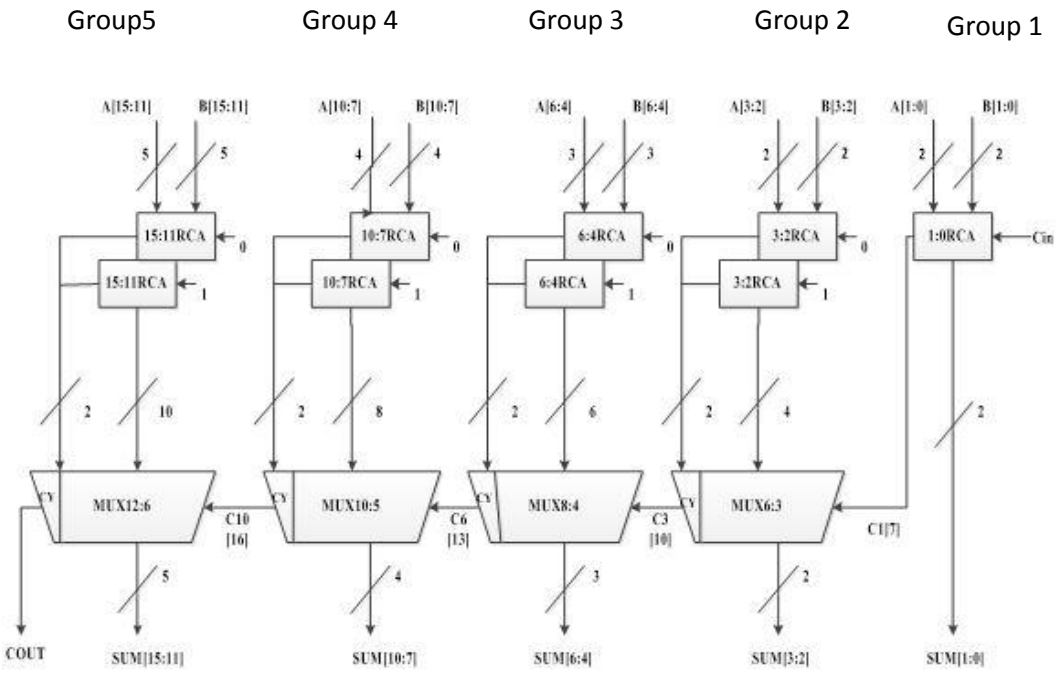


Fig.1. 16-bit Regular SORT Carry Select Adder

BEC Based Carry Select Adder:

In this structure the RCA block with Cin as 1 is replaced by a Binary to Excess one convertor to achieve low power and gate count compared to that of regular carry select adder. The Boolean logic for 4-bit binary to excess 1 convertor is given below,

$$S0 = \sim B0$$

$$S1 = B0 \wedge B1$$

$$S2 = B2 \wedge (B0 \,\&\, B1)$$

$$S3 = B3 \wedge (B0 \,\&\, B1 \,\&\, B2)$$

The functional table for 2-bit BEC is shown in Table I. The functionality of CSA obtained using BEC and multiplexer can be explained using Fig.2.

Table 1:

BEC[1:0]	X[1:0]
00	01
01	10
10	11
11	00

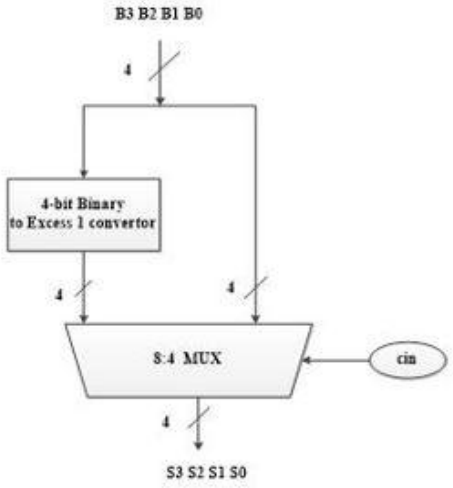


Fig.2.Functioning of CSA with 4-bit BEC

From the fig.2, it is observed that sum output from RCA with Cin=0 is given as input to 4-bit BEC and the output from BEC is given as one input to the multiplexer. The output of BEC corresponds to the output of RCA block with Cin=1. The other input to multiplexer is the output from RCA block. The multiplexer selects the corresponding sum and carry using the input carry Cin. The advantage of BEC logic is that it can be realized with less number of logic gate. Thus silicon area is reduced. The fig.3, shows the 16-bit carry select adder using BEC logic.

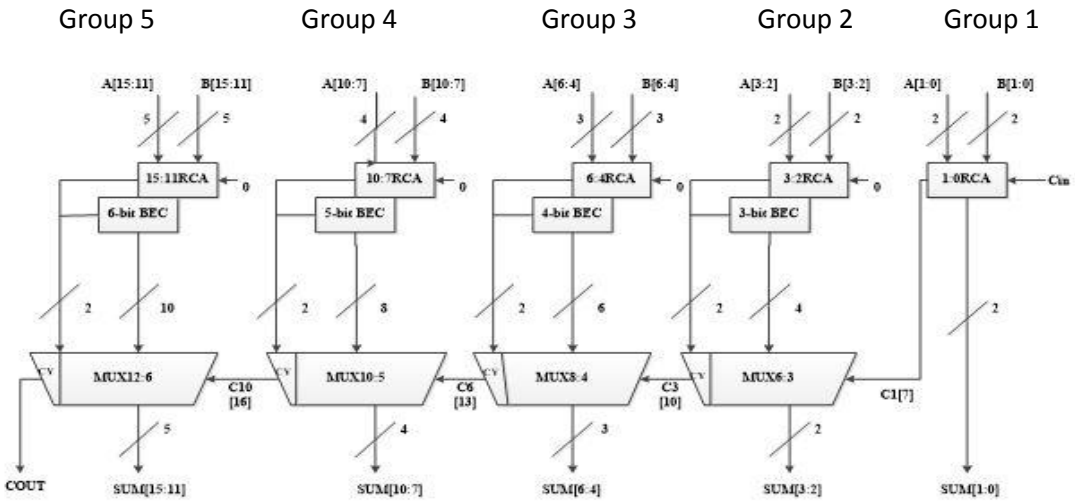
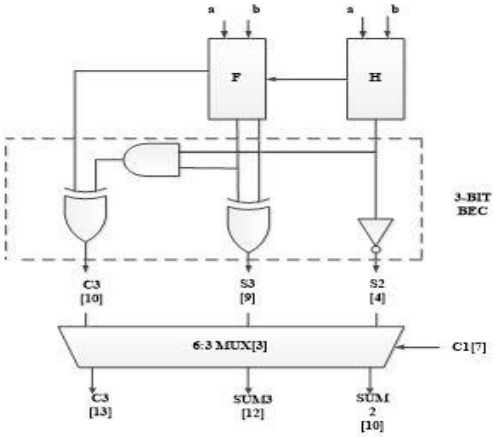
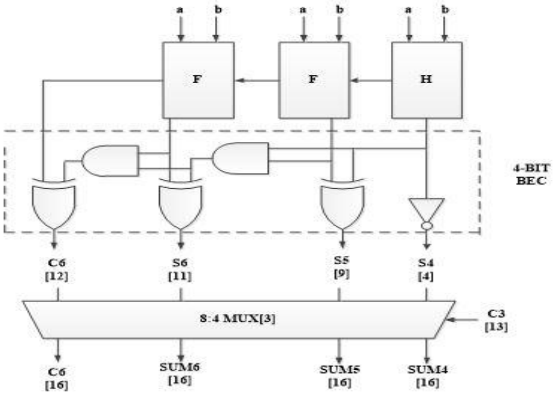


Fig.3.16-bit Carry Select Adder using BEC

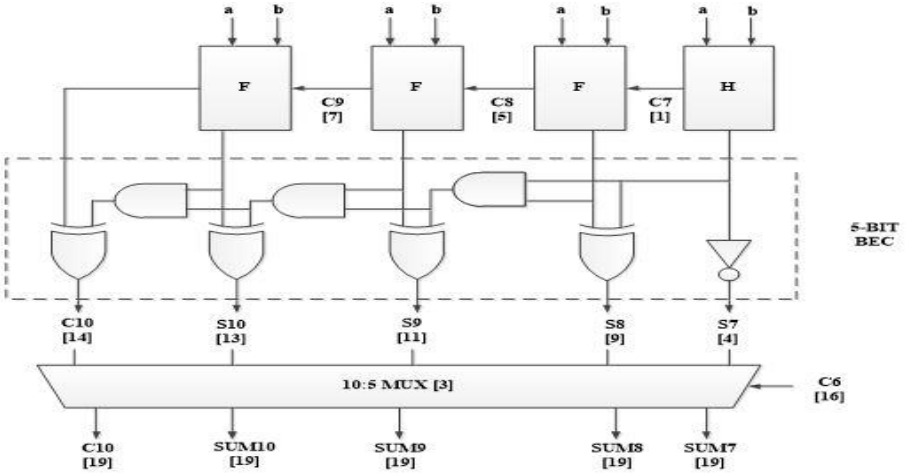
The delay evaluation for BEC based logic can be explained using the fig.4. The values inside [ ] indicates the arrival time. For group 2 the arrival time of c1 of 6:3 multiplexer is before c3 and s3, after s2. Thus sum3 and final c3 are calculated using multiplexer and s3. Sum3 and c3 can also be calculated fractionally from c3 and multiplexer. Sum2 is calculated from c1 and multiplexer. For group 3, group 4 and group 5 the arrival time of select input to the mux is greater than the arrival time of BEC's outputs. The delay in multiplexer and the influx time of selection input to the multiplexer determines the delay of group 3, group 4 and group 5.



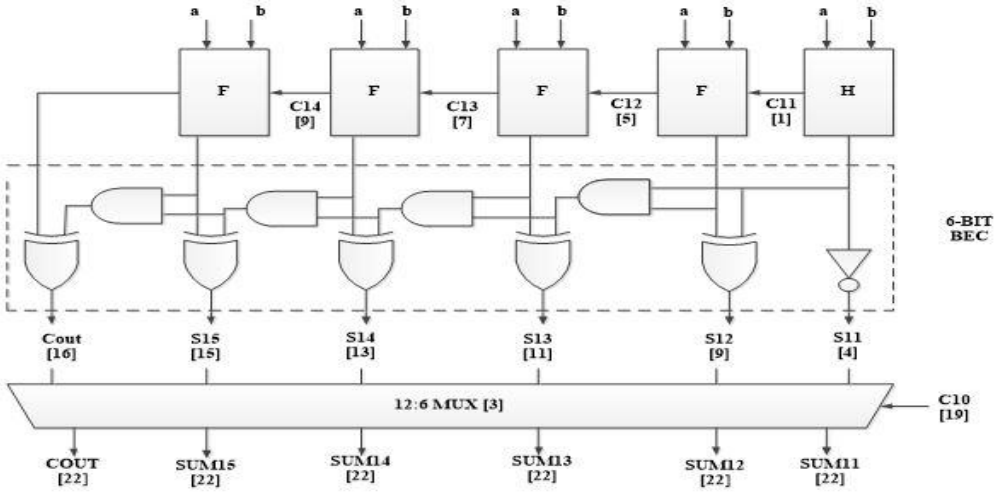
(a)Group 2



(b)Group 3



(c)Group 4



(d)Group 5

Fig.4. Delay and area evaluation of BEC based CSA

Carry Select Adder Using D-Latch:

The structure of CSA is similar to that of CSA using RCA's and BEC. In the carry select adder using D-latch, either the RCA using Cin=1 or RCA using Cin=0 is replaced by D-latch with enable signal as the control signal.Similarly the BEC block in the BEC based CSA can be replaced by D-latch. The enable signal replaces the Cin of the ripple carry adder. The enable signal is a clk signal. The structure of CSA using D-latch is shown in fig.5.

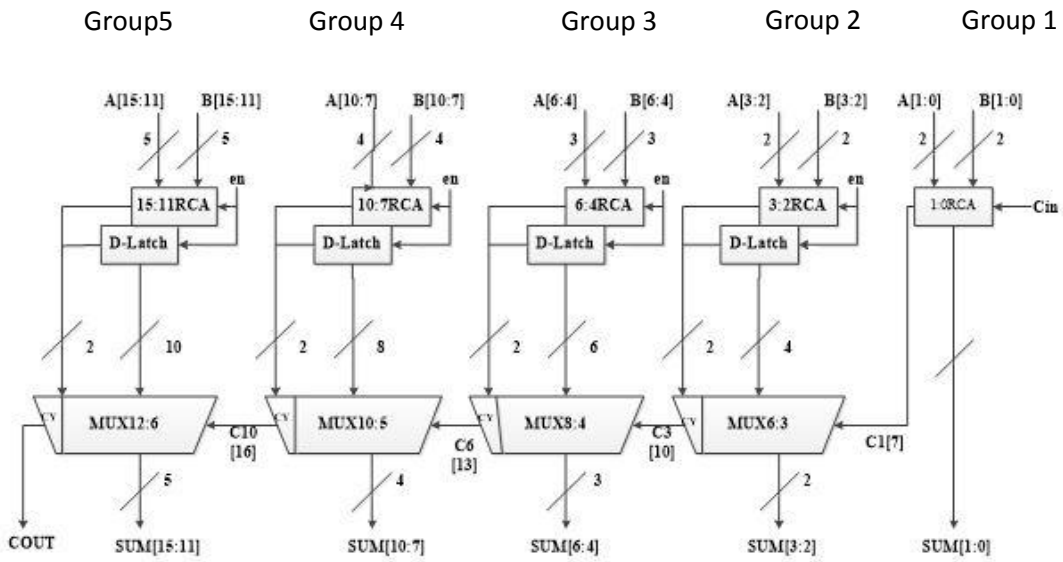


Fig.5.16-bit Carry Select Adder using D-Latch

One bit wide data can be stored in a Latch. The outputs are affected in a perpetual manner as long as they are enabled. In this 16-bit adder, the least significant adder is a 2-bit ripple carry adder. The most significant part of the adder is 14-bit wide and works according to the clock signal given as enable. When the clk goes high, the RCA calculates sum and carry for Cin=1. When clk goes low, the RCA calculates sum and carry for Cin=0. These results are stored in D-latches. Carry out from group 1 is given as the select input for multiplexer in group 2.

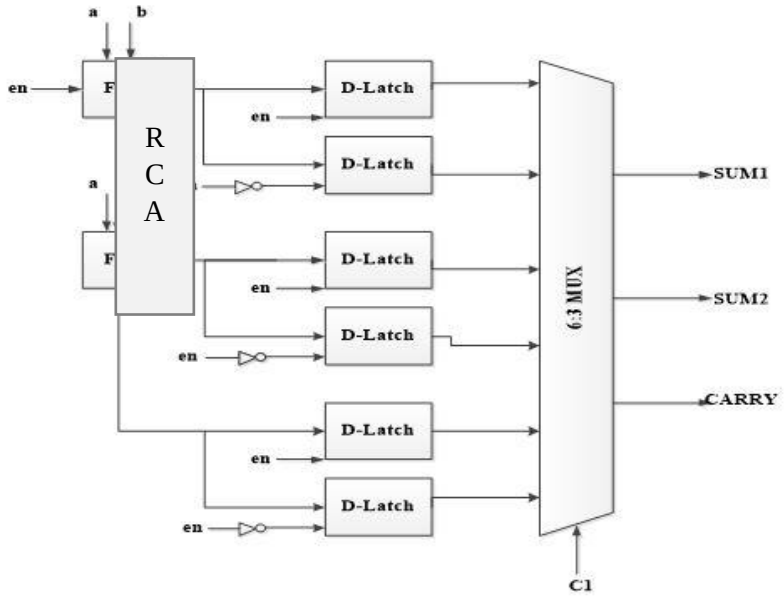


Fig.6.Group 2 for D-latch based CSA

Group 2 for CSA using D-latch is shown in fig.6. The Cin to the RCA is the enable signal which is a clk signal. The carry out of first full adder is given as the third input to the second full adder. There are six D-latches that are used to store the sum and carry from the full adders. The multiplexer selects the actual sum and carry based on the selection input.

Results

The design is developed using Verilog HDL and simulated using Modelsim-Altera 10.1d. Simulation results are shown in fig.7 and fig.8.

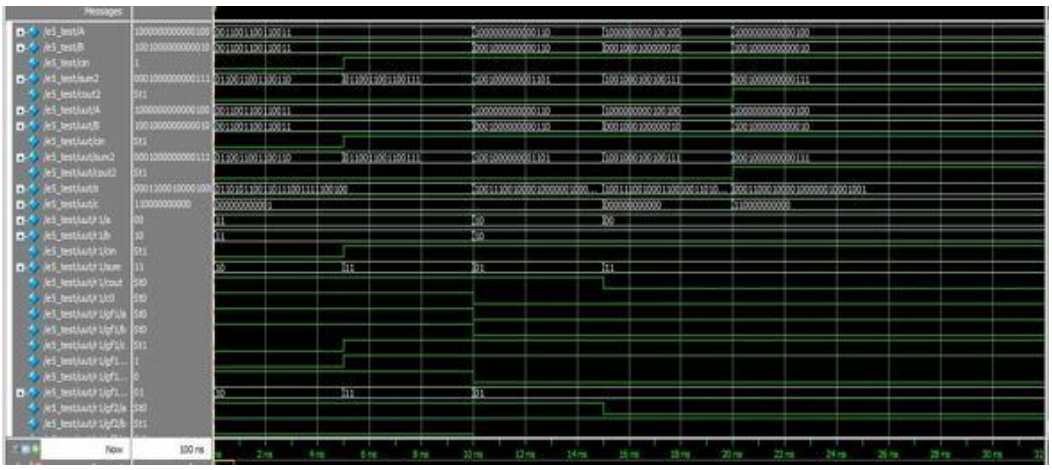


Figure 7: Simulation result for BEC based CSA

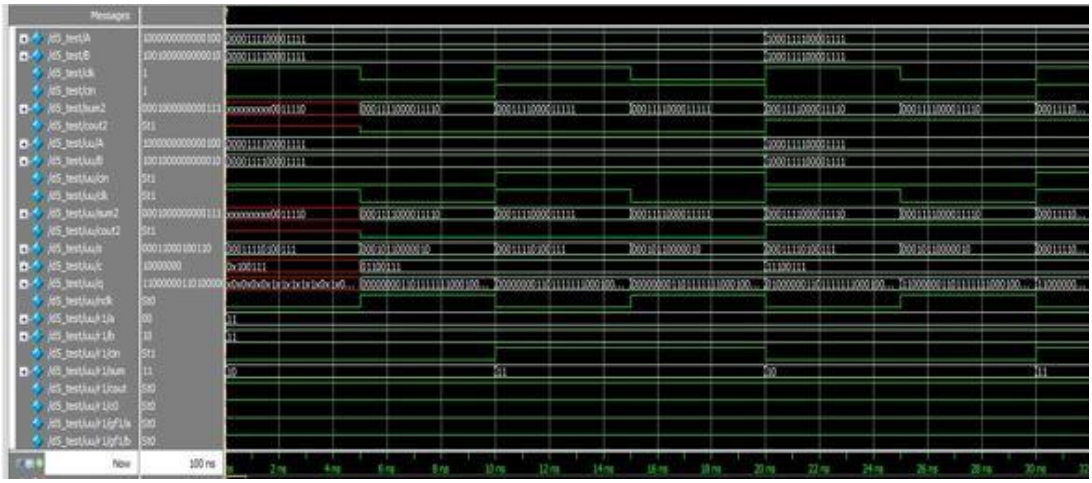


Figure 8: Simulation result for D-latch based CSA

The design is synthesized using Xilinx ISE 8.1i using the family Spartan 3E. XC3S500E device is used with the package FT256 and with the speed grade of -5. The delay and power for BEC based Carry Select Adder and D-latch based Carry select Adderis compared and is shown in the Table-II

Table 2:

ADDER(16-BIT)	DELAY(nS)	POWER(mW)	PDP(10^-12)
CSA using BEC	16.110	25	402.75
CSA using D-latch	13.796	24.60	339.38

Conclusion

A simple approach to lower the delay in the BEC based SQRT CSA is proposed. The compared results shows that the CSA based on D-latch has lesser delay. It can also be observed that the power-delay product has also been reduced in the proposed adder. The Carry Select adder using D-latch is efficient for high speed applications.

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