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Multiple Single Input Change Vector Generation By Using Single Cycle Access Method: BIST Architecture

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Abstract

This paper proposes a new single cycle access test structure for logic test. It will eliminates the unnecessary dynamic power consumption problem of conventional shift-based scan chains during switching transition in the scan FF and also reduces the accessing time within one clock cycles. This leads to more realistic circuit behavior during stuck-at and at-speed tests. It enables the complete test to run at higher frequencies equal or close to the one in functional mode. It will be shown that within one clock cycle testing can be achieved compared to other published solutions We carried out testing with some published solutions on ISCAS'89 net list. In functional mode this LFSR module will be used for stegnography application and in testing mode this will act as a random generator .The structure allows an additional on-chip debugging signal visibility for each register.

Keywords- LSB steganography, Built-in self-test (BIST), linear feedback shift register (LFSR).

I INTRODUCTION

In recent years, the design for low power has become one of the greatest challenges in high-performance very large scale integration (VLSI) design. As a consequence, many techniques have been introduced to minimize the power consumption of new VLSI systems. However, most of these methods focus on the power consumption

during normal mode operation, while test mode operation has not normally been a predominant concern. However, it has been found that the power consumed during test mode operation is often much higher than during normal mode operation.

Another category of techniques used to reduce the power consumption in scan-based built-in self-tests (BISTs) is by using scan chain-ordering techniques [7]–[13]. These techniques aim to reduce the average-power consumption when scanning in test vectors and scanning out captured responses. Although these algorithms aim to reduce average-power consumption, they can reduce the peak power that may occur in the CUT during the scanning cycles, but not the capture power that may result during the test cycle (i.e., between launch and capture).

Automatic test pattern generation (ATPG) for sequential VLSI circuits is an NP-complete problem with an exponential complexity. The complexity of combinatorial logic varies. Less complex logic is tested within a few capture cycles, generating an immense number of don't cares during the rest of the test, even when test compression methods are used. Complex and hard to test logic needs to be stimulated and captured quite often but the pattern need to be shifted throughout the complete scan chain. One approach to reduce test time is to use parallel scan chain. This leads to a massive increase of parallel scan chains to reduce the length of the scan chains. In order to further reduce test data volume, a built-in-self-test (BIST) mechanism is used.

Mostly LFSR is used as random number generator to give random inputs for testing. So for any BIST application LFSR will be main design module .

II OVERVIEW

Several advanced BIST techniques have been studied and applied. The first class is the LFSR tuning. Girard *et in [4]* analyzed the impact of an LFSR's polynomial and seed selection on the CUT's switching activity, and proposed a method to select the LFSR seed for energy reduction .The second class is low-power TPGs. One approach is to design low-transition TPGs. Wang and Gupta in [5] usedtwo LFSRs of different speeds to control those inputs that have elevated transition densities . Corno *et al. in [6]* provided a lowpower TPG based on the cellular automata to reduce the test power in combinational circuits . Another approach focuses on modifying LFSRs.E sram in [7] reduces the power in the CUT in general and clock tree . However, this dependency implies that nondetecting subsequences must be determined for each circuit test sequence. Bonhomme *et al.* [9] used a clock gating technique where two nonoverlapping clocks control the odd and even scan cells of the scan chain so that the shift power dissipation is reduced by a factor of two. The ring generator [10] can generate a single-input change (SIC) sequence which can effectively reduce test power. The third approach aims to reduce the dynamic power dissipation during scan shift through gating of the outputs of a portion of the scan cells.

Bhunia *et al.* [11] inserted blocking logic into the stimulus path of the scan flip-flops to prevent the propagation of the scan ripple effect to logic gates. The need for transistors insertion, however, makes it difficult to use with standard cell libraries that do not have power-gated cells. In [12], the efficient selection of the most suitable

subset of scan cells for gating along with their gating values is studied. The third class makes use of the prevention of pseudorandom patterns that do not have new fault detecting abilities [13]–[15]. These architectures apply the minimum number of test vectors required to attain the target fault coverage and therefore reduce the power. However, these methods have high area overhead, need to be customized for the CUT, and start with a specific seed. Gerstendorfer *et al.* also proposed to filter out nondetecting patterns using gate-based blocking logics [16], which, however, add significant delay in the signal propagation path from the scan flip-flop to logic.

Several low-power approaches have also been proposed for scan-based BIST. The architecture in [17] modifies scan-path structures, and lets the CUT inputs remain unchanged during a shift operation. Using multiple scan chains with many scanenable (SE) inputs to activate one scan chain at a time, the TPG proposed in [18] can reduce average power consumption during scan-based tests and the peak power in the CUT. In [19], a pseudorandom BIST scheme was proposed to reduce switching activities in scan chains. Other approaches include LT-LFSR [20], a low-transition random TPG [21], and the weighted LFSR [22]. The TPG in [20] can reduce the transitions in the scan inputs by assigning the samevalue to most neighboring bits in the scan chain. In [21], power reduction is achieved by increasing the correlation between consecutive test patterns. The weighted LFSR in [22] decreases energy consumption and increases fault coverage by adding weights to tune the pseudorandom vectors for various1probabilities.

I. Pseudo-Random Number Generator

Pseudo random number generator (PRNG) prevents invaders to find message bits easily. A secret key can be used as a seed for PRNGs. Using a seed causes PRNGs to generate the same random numbers on receiver side as on the sender side. In this paper, a linear feedback shift register (LFSR) is used as PRNG.

1.1 Implementation of LFSR

A LFSR is made of sequential shift-register with combinational feedback logic connected to it which can generate a sequence of binary values in a pseudo-random manner. A design modeled around LFSRs often has both speed and area advantages over a functionally equivalent design that does not use LFSRs. Linear Feedback Shift Register(LFSR) method is commonly used conentional method in BIST for test pattern generator. In this conventional method we can have 100% fault coverage.there are two modes in BIST.test mode and functional mode.power dissipation in test mode is more.[2]. As shown in Fig. 1, it is obtained with an array of FFs with a linear feedbackperformed by several XOR gates. Although LFSRs are very simple to implement, they are based on a rather complex mathematical theory [5]. A 3-stage LFSR is characterized by its feedback polynomial [7], [5] given by $P(x) = 1 + x2 + x3$. The initial value of LFSR is called seed value..The power consumption is high in this method As there are more switching activities

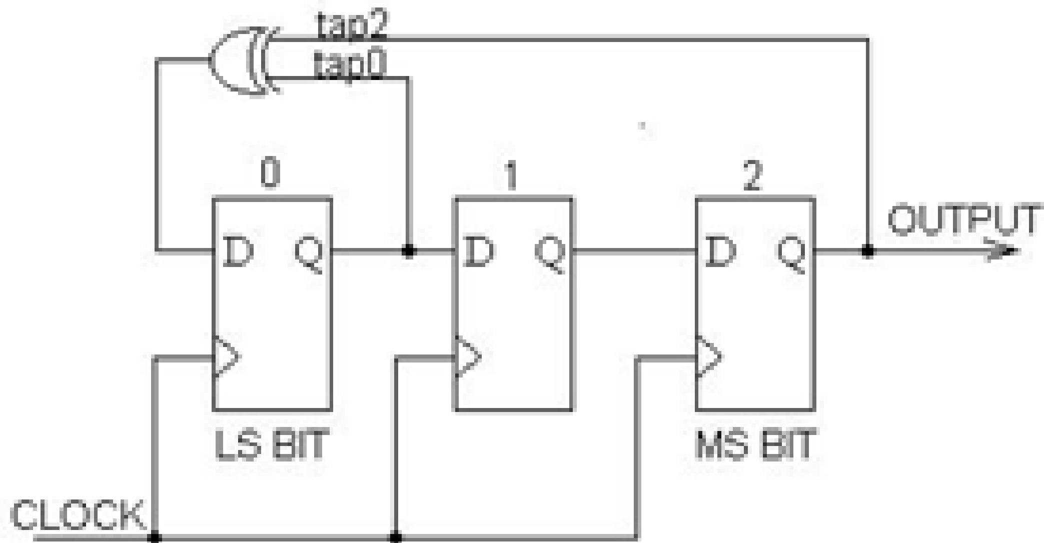


Fig 1 Three bit Conventional LFSR

Feedbacks around an LFSR's shift register are connected to the certain points (taps) of LFSR construction and constitute either XORing or XNORing these taps to provide taps back into the register.

The selection of taps determines how many values can be generated in a given sequence before the sequence is repeated. Certain tap arrangement lead to maximal length sequences of (2n - 1).

3.2 RECONFIGURABLE JOHNSON COUNTER

The ring generator can generate a single-input change (SIC) sequence which can effectively reduce test power. Generated SIC sequences have low transition sequences for each scan chain. This can decrease the switching activity in scan cells during scan-in shifting.

For a short scan length, we develop a reconfigurable Johnson counter to generate an SIC sequence in time domain. As shown in Fig. 2 it can operate in three modes.

1) *Initialization:* When RJ_Mode is set to 1 and *Init* is set to logic 0, the reconfigurable Johnson counter will be initialized to all zero states by clocking CLK2 more than l times.
2) *Circular shift register mode:* When RJ_Mode and Init are set to logic 1, each stage of the Johnson counter will output a Johnson codeword by clocking CLK2 l times.
3) *Normal mode:* When RJ_Mode is set to logic 0, the reconfigurable Johnson counter will generate $2l$ unique SIC vectors by clocking CLK2 $2l$ times.

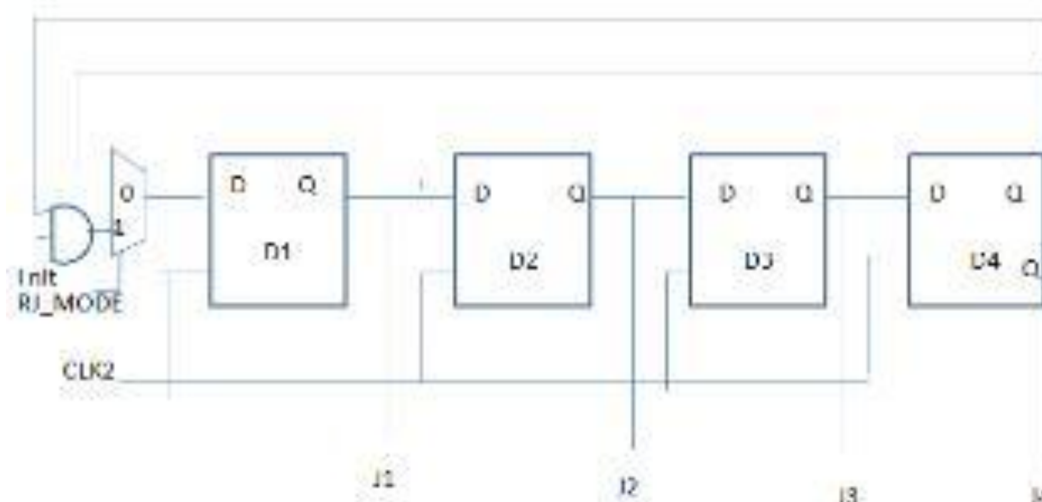


Fig 2 Reconfigurable Johnson counter.

3.3 SCALABLE SIC COUNTER

When the maximal scan chain length l is much larger than the scan chain number M, we develop an SIC counter named the "scalable SIC counter." As it contains a k-bit adder clocked by the rising *SE* signal, a k-bit subtractor clocked by test clock CLK2, an M-bit shift register clocked by test clock CLK2, and k multiplexers. The value of k is the integer of $\log 2(l - M)$. The waveforms of the scalable SIC counter are shown in Fig. 3 The k-bit adder is clocked by the falling *SE* signal, and generates a new count that is the number of 1s (0s) to fill into the shift register. As shown in Fig. 3.3 it can operate in three modes:

1) If $SE = 0$, the count from the adder is stored to the k-bit subtractor. During $SE = 1$, the contents of the k-bit subtractor will be decreased from the stored count to all zeros gradually.
2) If $SE = 1$ and the contents of the k-bit subtractor are not all zeros, M-Johnson will be kept at logic 1 (0).
3) Otherwise, it will be kept at logic 0 (1). Thus, the needed 1s (0s) will be shifted into the M-bit shift register by clocking CLK2 l times, and unique Johnson codewords will be applied into different scan chains.

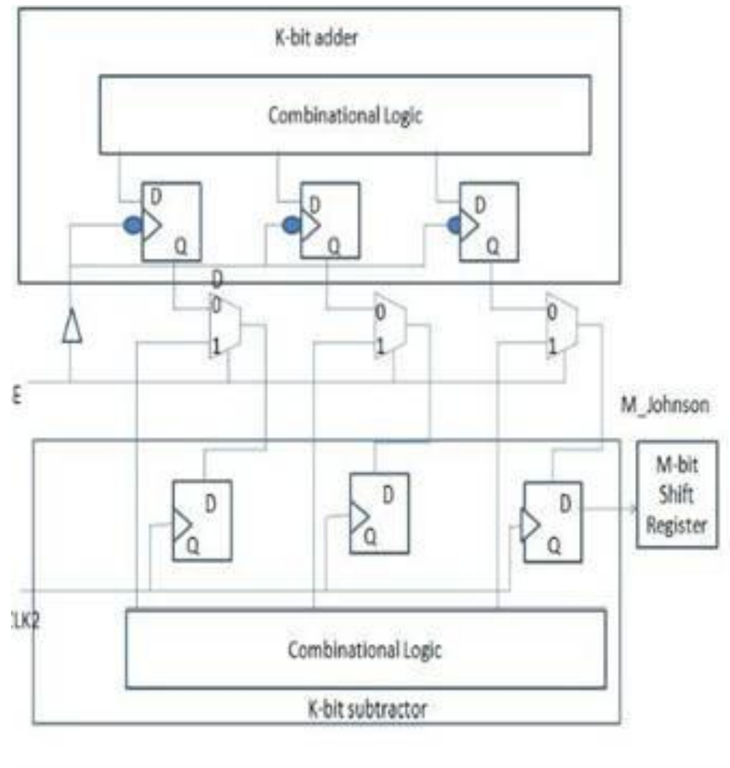


FIGURE 3 SCALABLE SIC COUNTER

IV BIST IMPLEMENTATIONS

In conventional scan-BIST architecture uses an LFSR to generate pseudo-random patterns that are serially loaded into each scan chain of the circuit under test (CUT). Here we used Vedic multiplier to verify the functionality of proposed SCA enabled MSIC based random generator for built in self test (BIST). Global scan enabled signal is used to control over testing process. Area will be increased considerably in case of Global SCA as compared to conventional S-FF due to large transitions in the design. But overall power dissipation will be increased due to shift based scan approach through page set up gated clock is used to avoid unnecessary transitions.

A. single cycle access structure

The Scan cells are connected into multiple shift registers. (Scan chains). Number of clock cycles needed to access the particular register is depends on register position from boundaries. The key element of the single cycle access structure (SCA) is the signal cycle access register (Flip-Flop, FF) with hold mode (SCA-FF). It is based on a standard scan register (S-FF) and uses two more 2-to-1 multiplexers. The new SCA FF can be seen in Fig. 4. The SCA-FF has one more input and one more output compared to the standard shift register (S-FF). The inputs clock {clk}, data-in {di}, and scan-in {si} still exists. The scan-enable is now a 2 bit bus {se[0:1]}. An additional scan output pin {so} is added. The reset input and inverse output pins are

not shown. The internal logic enables the register to run in one additional hold mode, whereas the additional output multiplexer can bypass the register to directly drive the value of {si}.

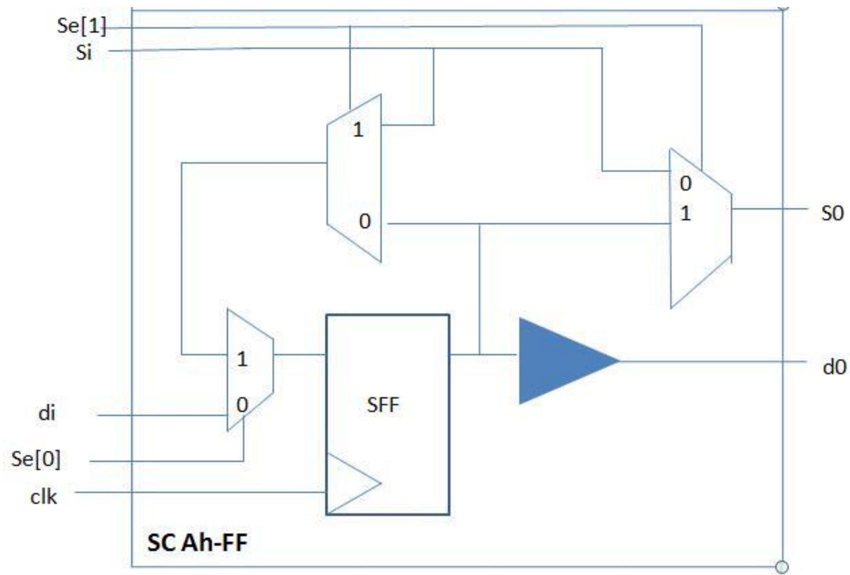
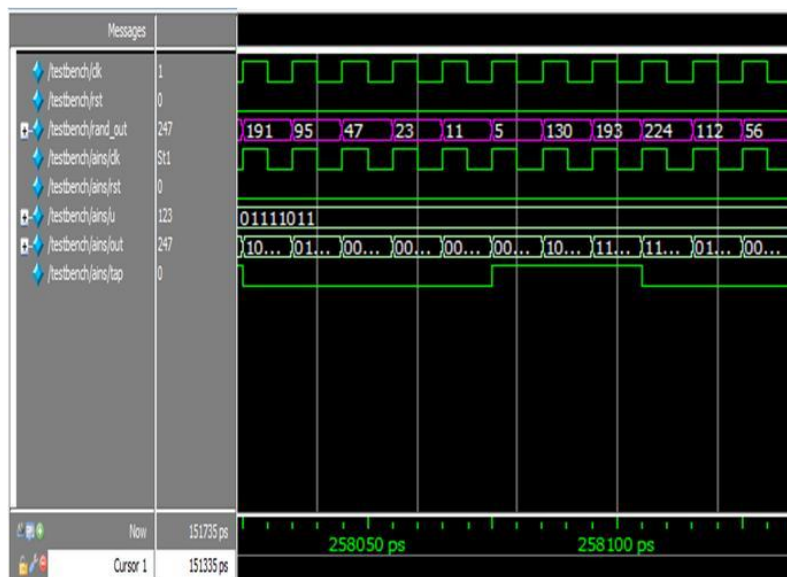


Fig 4 .SCA FF

V RESULTS

5.1 SIMULATION OUTPUT OF LFSR

Corresponding verilog code is written for LFSR and test patterns generated are shown in the waveform.



5.2 SIMULATION RESULT OF SCALABLE SIC COUNTER

Corresponding verilog code is written for SCALABLE SIC COUNTER and the patterns generated are shown and they have less switching activity.

5.3 SIMULATION RESULT OF SCA METHOD

Test patterns are applied to vedic multiplier and the corresponding wave forms are mentioned .nIn BIST there are functional mode and testing mode . In functional mode values to the test pattern generator should be given externally.In testing mode inputs are given by the LFSR itself.

VI COMPARISION OF TPG

Random generator	Power(mW)	Benchmark s641 model
LFSR	68.35	67.71
MSIC pattern generator	66.69	59.04

Random generator	Number of seeds used	Transitions covered
LFSR	12	5.048 xe+07
MSIC pattern generator	10	5.110 xe+07

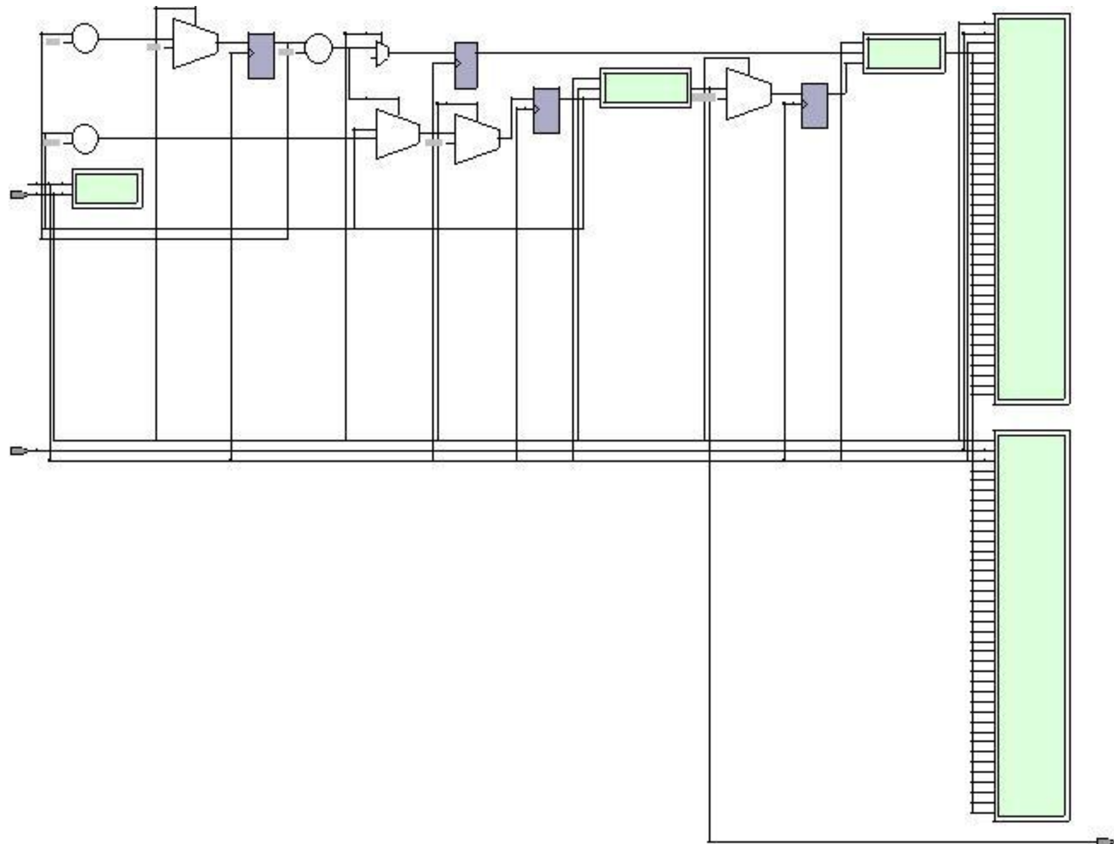


Figure 5. RTL view

V. CONCLUSION

This paper has proposed a new shift scan method called single cycle access. Using these method within single clock we can access any output. Here the output is measured at any particular instant, by this execution time will be less when compared to conventional shift scan method. Switching activity is less when compared to existing methods. Proposed method is applied to vedic multiplier and corresponding waveforms are mentioned above.

REFERENCES

[1] A. P. Chandrakasan, N. Verma, and D. C. Daly, "Ultra low power electronics for biomedical applications," *Annual Review of Biomedical Engineering*, vol. 10, pp. 247-274, August 2008.

[2] L. Mateu and F. Moll, "Review of energy harvesting techniques and applications for microelectronics," *Proc. SPIE Microtechnologies for the New Millennium*, pp. 359-373, 2005.

[3] V. Raghunathan and P. H. Chou, "Design and power management of energy harvesting embed ed systems," *Proc. International Symposium on Low Power Electronics and Design*, pp. 369-374, 2006.

[4] C. Lu, S. P. Park, V. Raghunathan, and K. Roy, "Efficient power conversion for ultra low voltage micro scale energy transducers," *Proc. Design, Automation and Test in Europe*, pp. 1602-1607, 2010.

[5] Optobionics Corp. (http://optobionics.com/)

[6] C. Lu, V. Raghunathan, and K. Roy, "Maximum power pointconsiderations for micro-scale solar energy harvesting systems," *Proc. International Symposium on Circuits and Systems*, pp. 273-276,2010.

[7] E. Esram and P. L. Chapman, "Comparison of photovoltaicarray maximum power point tracking techniques," *IEEE Transactions on Energy Conversion*, vol. 22, no. 2, pp. 439-449, June 2007