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Implementation of Optimized SRAM Cell Design For High Speed And Low Power Applications

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Abstract

This paper explores the design and analysis of new Static Random Access Memories (SRAMs), focusing on optimizing high speed and low power. In this paper, a new SRAM cell architecture is employed, which consists of an asymmetric inverter pair to reduce the power consumption but has a slightly increased area. The circuits consume lower power during read and write operations compared to 6T conventional circuit. The circuit consists of one memory cell and the precharge circuitry connected with the bit lines pairs of memory. All circuits are synthesized using Cadence' Tool and the circuits are optimized using TSMC library based on 90 *nm* technology. The applications of SRAM cells are mainly in low power and high speed fields, especially mobile phones, laptops etc.

Index Terms: 9T SRAM Cell read and writes operation.

Introduction

In the past decades there has always been a need to decrease the relative speed difference between the external memories and the processor. Usage of multilevel caches in the chips is a method of enhancing the IC performance and also reduction in accessing of external memories. The main aspects of the designs now are optimizing the power and speed of the SRAMs during the read as well as write operations.

In order to achieve the power consumed, there is a use of zero aware asymmetric cell, which when incorporated in the circuit enables better performance during the read and write operation when compared to the conventional 6T circuit. Since SRAMs are widely used, the proposed method results in a very useful power reduction method.

Zero – Aware Ssymmetric Cell

The corresponding circuit diagram of the design explained [2] is shown in Fig. 1. Transistor N3 is used for power reduction during the write zero operation. The signal line WS controls transistor N3. During the read operation critical path, having an alternative path for discharging improves the efficiency of the operation. Also using different bit lines for the read and writes operations makes the cell more stable.

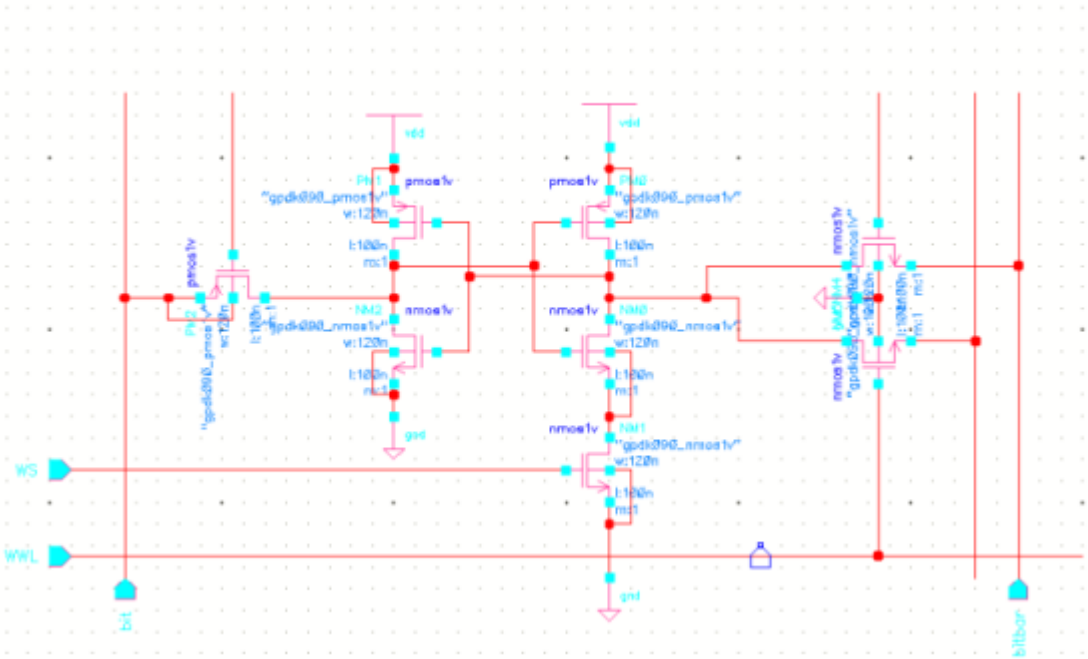

Figure 1: Zero – Aware Asymmetric Cell

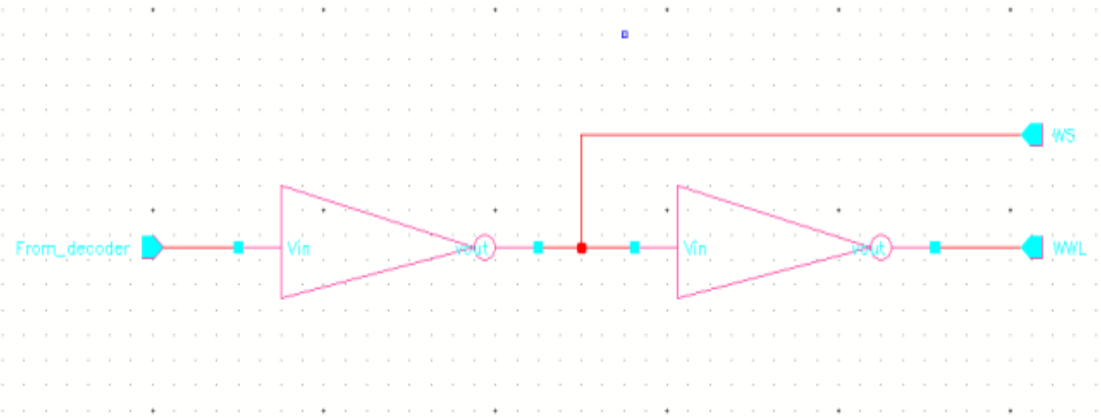

Figure 2: Generation of Write Select (WS) and Write Word Line (WWL) signals\

Proposed Circuit Design and Its Functioing

Fig. 2. Shows the schematic of the 9T SRAM Cell. Transistor N7 is used for reducing the power and it varies from the zero aware circuit in the aspect that N7 is connected to the bit line and not to the write select. Area overhead is reduced due to this and the performance of the design is made identical to the 6T Cell by connecting N6 as shown in the figure above. Since the resistance is reduced, the power consumption is more efficient as compared to the zero aware circuit. The input RBL' and N5 can be used to perform the necessary read operation. The usage of tail transistors along with a pass transistor helps in the performance of the read operation. Optimizing the circuit at all times requires the WS signal to be operated as a compliment of the WZ signal but this aspect might not occur all the time since errors may be present in the clock. Finally the functionality of the WS signal and replace the control of the tail transistor using the bit line signal. Appropriate sizing of the transistors prevents the tail transistors from altering the stability of the read operation. This hence results in a better power and delay performance when compared to the zero aware circuit and also the 6T conventional cell.

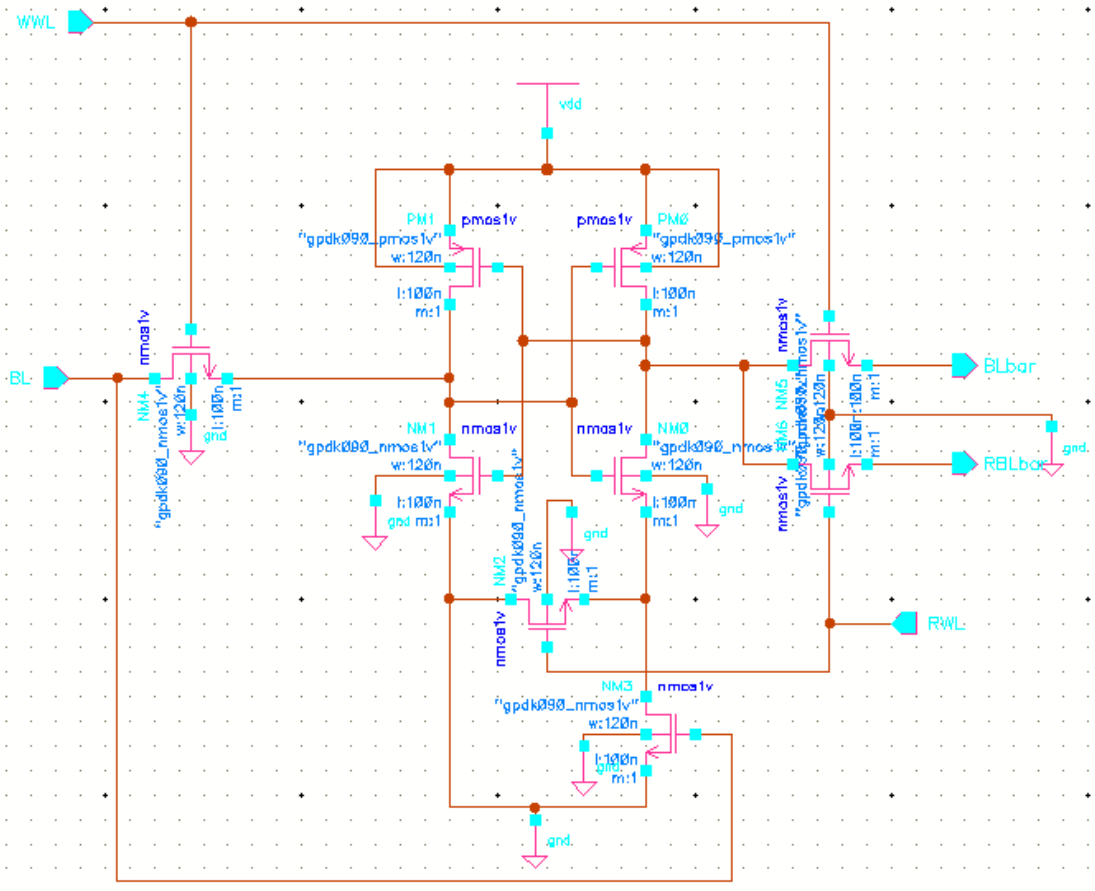

Figure 3: Schematic of 9T SRAM Cell

Designing of Read And Write Circuits Along With Results

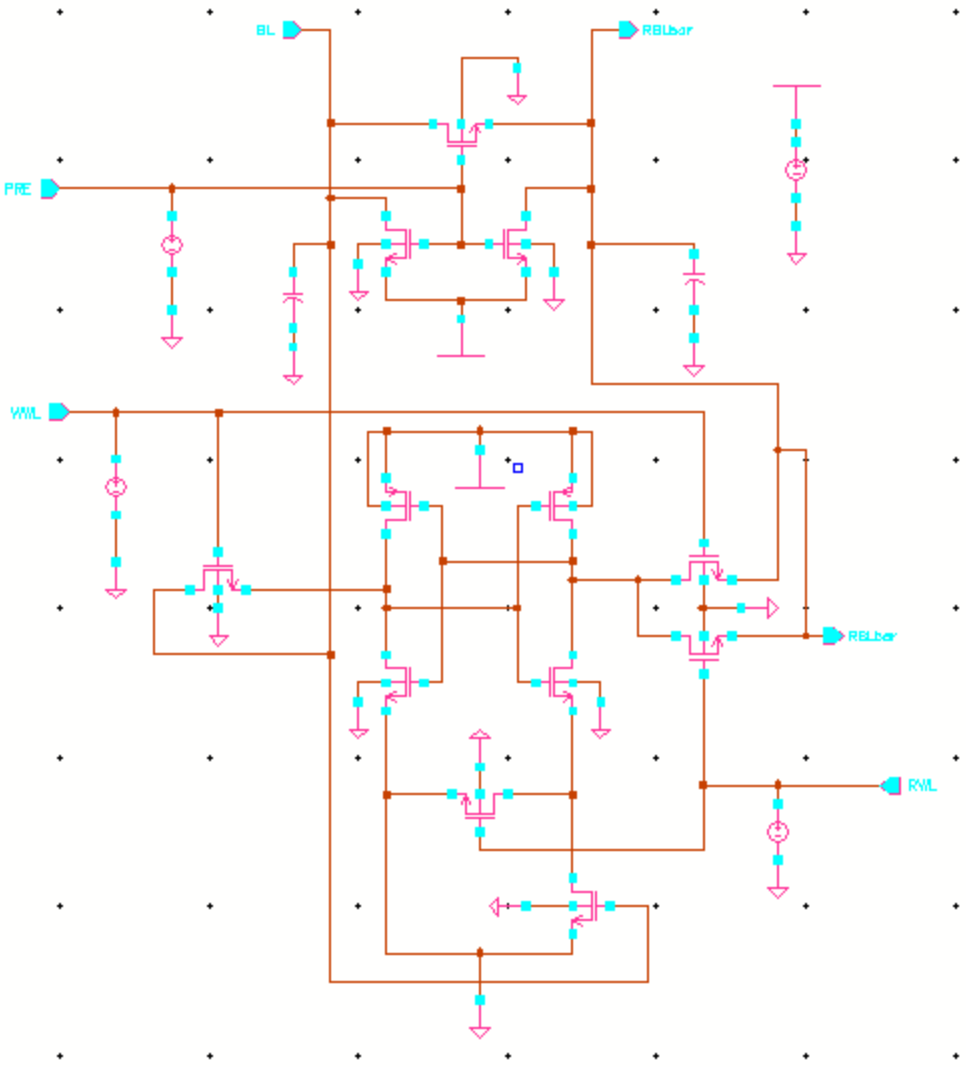

Figure 4: Schematic Diagram for Read Mode

Fig. 3. shows the design of the read mode circuit. The above circuit is designed with the main goals being reduction in delay and power during the read operation. Similarly, Fig. 4. shows the design of the write mode circuit. This is also designed for achieving the same goals as in the read mode case. The simulation for different modes is done in Cadence using different W/L ratios for the transistors until the necessary conditions are satisfied. In both the read as well as the write modes, the circuit consists of a memory cell and precharge circuitry connected with the bit line pairs of memory.

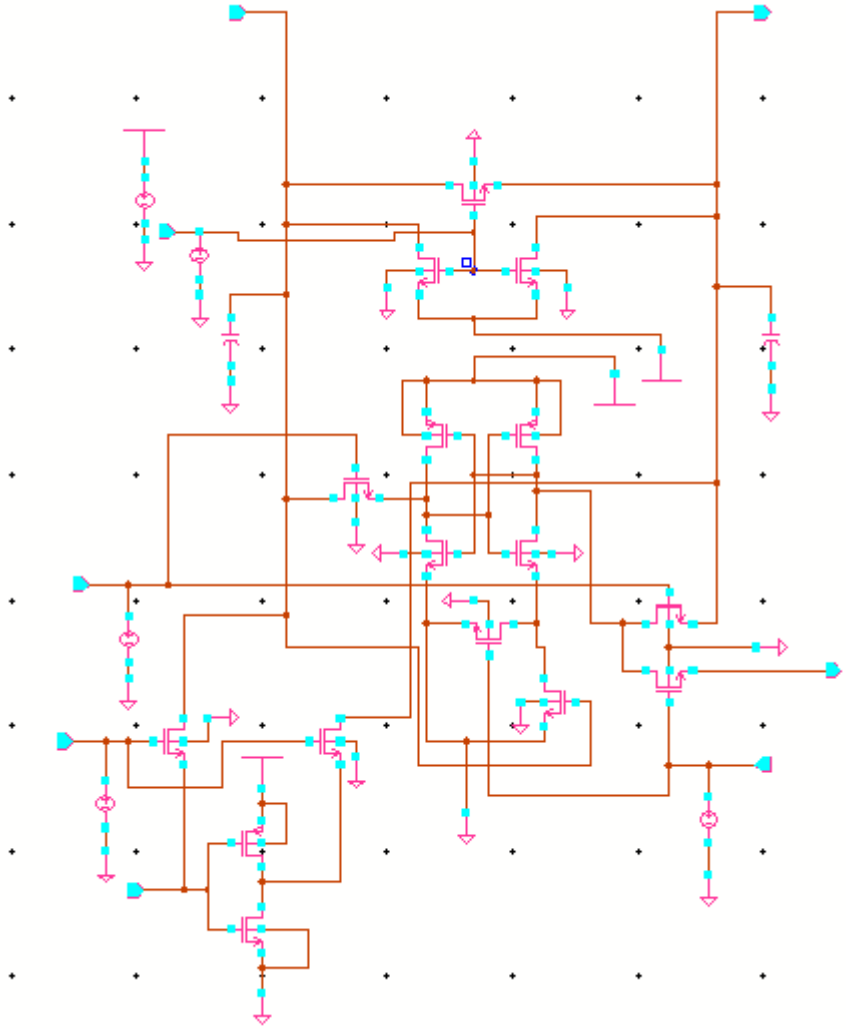

Figure 5: Schematic Diagram for Write Mode

Cadence ADE Tool for the purpose of simulating the design and the following are the required inferences:

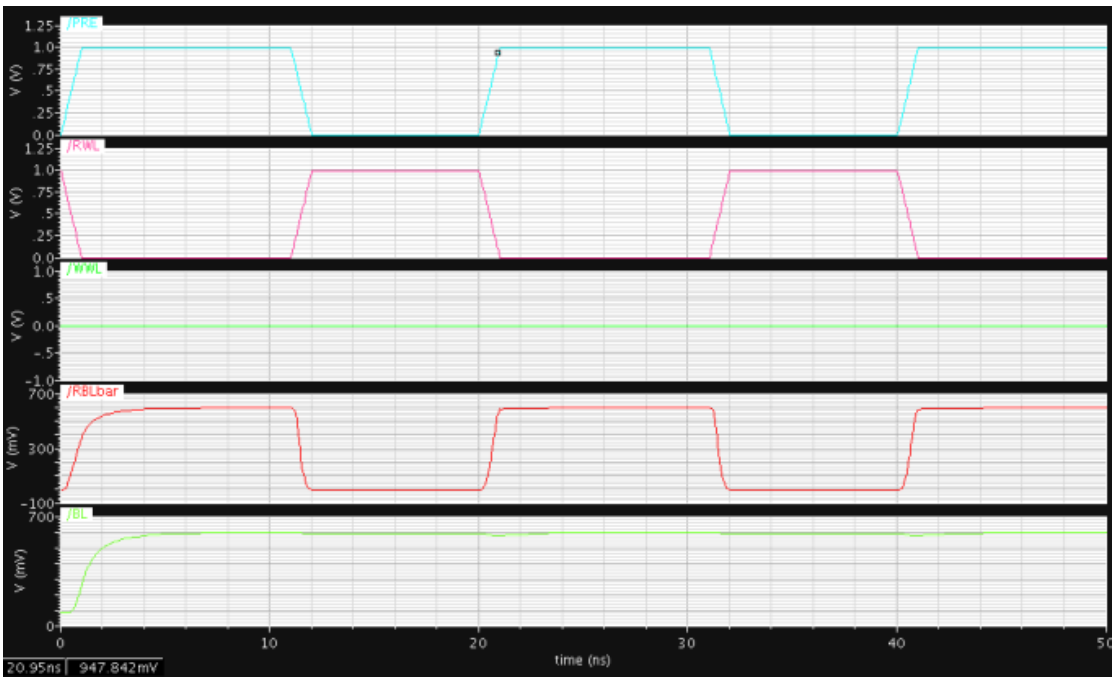

Figure 6: Bit Line Voltage variations during read 1 operation

The above Fig. 6. indicates how the voltage of the bit lines varies during the read 1 operation. Initially the bit lines are all precharged to 1V when the PRE signal occurs and once the read operation is performed, these are bound to change. The status of all the bit lines is as shown above. Sizing of transistors helps in the adjustment of the power consumed. Similar process applies for the read 0 operation and Fig. 7. indicates the status of the bit lines. Power values for read 0 and read 1 operations are shown in TABLE I.

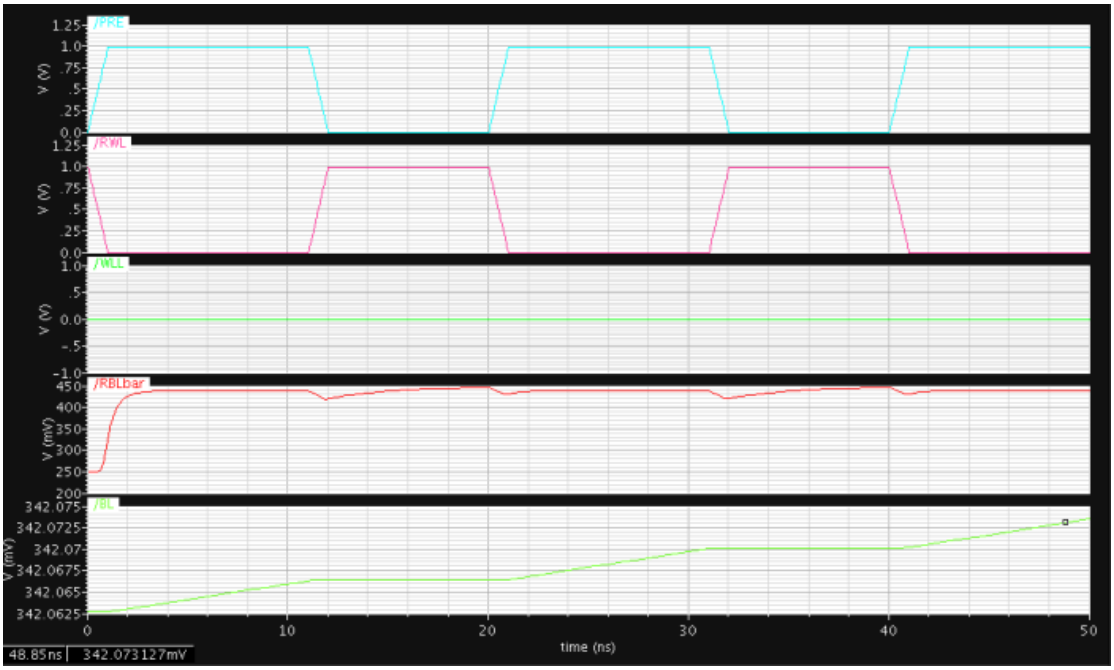

Figure 7: Bit Line Voltage variations during read 0 operation

Table 1: Power Consumptions Values

W/L	Power (mW)	Power (mW)
1	0.0213	0.0922
2	0.0207	0.0814
3	0.0208	0.0802
4	0.0208	0.0768

Conclusion

After implementation of the mentioned design it is observed that the power consumption levels have decreased. Effective levels are achieved by varying the W/L ratio of the tail transistors. Simulation of the design was done using Cadence' Tool and the circuits are optimized using TSMC library based on 90 *nm* technology. The power saving can be calculated from the tabulated values and it hence concluded that since SRAMs are very highly used cells, the above implemented designs help in achieving a lot of power saving in all the fields that this designed is implemented in.

References

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