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Reduced Power and Optimized Switching Activity Multiplier Architecture Design

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Abstract

Based on the idea of partial product reduction, for the design of low power, high performance and switching activity reduction, a new multiplier is proposed. Multiplication plays a crucial role in many of the DSP implementations in multiplying matrices, vectors, IIR filters etc. since it consumes more dynamic power in all applications. Hence for the sake of optimizing the power consumption and the switching activity of the logic circuit, new multiplier architecture has been proposed.Bypassing logic greatly outplays all others in terms of power consumption whereas Wallace tree outplays others in terms of performance. Comparing with array multiplier architecture, mixed style multiplier architecture yields high performance, reduced dynamic power consumption due to the reduced switching activity.

Keywords – Bypassing logic, Wallace tree, mixed style multiplier architecture

Introduction

Now-a-days, power consumption became an emerging factor in designing modern VLSI chips especially with the multipliers. Power is an emerging factor both for environmental causes and to save battery life. Since multipliers occupy more hardware resource and execution time complexity than adders and subtraction. Design based on the bypassing technique focuses on switching power reduction and design based on Wallace tree architecture results gain in the performance speed. So the mixed multiplier architecture results in power saving and switching activity reduction. Comparing with the array multiplier, mixed multiplier architecture highly outperforms reduction in area, power dissipation with increased delay and reduced switching

activity, whereas array multiplier yields low power dissipation with decreased delay. In this technique dynamic power dissipation is more dominant as it is defined as load capacitance charging where is evaluated by the equation $P_{dynamic}= C_L V^2_{DD} E(sw) f_{clk}$ spots C_L is the output capacitance, V_{dd} voltage which is supplied, E (sw) is the switching activity and f_{clk} the clock frequency. There are many optimization techniques that are applied to reduce dynamic power in arithmetic circuits. Subsequently, low power multiplier design is a requisite for the design and application of the effective power optimized resources.

The multiplier design consists of two possibilities. Firstly, trees form, such as Wallace tree, which has the benefits of a logarithmic depth tree. Secondly, is the array form, points it has a linear delay. The well-being of the array multiplier is it is easier to design because of its regular structure, and is easy to fabricate on a chip. The well-being with the Wallace tree is its computation speed, because its depth of the adder chain is highly reduced. Due to these regularities, it plays the prominent IC technologies where performance shows a conspicuous role. These factors have represented the Wallace tree as suitable formerly for high speed applications.

We propose a method in this paper, in order to reduce dissipation of power in the digital multipliers, which focuses greatly on the switching activity. Comparing with the sequential logic one of the most major factor is the gating of clock, where clock is inhibited by the enable signal, thereby isolates any one of the large block in the circuit which results in elimination of switching and the power consumption. Likewise in these combinational circuits the same technique has been used by isolating some unnecessary inputs of specific block by introducing an EN signal as these inputs does not perform valuable computation for the final results which in further does not affect the overall functionality of the circuit called as bypass isolation technique shown in fig 3.

This paper contributes, the computation of a technique same as clock gating which is nothing but isolating some parts of the circuit by bypassing specific modules, when the specific module is being idle, is employed thereby reducing the switching activity. Keeping delay and area overhead bypass switches as major issues; this architecture is carried out using analog switch or electronic relay in the isolation block. Instead of using basic multiplier architecture, we propose a combination of Wallace tree and bypassing logic architecture, results in high performance with less delay and reduced power consumption. Using this modified approach, we can achieve both problems by proposing a logic which performs two architecture one part of the multiplier works by an array structure with bypassing logic, which consumes less power due to the reduced switching. Other part works through a Wallace tree, for better speed improvements than conventional multiplier. In many of the DSP implementations, since the bits of higher order of one or more operands of the multipliers are zero, thereby results improvement in power*delay product. Fig 1 shows the full adder with bypass features cell.

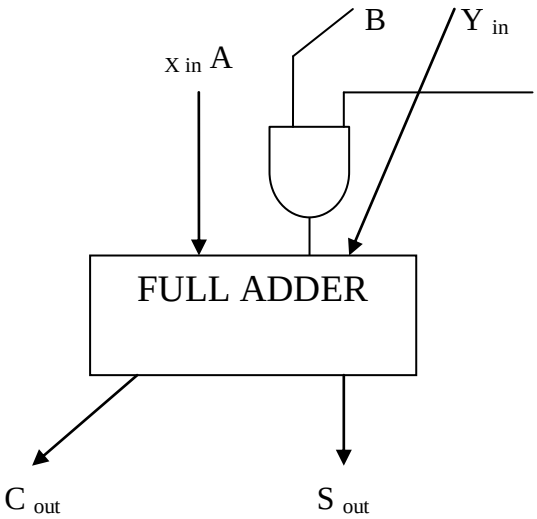

Figure 1: FAB Cell

Wallace Tree Architecture

In this section, we discuss the switching of a multiplier circuit which exhibits effective power consumption. Switching activity is influenced by the great usage of the physical capacitance in the chip and if switching doesn't exist in circuit, there will not be any dynamic power dissipation. Hence, the switching is greatly determined by the data activity. Switching activity can be interpreted as the possibility when transitions occur during power consuming at a specific time, when the circuits does not influence glitching.

The Wallace tree multiplier is substantially faster than a conventional array multiplier since its height in word size is logarithmic, but not linear. It involves three steps for multiplying one or more numbers using Wallace logic,

1. Aggregation of bit products.
2. Minimization of the n number of partial products into a two row matrix using a carry save redundant adder.
3. Addition of last two rows using a faster CLA.

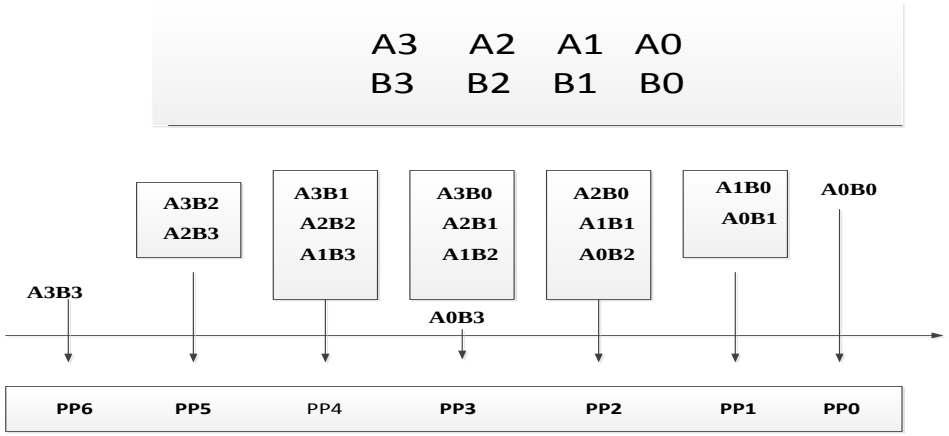

Figure 2: Wallace Tree Operation

The partial product additions are carried out as follows.PP1 and PP4 partial products are calculated using two half adders whereas PP2, PP3, PP4 calculations are carried out using full adders and it finally forms a two row matrix which is fed to a final adder. In such a way the partial products are calculated using Wallace tree to improve the better performance efficiency than other tree architectures. In our proposed architecture, in order to improve the power and delay inefficient, bypassing logic and Wallace tree logic are used. By implementing both architectures better results in power and performance is achieved.

Carry Bypassing Logic

The logic isolation block is nothing but a clock gating in sequential logic, where in combinational circuits it acts as a bypassing switch, inputs of the specific blocks are isolated and is bypassed to the next module thereby reducing the switching activity by using an En signal as shown in fig 3. The novelty is to perform isolation.

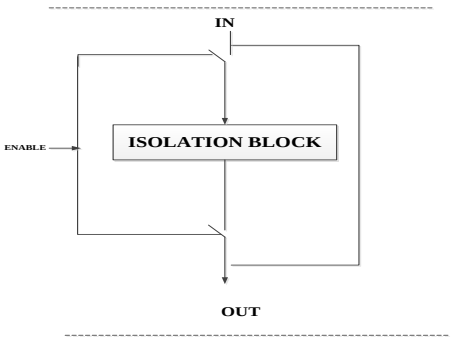

Figure 3: Bypass Isolation Technique

Vector multiplication can easily be implemented through CSA array multiplier. By bypassing the particular block in CS array multiplier for the reduction of the partial

product tree in the form of carry bypass redundant and to transfer the redundancy bits to normal binary form a final chain adder is also used. Here, a 4*4 carry bypass array multiplier is used for bypassing technique, the most advantageous is because of the interconnection topology can easily be implemented, which is similar to clock gating or block isolation method in the power awake devices.

The CS array multiplier functions as follows. Assuming $X = (x_{n-1,\ldots,}x_2,x_1,x_0)$, and $Y= (y_{m-1,\ldots..,}y_2,y_1,y_o)$ are the numbers which are fed into an array by randomly generating the bits of FA*cells that multiplies x_i * $y_j$using transmission gates and finally adds up using a one bit FA, with the carry bits which gives a output sum and carry. The carry bypass array multiplier also called as the vector merging adder is used to give the final result, why we use carry bypass adder is that the carry signal bits are not added instantly rather it is fed to the next phase where the final sum and carries are combined to a propagate adder.

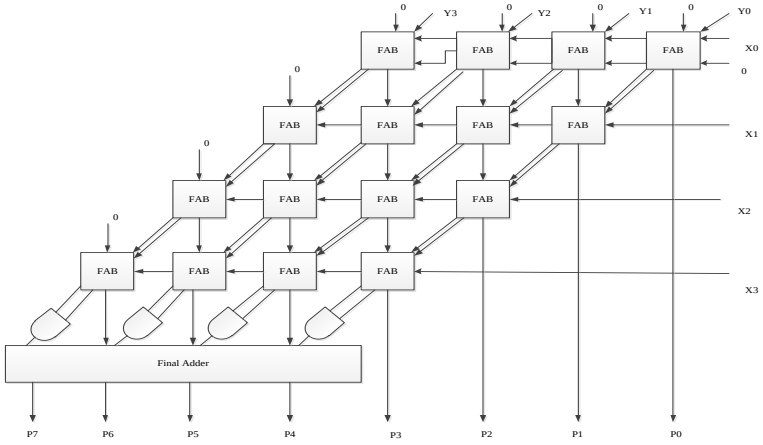

Figure 4: Bypassing Architecture

The simulation result of the bypassing logic structure is shown in fig 5. It greatly achieves the dynamic power dissipation in this architecture where in proposed technique half of the logic is executed by this structure shown above in fig 4.

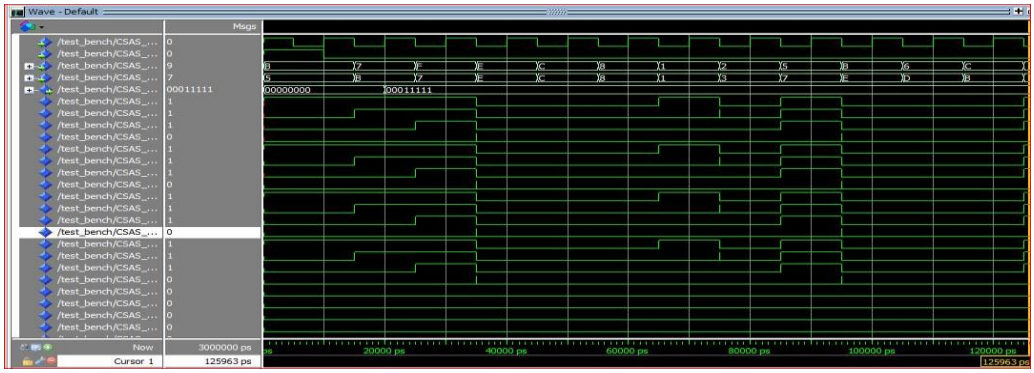

Figure 5: Simulation result of bypassing logic

Mixed Style Multiplier Architecture

As shown in fig.6, two 8 bits are multiplied by dividing it into 4 bits each part and is represented as P,Q,R,S. First 8 bit values are represented as (P,Q) and the second 8 bits are represented as (R,S) .The splitting is done in the form of 2 structures Wallace and Bypass multiplier. Bypassing logic is carried out by multiplying R and S input with Q. The Wallace tree logic is implemented by multiplying R and S input with P .Finally all the outputs are added to produce individual partial products P0-P15.

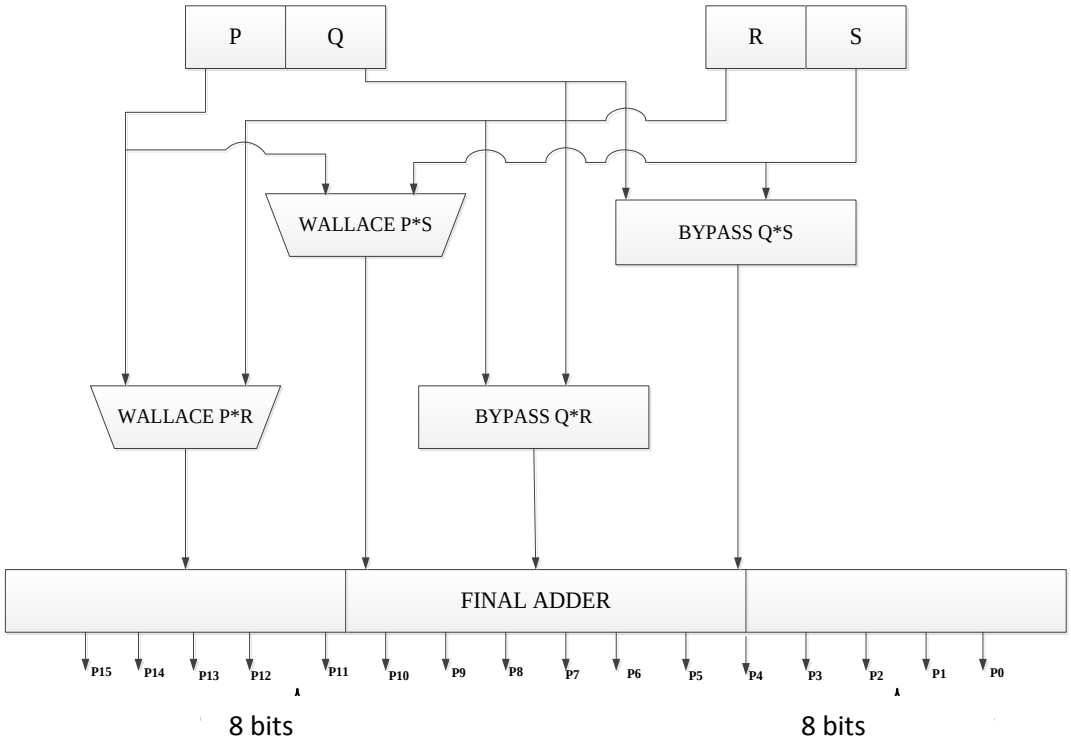

Figure 6: Multiplier Architecture

The major advantage over this approach is the improvement in speed and in effective power savings. Comparing with conventional multiplication, due to its irregular structure it results in great loss of power as well as delay. So, tree approaches are used to overcome the drawback of the conventional one.

Results and Discussion

The mixed style multiplier architecture is simulated using ModelSim and is functionally simulated using Xilinx simulator and the simulation results are shown below.

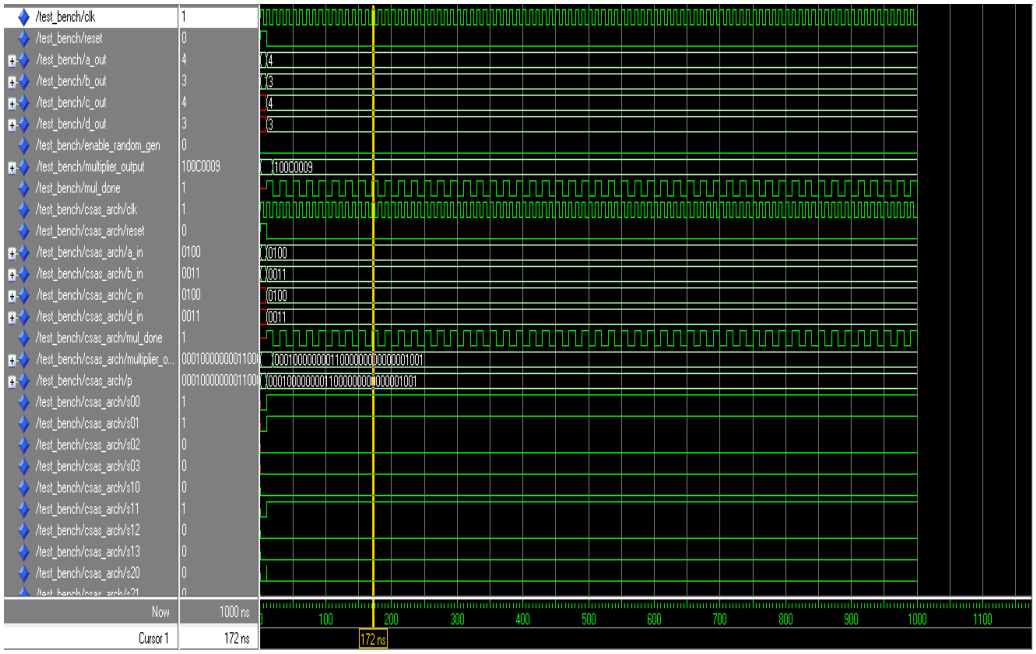

Figure 7: Simulation Results of The Proposed Architecture

The mixed style proposed architecture greatly outperforms the performance and the dynamic power consumption. Experimental results prove the reduction in power, area and the increased performance. The functionality behind this architecture is if one or more operands comprises many 0's than 1's, so that particular half must be passed via bypass multiplier for better power saving. The dynamic power results are shown below in fig 8.

Device	
Family	Spartan3e
Part	xc3s500e
Package	fg320
Grade	Commercial
Process	Typical
Speed Grade	-5

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0

Characterization	
PRODUCTION	v1.2,06-23-09

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.002	1	---	---
Logic	0.001	86	9312	1
Signals	0.001	96	---	---
IOs	0.010	51	232	22
Leakage	0.081			
Total	0.095			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	26.1	82.5	27.5

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.031	0.005	0.026
Vccaux	2.500	0.018	0.000	0.018
Vcco25	2.500	0.005	0.003	0.002

	Total	Dynamic	Quiescent
Supply Power (W)	0.095	0.014	0.081

Figure 8: Dynamic power summary of the proposed approach

Synthesisreport

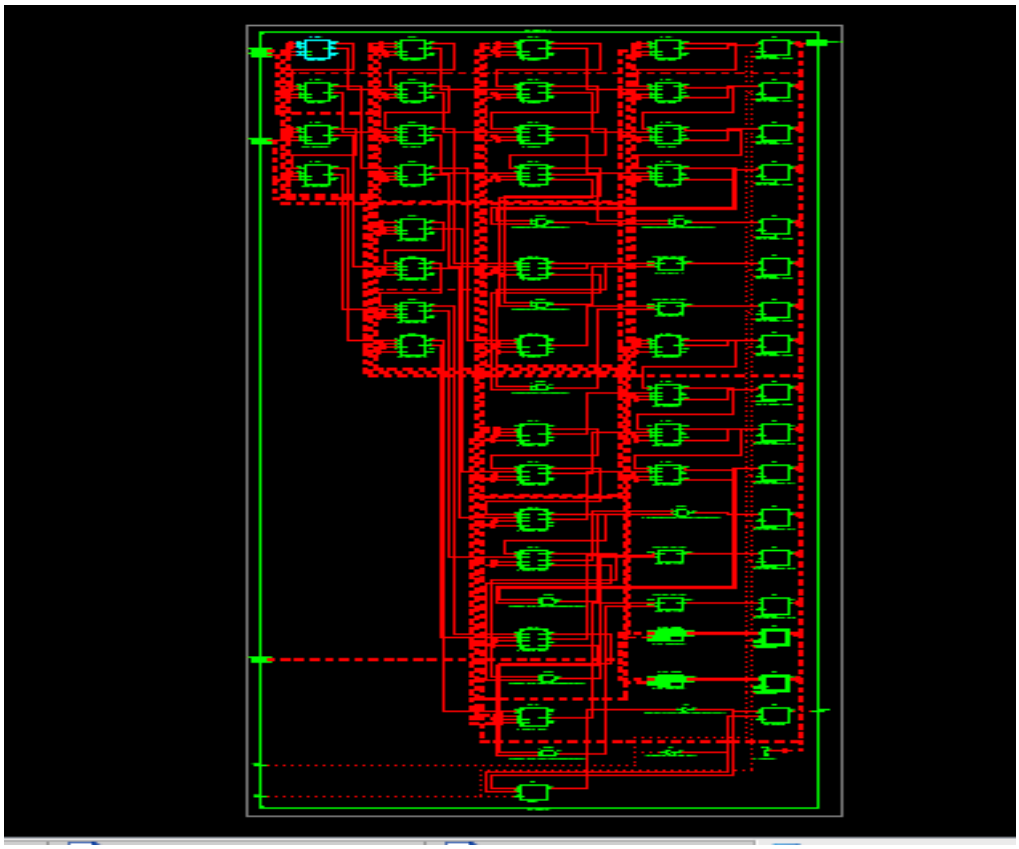

Figure 9: RTL Schematic Of The Proposed Multiplier Architecture

Conclusion

The architectural exploration of the low power and high speed multiplier has been designed in this paper. Bypassing logic and efficient Wallace tree logic and has been evaluated. Finally, bypass technique yields reduction in dynamic power and Wallace logic yields performance improvement which makes ideal for implementing VLSI DSP systems. It can also be implemented by using booth multiplier architecture or other efficient tree structures for further reduction of partial products for obtaining better efficient multipliers.

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