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Hybrid LDPC Decoder For High Error Detection and Correction Applications

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Abstract

In this paper, a low-power high-efficient Hybrid LDPC Decoder Architecture for high error detection and correction applications is proposed. The majority logic circuit is integrated with LDPC decoder in order to reduce the maximum number of errors. The existing architecture requires a large decoding time. For memory applications, this increases the memory access time. The proposed hybrid method detects for errors in a word in the first iteration of majority logic decoding. If no errors are detected, then the decoding stops and remaining iterations are not performed. The scope of this paper is to reduce the decoding latency and hardware complexity by ending the decoding process if errors are not detected. The architecture is synthesized on Xilinx 9.2i and targeted to 90nm device. Synthesis report shows that the proposed architecture reduces the decoding latency and power consumption when compared to the conventional architecture design.

Keywords: Error correction codes, Iterative decoding, Linear code, Parity check codes, Turbo codes.

Introduction

Low density parity-check (LDPC) codes are a class of linear block codes which provide near-capacity performance on a large collection of data transmission and storage channels. LDPC codes have excellent performance for high speed data transmission and low complexity. However, moderate-length or short length binary LDPC codes have been shown to have an early error floor and degraded decoding performance. These codes have been implemented in various standards such as WiMax (IEEE 802.16) and other high speed applications, where parallel

implementations of iterative message-passing algorithms are ideally used in LDPC decoding.

The iterative decoding process of LDPC codes consists of two main steps: 1) To compute independent messages proportional to the aposteriori probability distributions of the code bits; and 2) communicating the messages. The complexity present in both steps depends on the message communication with respect to the process of computing the messages. The communication mechanism for LDPC codes is defined by a pseudorandom bipartite graph and is internal with respect to message computation or internal interleaver, whereas the computational complexity is very low. The complex interconnects and stringent memory requirements in a serial decoder implementation, restricts the LDPC codes to be used in low latency and power-dependent applications.

LDPC codes are suitable for iterative decoding. LDPC implements parallelism in the decoding process thereby achieving high decoding throughput. Several methods on LDPC decoding mainly focuses on floating point arithmetic or infinite precision. However, hardware implementations of the decoding algorithms for LDPC codes must deal with quantization effects in a fixed-point realization.

This paper presents a novel design of LDPC decoder to detect and correct errors in low power applications. The remaining sections are organized as follows: Section 2 exhibits the related works. In section 3, the design of proposed hybrid LDPC decoder is introduced. Section 4 discusses the results of the proposed decoder and section 5 concludes the work.

Related Works

Reference [1] investigated the limits of communication systems with noisy decoders. The author studied the motivation to determine the working efficiency of error control codes when the decoders are faulty. The second reason was to determine the fundamental limits for processing unreliable signals with unreliable computational devices. The results provided an achievability result for reliable memory systems constructed from unreliable components.

An efficient log-likelihood-ratio-based belief-propagation (LLR-BP) decoding of LDPC codes and its reduced-complexity versions have been presented in [2]. Two main approaches for simplified check-node updates by incorporating either a normalization term or an additive offset term in the BP-based approximation were presented. Their results showed that both offset and normalized BP-based decoding algorithms achieved a performance very close to that of BP decoding simultaneously providing advantages for hardware implementation.

Reference [3] proposed high-throughput memory-efficient decoder architecture for LDPC codes based on turbo decoding algorithm. A new merged-schedule merge-passing algorithm was also proposed to reduce the memory overhead of their algorithm for low to moderate-throughput decoders. Moreover, a parallel soft-input–soft-output (SISO) message update mechanism was proposed. Simulation results showed that their algorithm attained a throughput of 1.92Gbps for a frame length of

2304 bits, power saving of 89.13% and 69.83% reduction in silicon area with a reduced interconnect length of 60.5%.

The various methods for constructing Block-Circulant (BC) Reed-Solomon-Based Low-Density Parity-Check (RS-LDPC) codes were investigated in [4]. Their system resulted in a BC form of a parity-check matrix from a random parity-check matrix for RS-LDPC codes. A decoder architecture and switch network for BC-RS-LDPC code was developed based on the new BC parity-check matrix with high performance to demonstrate the efficiency of the technique. Their results showed that the designed decoder consumed 1.3M gates at an operating frequency of 450MHz and achieved a data throughput of 41Gbps with 8 iterations.

The VLSI architectures for LDPC decoders for low power and low voltage applications were studied in [5]. They implemented the algorithm on a bit-serial fully-parallel LDPC decoder fabricated in a 0.13µm CMOS process and evaluated the power consumption. The prototype decoded with 10.4pJ/bit/iteration, whilst performing within 3dB of the Shannon limit at a BER of 10-5 and total throughput of 3.3Gbps.

Proposed Decoder Design

The decoder designed using our method consists of three processing elements-Check Node Unit (CNU), Variable Node Unit (VNU) and Majority Logic Circuit (MLC) as shown in Fig. 1. The CNUs and VNUs are connected through the routing network. The input and output of the check node unit are denoted by the connectivity given by parity-check matrix. The outputs taken from the VNU are given to the MLC after the required number of iterations has been completed. One step Majority Logic Decoding (MLD) corresponds to the decoder for the Euclidean geometry low density parity check (EG-LDPC) code with N=15. First, the data block is loaded into the registers and then the check equations are calculated. If a majority of them has a value of one, the last bit is inverted and all other bits are cyclically shifted. All these operations constitute a single iteration. After N iterations are completed, the bits are in the same position in which they were loaded. Every bit could be corrected only once during the process. A long decoding time is required if N is large. The following properties of check equations have to be followed:

1) All the equations must include variables whose values are stored in the last register [P15 in Fig. 1].
2) The remaining registers are included in at most one of the check equations.

In MLD, if errors are detected in the first few iterations, the decoding process can be stopped without carrying out the remaining iterations. In the first iteration, if at least one of the check equations is affected by an odd number of bits in error, then errors will be detected. In the second iteration, as bits are cyclically shifted by one position, errors will affect other equations such that some undetected errors in the first iteration will be detected. As the iterations progress, all the errors will be ultimately detected.

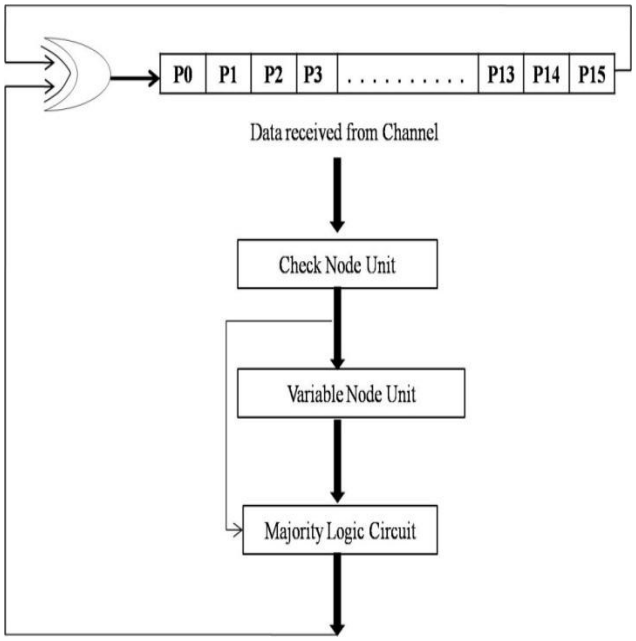


Figure 1: Proposed LDPC Decoder Architecture

Conventional LEDCC decoder

The basic Logic error detection and correction circuit (LEDCC) decoder is a simple but efficient decoder which corrects multiple random bit-flips based on the parity check equations. The LEDCC circuit in Fig. 2 consists of a linear feedback shift registers, majority gate, XOR matrix and XOR for codeword bit correction. The input signal from the linear feedback shift register is shifted from end to end and the intermediate values at each tap are used to determine the results {Bj} of the check sum equations from the XOR matrix.

The output signal is obtained at the final tap as the decoded value of input. The register contents are rotated and the same processes are continued until all codeword bits are processed. It is checked that if the codeword has been correctly decoded, the parity check sum should be zero. Other conventional designs require the number of cycles to be equal to the number of input bits, i.e. number of intermediate taps, which is a major drawback.

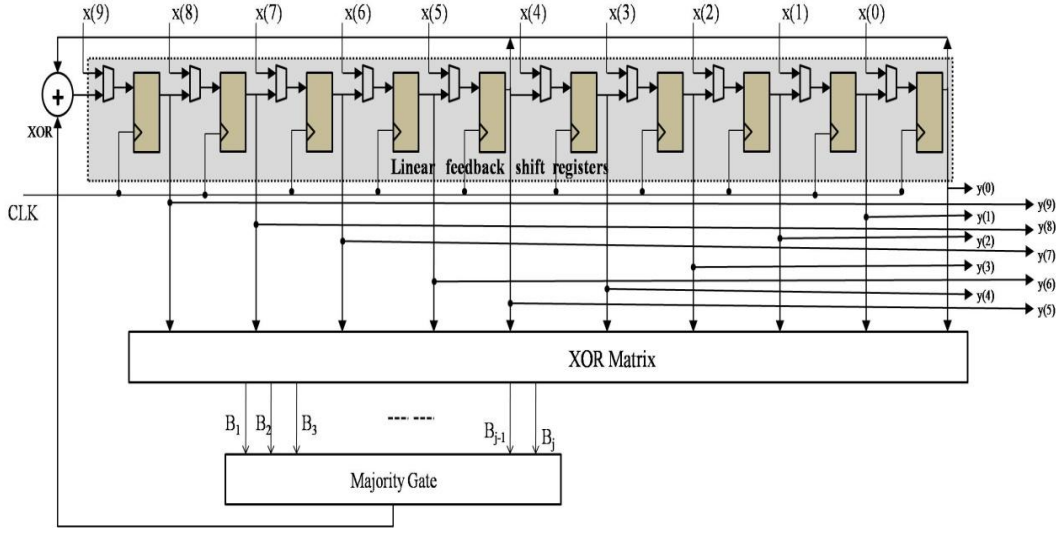


Figure 2: A Basic LEDCC Decoder

Proposed LEDCC Design

The proposed decoder design is depicted in Fig. 3. The designed LEDCC decoder has a linear feedback shift register, a majority gate for bit inversion, an XOR matrix and additionally two blocks—control unit and tristate buffers. The control unit sets a finish flag after the third cycle for no errors detected. The output tristate buffers have high impedance always unless it receives the finish signal from the control unit so that the current values of the shift register are pushed to the output y. The control unit is shown in Fig. 4 and it manages the error detection process.

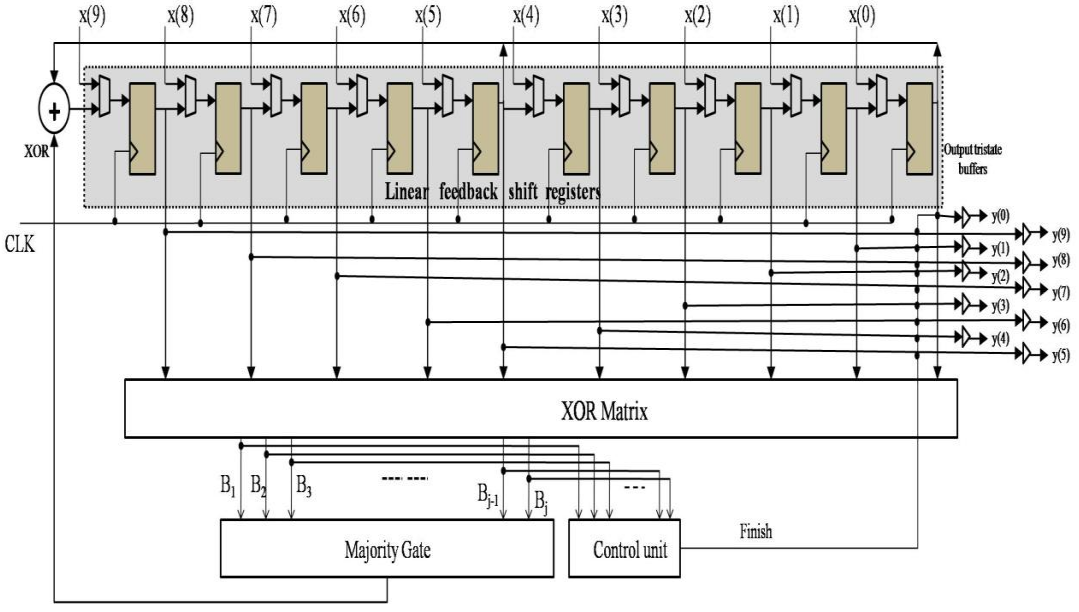


Figure 3: LEDCC decoder with N-tap shifter

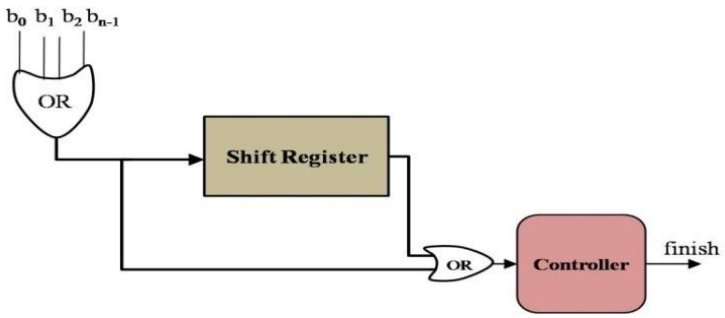


Figure 4: Control Unit

Design of proposed Check Node

The architecture of the check node module of LDPC decoder is shown in Fig. 5. It is used in determining the strength of the received signal against noises in the channel. Four directional difference vectors are calculated with twelve |SUB|, four ADD, and four sorter & concatenator modules. Then, the value of smallest difference is decided by using the sorter & concatenator units. In the proposed design, ADD and subtractor units are required for the design of check node.

Since, the gate count or hardware complexity of one multiplier or division is much more than one adder or subtractor unit, all multipliers or divisions are replaced by adder or subtractor unit, thereby reducing the hardware cost.

After addition and subtractions are determined on received sequences, the sorting and concatenation (Fig. 6) is performed over these sequences in order to compute the response of the check node unit in LDPC decoder. Each check node block produces 6 bit length of sequence and thus it produces 24 bit length sequence.

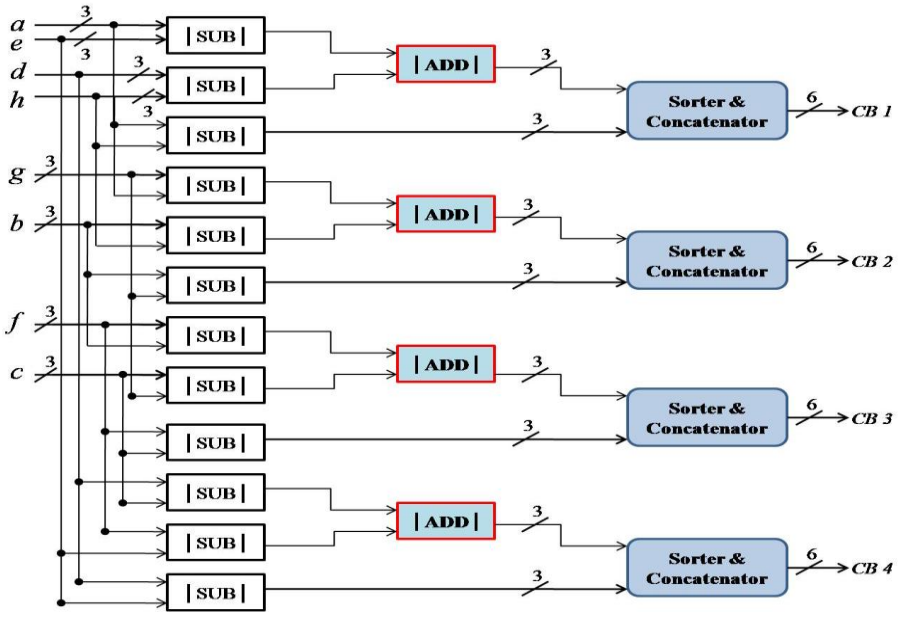


Figure 5: Check Node Architecture

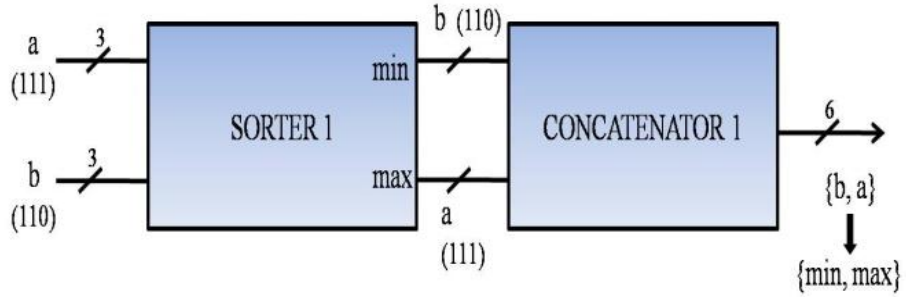


Figure 6: Internal of Sorter & Concatenator Unit

Design of Proposed Variable Node

The variable node unit architecture shown in Fig. 7 computes the hard decision vector x. This vector is routed through the routing network to the check node block (CNB). The routing between two nodes has single-bit value and the routing network size is smaller compared to that used in sum product algorithm. The variable node processor unit is comprised of a flip-detection circuit, line buffer, multiplexed adder and concatenator. Initially the received signal y from check node unit is fed to the Variable node block (VNB) through a register-feedback assembly. The received values are 6-bit signed-magnitude (SM) values. Let $[sn : mn]$ be n^{th} 4-bit value provided to the n^{th} VNB, where sn denotes hard decision value and mn denotes the magnitude of the same.

The SM makes the correlation calculation simple to be implemented. The correlator circuit consists of an inverter followed by a 1-bit multiplexer. The proposed VNA unit consists basic multiplexer, line buffer, summer and concatenator modules. The block datas received from CNU unit are divided in to four subblocks. The first three submodule blocks are processed by adder module and last submodule block is processed directly by multiplexer unit. The control signal for multiplexer module acts as a select line in this unit, which is generated and illustrated in Fig. 8.

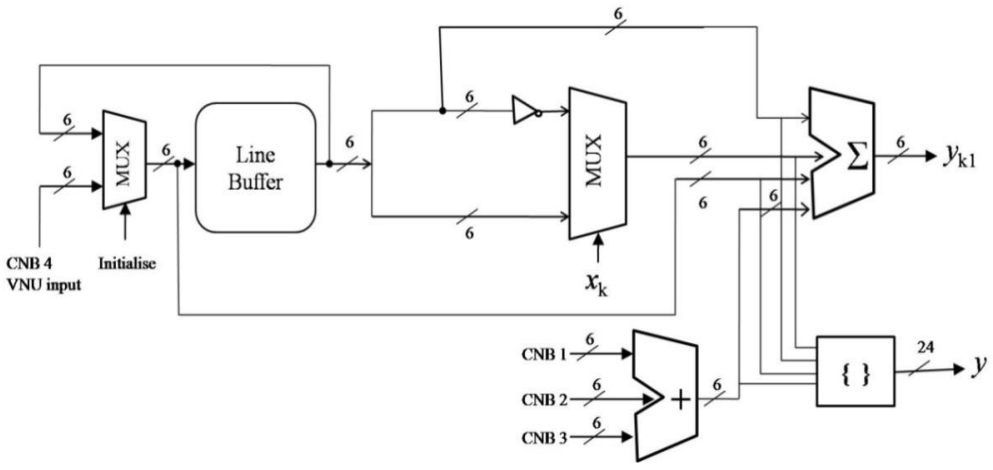


Figure 7: Variable Node Architecture

Fig. 8 explains the generation of control signal (x_k). The signed bit input is applied to the shift operator. The multiplexers and line buffers help in producing the control signal, which is fed to the VNU. The use of simple computational methodologies along with less row and column weights reduces the operations thereby, resulting in significantly less power consumption.

The subtraction unit receives six bits from variable node architecture and line buffer unit and thus produces single sign bit which satisfies the following constraint:

x_k =1 if (y_{k1}-output of line buffer) ≥0 (1)

x_k =0 if (y_{k1}-output of line buffer) <0 (2)

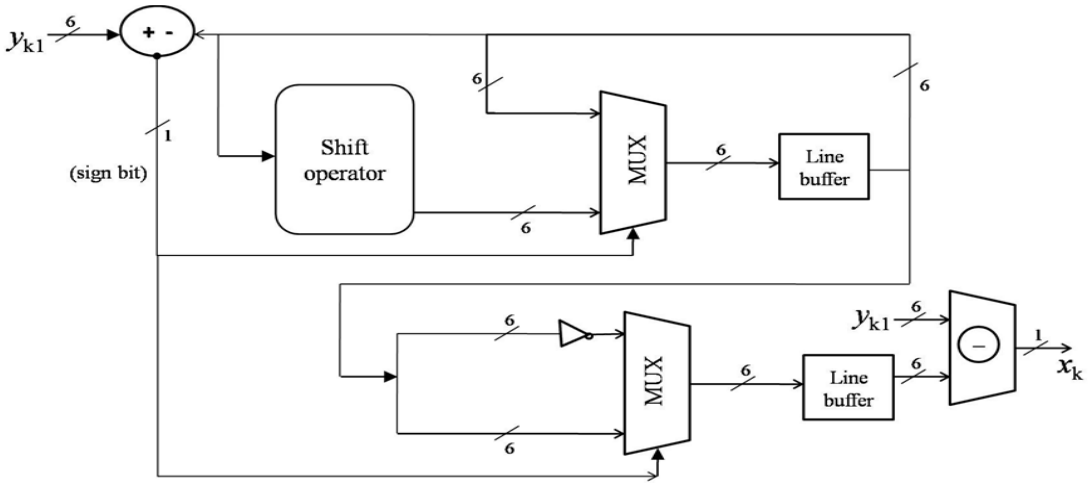
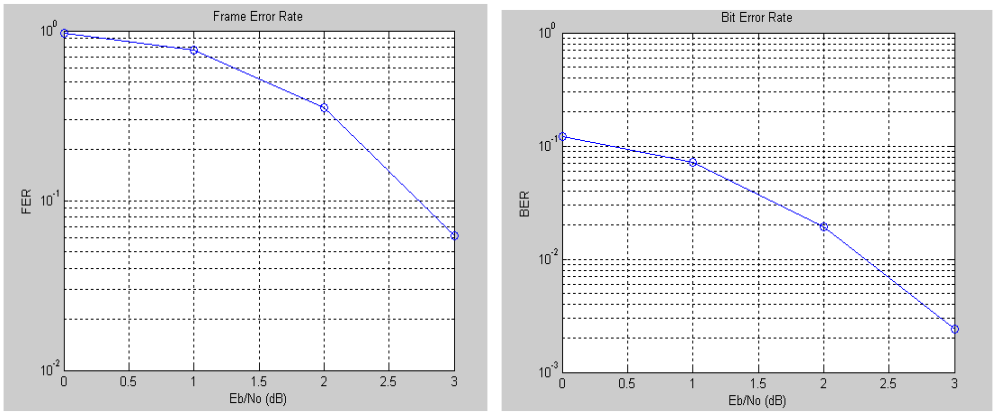


Figure 8: Generation of control signal x_k

Results and Discussions

A number of performance evaluation and resource utilization parameters are determined for the proposed LDPC decoder. The present research is focused on the design and development of pipelined LDPC decoder for low power applications. The simulation results shown in Fig. 9 illustrates the relationship between SNR (Signal to noise ratio)–FER (Frame error rate) and SNR–BER (Bit error rate).



(a) (b)

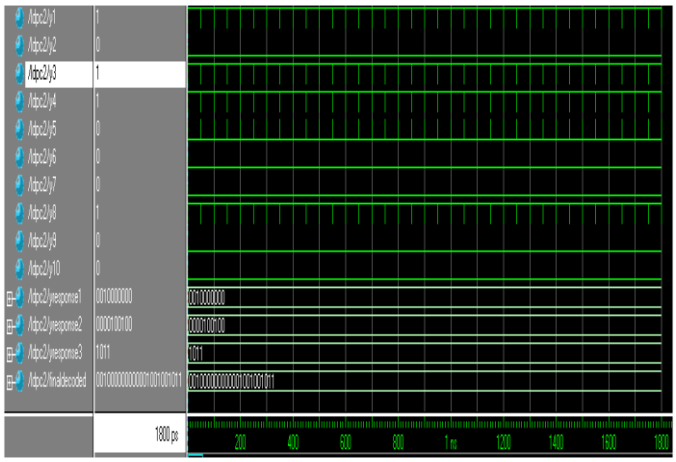
Figure 9: Result showing plot between (a) SNR and FER, (b) SNR and BER.

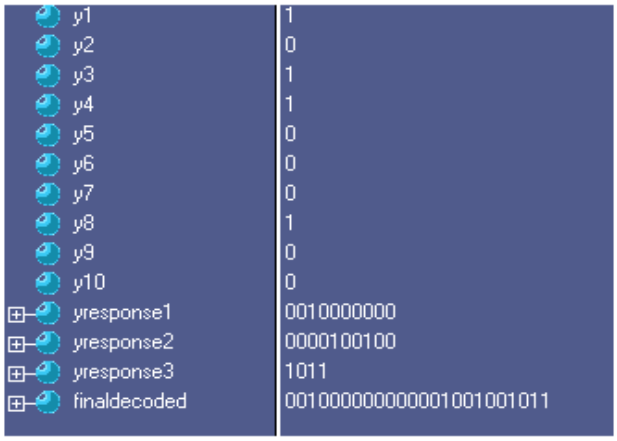
In Fig. 10, the variable count1 indicates the maximum number of errors detected in the received code words. In this work, the maximum number of detectable errors in the received code word is 4. The RTL schematic view and Technology schematic view and the Chip layout of proposed LDPC decoder IC are shown in Fig. 11.

The parameters considered for investigation include number of slices (S), number of LUT's (Look up table), Slice latches (SL), gate counts (GA), Power consumption (PC), and Area Utilization. All these parameters are tabulated in Table 1 and graphically plotted in Fig. 12.

Table 1: Performance Analysis of Hardware Utilization

Performance parameters	**Proposed Architecture**
Slices	56
LUTs	100
Gate Count	2304
IOBs	48





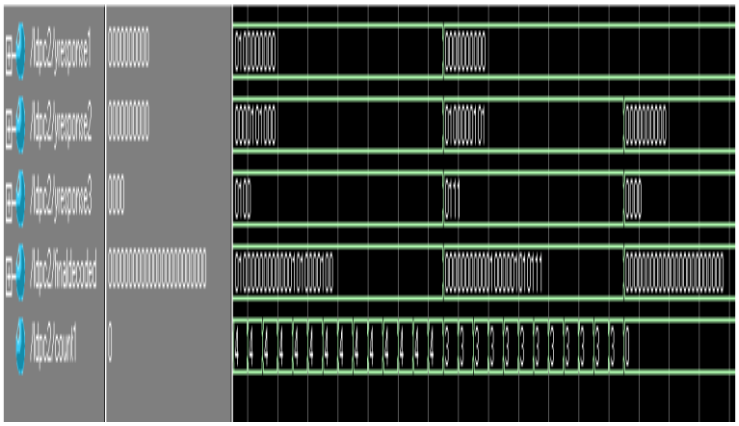
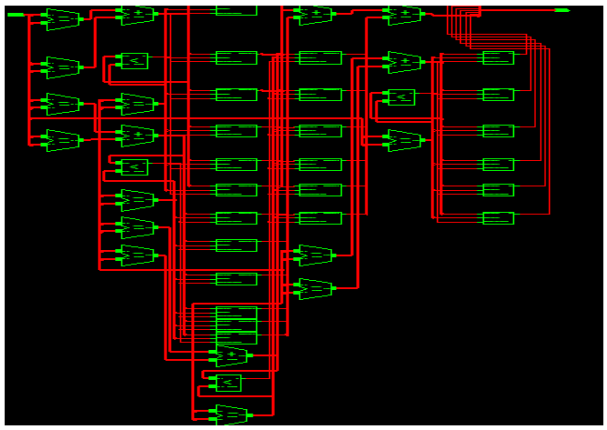
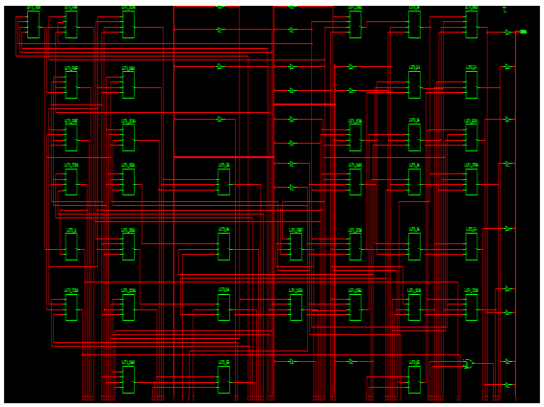


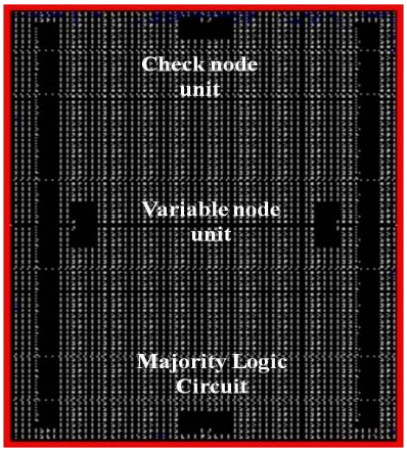
Figure 10: Error Detection Process In Proposed Method



(a)



(b)



(c)

Figure 11: Simulation results of proposed technique. (a) RTL schematic view, (b) Technology schematic view and (c) Chip layout of proposed decoder IC.

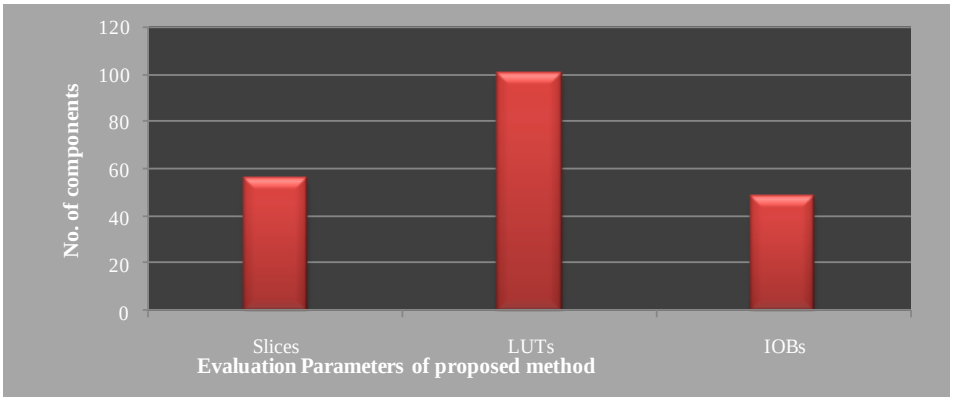


Figure 12: Graphical Plot of Hardware Utilizations

The proposed LDPC decoding architecture is synthesized using Xilinx project navigator version 9.2i tool. The proposed architecture provided decoding latency of 28ns for both check node and variable node implementation.

Sangmin *et al*. (2013) [8] achieved the decoding latency about 16.32ns whereas Spagnol *et al*. (2009) [9] achieved decoding latency about 50.05ns.The proposed LDPC architecture is performed as superior in this way. Also, the proposed architecture consumed 4-input LUTs about 100. Sangmin *et al*. (2013) [8] consumed 6422 LUTs and Spagnol *et al*. (2009) [9] consumed 12924 LUTs with respect to their various designing methodologies. The various comparisons of proposed technique in terms of several parameters are illustrated in Table 2, Table 3 and Table 4.

Table 2: Performance Comparison in terms of Latency and LUTs

Methodology	**Decoding Latency (ns)**	**LUTs**
Proposed	16.32	100
Sangmin kim *et al*. (2013) [8]	56.36	6422
Spagnol *et al*. (2009) [9]	50.05	12924

Table 3: Performance Comparison of Spartan and Virtex Families

Family	**Power Consumption (mW)**	**Latency (ns)**
Spartan	81	16.32
Virtex	151	17.72

Table 4: Performance Analysis based on Error Detection and Correction

Methodology	**Error detecting capabilities**	**Error correcting capabilities**
Proposed work	4	4
MLDD (Liu *et al*.) [6]	3	3

Conclusion

The hybrid LDPC architecture integrated with majority logic algorithm is proposed in this paper. The proposed Hybrid Architecture detects and reduces the maximum number of errors in the received code words. The simplified architecture for variable and check node is designed for low power applications. The simulation and synthesis result shows that the proposed hybrid LDPC Architecture consumed 16.32ns of decoding latency which reduces the decoding latency rate about 28.9% whereas compared with conventional methods.

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