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VLSI Implementation of Optimized Carry Select Adder

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Abstract

In many DSP and microprocessors where arithmetic operations are performed speed becomes a challenging task. The carry select adder (CSLA) is the fastest of all the other conventional structures, though there is an increase in the area and the power consumed. To reduce the area and power, here two efficient designs of carry select adder are introduced using simple gate level modification. Here, modified Half adder and Full adder circuits are used along inside the proposed designs which further reduces the area, delay and power consumption of the CSLA. Based on the proposed designs, 32 bit CSLA are designed and compared. The entire architecture is designedusing VHDL, simulated using ISim and synthesized using Xilinx ISE 13.2.

Keywords: low power; area; delay; adder; CSLA.

Introduction

The demand for portable and mobile devices are going on increasing, so area and power-efficient high-speed logic systems have become one of the most significant areas of research in VLSI system. An efficient arithmetic processing unit with optimized performance parameters such as speed, power and area is substantial for the

design of an efficient area and power efficient high speed VLSI architecture. Adders are the main components of arithmetic unit. So in order to make an efficient arithmetic unit an optimized design of adder is a must. Adders act as a crucial part in many digital signal processors and microprocessors. So the design of an efficient adder leads to efficient processors and devices.

A lot of researches are going on in the area of optimizing adder parameters. In a conventional adder (ripple carry adder) the area and power consumption is less, but it has a very high delay. So in order to reduce the delay and make a faster design several adders was proposed. One of such adder which is having the fastest design is carry select adder (CSLA). A conventional carry select adder [1] is having a double RCA structure that produces a pair of sum and output carry words corresponding to C_{in}=0 and C_{in}=1. And the output is then selected with the help of the multiplexer. Though the CSLA is having a lower delay, the area and hence power consumption gets doubled compared to ripple carry adder.

A number of attempts have been made to reduce the area and power consumption in CSLA. A carry select adder generating carry of block with carry in as 1 from the block with carry in as 0 was proposed by Tyagi.A[2] in 1990. Later in 1998, T.Y.Ceiang and M.J.Hsiao[3] proposed a carry select adder consisting of a single ripple carry adder. This was a real breakthrough in the carry select adder history. Later in the year 2005 a further modified carry select adder which reduces the area and power consumption was proposed by Amelifard B, Fallah F and Pedram M[4]. It reduces the gap between carry select adder and ripple carry adder. Kim and Kim [5] reduced the dual RCA structure by using one RCA and an add-one circuit, where he used multiplexer for implementing the add-one circuit. The add-one circuit here replaces the RCA with C_{in}=1. A low power and fast carry selct adder was proposed in [13]. Here a transistor level modification is carried out for reducing the power consumption. Another fast and low area carry select adder circuit was proposed [12]. This design employs an incrementer instead of logic adder circuit, which makes it fast and low area consuming design. Ramkumar and Kittur [7] proposed a binary to BEC based carry select adder. It reduces the number of logic resources used, but has a higher delay than conventional CSLA. Heetal [6] suggested a Square root CSLA(SQRT CSLA) for implementing large bit width adders with less delay. Here the CSLAs having different bit widths are cascaded in an ascending order of bit size. This design, thus helps to reduce overall delay by providing a parallel path for carry propagation. A common Boolean logic (CBL) based CSLA was also proposed [8]. This design consists of lesser logic resources, but was having a larger carry propagation delay, almost equal to that of RCA. In order to overcome this, a SQRT-CSLA using CBL was proposed in [9]. But this design requires more resources and delay than BEC based SQRT-CSLA [7]. Further a new design with less area, power, delay and data dependency was proposed [10]. This design involves less logic resources and less carry propagation delay. An adder circuit using koggestone adder and simple logic circuit was proposed in [11]. This design is faster, but consumes more area.

This paper proposes two new CSLAs. The basic idea of this paper is using anAND-OR-INVERTER logic circuit for the implementation of XOR gate which in turn reduces the area consumed. This logic circuit is used here for implementing efficient

half adder, full adder and CSLA. Section 2 discusses about the existing CSLA. Section 3 covers the comparison of existing XOR gate, half adder and full adder with the modified xor gate, half adder and full adder. In section 4 we discuss the two proposed CSLAs using these modified adders.

Existing Method

In [10], one of the most efficient CSLA designs interms of area, delay and power is described. This system was designed by comparing the conventional CSLA with BEC based CSLA and reducing all the redundant terms. The block diagram of existing CSLA is given in fig 1. Thus, this design reduces the number of logic gates and also the carry propagation path.

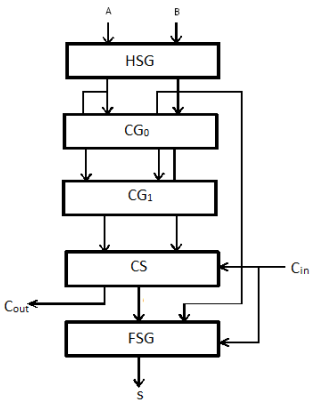


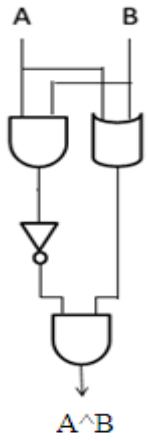
Figure 1: Existing CSLA

Now by analyzing this adder closely, we can get to know that there are some methods which can be used to reduce the three parameters (area, power and delay) than this existing method.

Thus, here two new designs with optimized area,delay and power performance are proposed.

Modified Half Adder and Full Adder

The main idea of this work is to use a modified XOR gate instead of a normal XOR gate. Normal XOR gate consists of two NOT gates, two AND gates and an OR gate. The modified XOR gate is implemented using two AND gates, one or gate and one not gate. The logic circuit modified XOR gate can be shown in fig 2



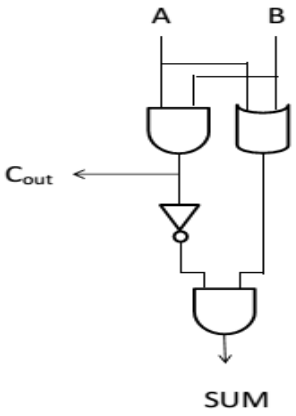


Figure 2(A): Modified XOR Gate **Figure 2(B):** Modified Full Adder

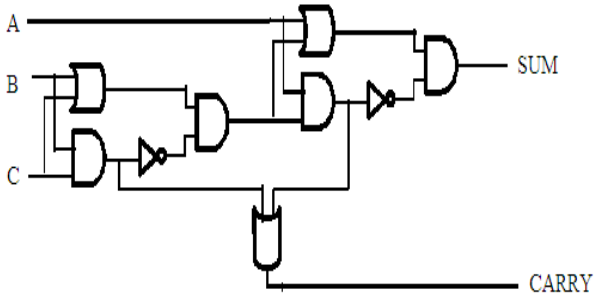


Figure 2(C): Modified Full Adder

The logic can be explained easily using the logic expression. The equations are as follows:-

$$A \wedge B = AB' + A'B \quad (1)$$

This design requires two NOT gates, two AND gates and one OR gate. The same logic gate is implemented here by using the logic

$$A \wedge B = (AB)'(A+B) \quad (2)$$

This design uses one NOT gate, two AND gates and one OR gate. Thus, one NOT gate usage is reduced here. This expression also gives the same output as xor gate output. ie.,

$$AB' + A'B = (AB)'(A+B) \quad (3)$$

The second xor gate design is more suitable for implementing low area half adders and full adders. While using this xor gate for half adder design, the carry output can also be taken from the xor circuit itself. Thus the need additional AND gate is reduced. A normal half adder consist of 3 AND gates, 2 NOT gates and 1 OR gate. But in

modified half adder a total of 2 AND gates, 1 NOT gate and 1 OR gate is only needed. Thus a reduction of 1 AND gate and 1 NOT gate is achieved by using this half adder circuit instead of the normal half adder.

Similarly for a full adder design, instead of various full adder configurations normally used, the full adder circuit using two modified half adder along with an OR gate is used as shown in fig. This design can be verified by logic equations of full adder. The logic equation of a normal full adder can be given as:-

$$SUM = A \wedge B \wedge C \quad (4)$$

$$CARRY = AB+AC+BC \quad (5)$$

The logic equation for modified full adder can be given as:-

$$SUM = A \wedge B \wedge C \quad (6)$$

$$CARRY = AB + (A \wedge B)\, C \quad (7)$$

This adder design uses the lowest number of logic gates than other full adder designs. Also, this design is having a low delay too. Here a full adder uses 4 AND gates, 2 NOT gates and 3 OR gates only. Thus a reduction of the number of gates is achieved by using this full adder.

Carry Select Adder With Modified Adder Circuits

A. Modified Half Adder Based Carry Select Adder (MH-CSLA)

Area-delay-efficient carry select adder is one of the most efficient carry select adder. This adder has reduced all the redundant logic and thus reduced the delay and area consumption of the adder. Here the carry selection is done prior to the full sum generation. Thus, this circuit is very much suitable for SQRT-CSLA implementation for large bit addition.

Now by replacing the logic circuits in this area-delay-power efficient carry select adder using the modified xor gate and modified half adder circuit we can reduce the total area consumption. Here the area reduction is done without causing any variation in the delay. Thus, this circuit maintains the lower delay of the area-delay-power efficient carry select adder and also reduces the area and power consumption too. Thus, for each bit adder section, we will get a reduction of 1 AND gate and 2NOT gates. The logic expression for the MH-CSLA can be given as:-

$$S_0(i)=A(i) \wedge B(i) = (A(i)\, B(i))' \, (A(i) + B(i)) \quad (8)$$

$$C_0(i)=A(i)\, B(i) \quad (9)$$

$$C_1^0(i)=C_1^0(i-1)\, S_0(i) + C_0(i) \text{ for } (C_1^0(0) =0) \quad (10)$$

$$C_1^1(i)=C_1^1(i-1)\, S_0(i) + C0(i) \text{ for } (C_1^1(0) =1) \quad (11)$$

$$C(i) = C_1^0(i) \text{ if } (Cin=0) \quad (12)$$

$$C(i)=C_1^1(i) \text{ if } (Cin=1) \quad (13)$$

$$C_{out}= C(n-1) \qquad S(0)= S_0(0) \wedge C_{in} \quad (14)$$

$$S(i) = S_0(i) \wedge C(i-1) \quad (15)$$

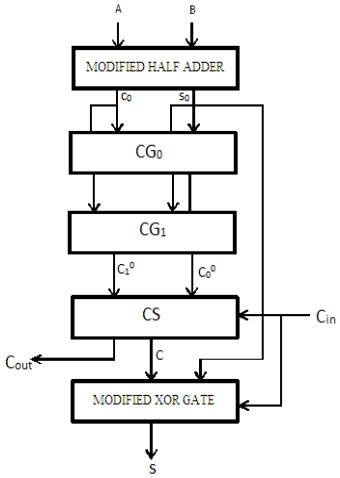


Figure 3(a): MH-CSLA architecture

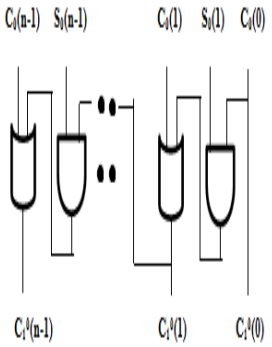


Figure 3(b): carry generation for C_{in}=0

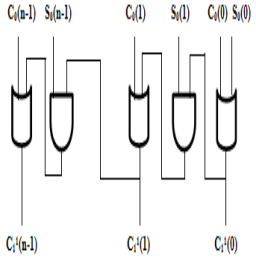


Figure 3(c): Carry Generation for C_{in}=1

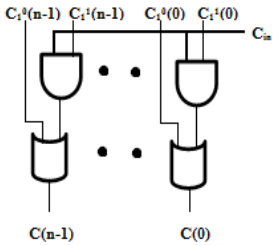


Figure 3(d): Carry Selection

The fig 3(a)-3(d) shows the circuit diagram of the MH-CSLA. Here CG_0 and CG_1 together forms carry generation unit.CG_0 gives the carry output for C_{in}=0 and CG_1 gives the carry output for C_{in}=1. The carry selection section selects the required carry corresponding to the C_{in} provided.

B. Reconfigured Carry Select Adder (R-CSLA)

Here a new implementation of carry select adder is done. Unlike the conventional carry select adder, here the RCA with C_{in}=0 is implemented using the modified full adder circuit instead of the normal full adder. Also the RCA with C_{in}=1 and MUX is replaced using the modified half adder section. The modified half adder section, thus provides carry propagation through minimal logic gates and also the sum calculation too is done with less logic gates. Thus, this design reduces the delay of carry propagation and also the total area and power consumption are also reduced.

The logic expression for R-CSLA is:-

$$S_0^0 = A_0 \wedge B_0 \qquad C_0^0 = A_0 B_0 \quad (16)$$

$C_0=C_{in}$ $S_0= S_0^0 \wedge C_0$ (17)

$C_1= C_{in}\, S_0^0$ $S_1^0=A_1 \wedge B_{11}$ (18)

$C_1^2=A_1B_1 + S_1^0\, C_0^0$ (19)

$S_1^1=S_1^0 \wedge C_0^0$ (20)

$S_1=S_1^1 \wedge C_1$ $C_2= S_1^1\, C_1$ (21)

$S_n= S_n^1 \wedge C_n$ $C_n= S_n^1 C_1$ (22)

$C_{out}=C_n \wedge C_n^2$ (23)

The block diagram of R-CSLA is given in fig 4. This design uses modified half adder and modified full adder sections.

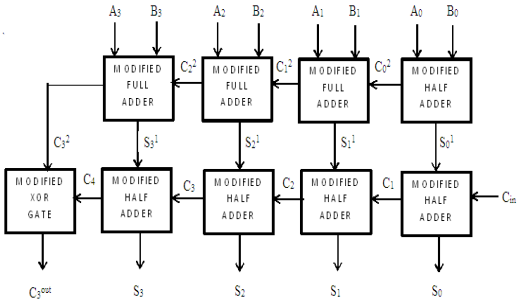


Figure 4(a): R-CSLA architecture

Area Evaluation

The area of various adders can be compared with the help of number of gates in the design. More the number of gates means more the area. So a comparison of the area of different carry select adders is shown in table1.

Table 1: Area Comparison of Different Adders

Design	No.of AND gates	No.of OR gates	No.of NOT gates
Area-delay-power efficient CSLA	8n-2	5n-1	4n
MHA CSLA	7n-2	5n-1	2n
R- CSLA	6n	4n-1	3n

The fig 3 gives a clear picture of the area consumption of the CSLAs. The proposed CSLAs consumes less area than the existing CSLAs. It is clear from the graph that difference in the area (number of gates) gets increased as the number of bits increases. Here both MH-CSLA and R-CSLA are having less number of logic gates than existing area-delay-power efficient CSLA. Also, R-CSLA is having least gate count when compared with the-CSLA is more suited for low area applications.

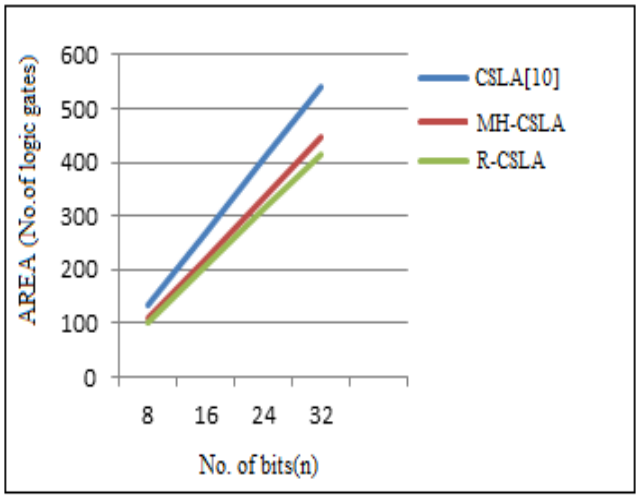


Figure 4(a): Area comparison of CSLAs

Performance Comparison

A 32 bit adder of the existing and the two proposed systems were designed using VHDL, synthesized using Xilinx 13.2 and simulated using ISim. The synthesis and simulation show that the proposed CSLAs are having lower area, delay and power than the existing CSLA. The simulation result and area evaluation help to obtain the comparison as in table 2.

Table 2: Performance Comparison of Various CSLA

Design (32-bit)	Area (No.of Gates)	Delay (ns)	Power (W)	ADP (10^{-6})	PDP (10^{-9})
Area-delay-power efficient CSLA	541	34.319	3.378	18.566	115.9295
MH-CSLA	445	34.173	3.378	15.206	115.4343
R-CSLA	415	30.362	3.362	12.600	102.077

From the above table, the area, power and delay of the proposed designs are reducedthereby increasing its efficiency.

The ADP comparison of the three models is shown in fig 5. The ADP is reduced in both the proposed systems and of all the three methods R-CSLA has the lowest value.

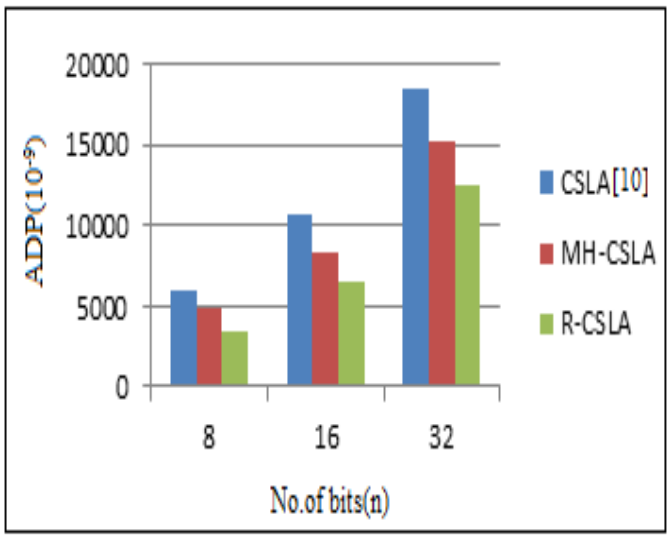


Figure 5: Comparison Of Area-Delay-Product(ADP)

Conclusion

The two new designs of CSLA proposed here have an implementation of a modified half adder and modified full adder circuit. The output shows that the adder area, power consumption and delay are reduced when compared with the existing ones. This method even gives an appropriate substitution for current CSLA in terms of area, power consumption and delay. When the proposed designs were compared R-CSLA has a lower value than MH-CSLA, thus can be used for implementing various low power devices with low area and delay.

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