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A 4.2ppm/°C Temperature Compensated CMOS Voltage Reference

[1]Paulcy Paul, [2]N.Kayalvizhi
[1]Student-Department of ECE, Amrita Vishwa Vidyapeetham University, Coimbatore
[2]Assistant Professor-Department of ECE, Amrita Vishwa Vidyapeetham University, Coimbatore

Abstract

A voltage reference circuit compatible with latest CMOS standards and temperature stability was developed using 90nm CMOS technology. The circuit includes CMOS transistors operating in saturation and triode regions, without the aid of resistors, diodes and bipolar transistors. In a band gap voltage reference circuit, the temperature independent reference voltage is attained by the base emitter voltages of the bipolar transistors used. In the proposed circuit these bipolar transistors and resistors are replaced by ratioed MOS transistors. The CMOS transistors were biased and designed in such a way that the temperature dependencies of mobility and gate oxide were nullified. The circuit was developed for a constant reference voltage of 1.03V with a temperature coefficient of 4.2ppm/°C, over a range of 0-160 °C. The circuit was operated with a supply voltage of 1.8V and draws a maximum value of supply current as 9.05μA and maximum power dissipation was 77.73μW.

Keywords: CMOS Voltage reference; Band Gap Reference circuit; Temperature Compensation; Temperature Coefficient.

Introduction

Stable Voltage references are required in most of the low-voltage application circuits in order to provide output voltage stability against temperature variations and transitions in supply voltage. But the large consumption of power and silicon area by Bipolar Junction Transistors (BJT) and resistors in Band Gap voltage Reference circuits (BGR) made incompatible in low power application [1]-[3]. Meanwhile, the curvature compensated BGR circuit recognizes exponential curvature compensation in temperature range and gaining a reference voltage of 3.6V through less number of BJT structures [4].

As a replacement of BGR circuits, [5] presented a temperature insensitive voltage reference on the basis of joint temperature compensation of the threshold voltages of nMOS and pMOS transistors and shows a significant reduction in temperature relation of mobility with no usage of subthreshold characteristics. Although, the usage of BJTs have been replaced by the MOS transistors in [5], the presence of resistors resulted in occupying large silicon area. As an alternative, a resistorless circuit with mutual compensation of thermal voltage (V_T) and threshold voltage (V_{th}) can be employed. Two linear dependent temperature terms, i.e., V_T and V_{th}, are used to obtain a low-temperature-reliant voltage reference circuit with a significant reduction of nonlinear temperature dependent parameters [6]. The variation of carrier mobility to temperature can be reduced by MOSFETs in subthreshold state with different V_{th}. Additional fabrication steps are needed to make MOSFETs with different threshold voltages.

Inspite of, a CMOS voltage reference having a voltage supply less than 1 V in low-voltage action, [7] still gains a low temperature coefficient which results in a zero temperature dependence of carrier mobility using a channel length of 350nm. Based on the sizing of the CMOS transistors, inorder to achieve a high precision temperature compensated voltage reference circuit, the base emitter voltages and resistors are replaced with the gate source voltages of MOS transistors that are working in subthreshold region. The size ratio of resistors are replaced by the size factor K_1/K_2, K being the width to length ratio of MOS transistor [8]. The temperature dependent parameters of the circuit are the threshold voltage and the drain-source voltages of the MOS transistors. The detailed explanation behind modeling a low temperature sensitive circuit is explained in section **2**.

Principle of Proposed Voltage Reference

From the basic idea of band gap reference, the reference voltage (V_{ref}) is obtained as a function of V_{BE} and $\alpha\Delta V_{BE}$, where α is the proportionality factor which is represented as ratio of resistors. Thus for a complete CMOS circuit, the above BJTs and resistors were replaced with appropriate MOS transistors.

The positive temperature coefficient term $\Delta V_{BE}$is replaced by ΔV_{GS} between two CMOS transistors operating in subthreshold region [9].Thus the skeletal equation for V_{ref} can be obtained as follows

$$V_{ref} = V_{th} + \frac{K1}{K2}\Delta V_{GS} \tag{1}$$

where K is the aspect ratio of the CMOS transistors used.

The I – V relationship of MOS transistors in saturation and triode regions are expressed as

$$I_{sat} = \frac{\mu C_{ox} K}{2}(V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \tag{2}$$

$$I_{triode} = \mu C_{ox} K \left[(V_{GS} - V_{th})V_{DS} - \frac{1}{2}(V_{DS})^2\right] \tag{3}$$

where, μ is the mobility of electrons inside the channel, C_{ox} is the oxide capacitance per unit area in the gate region and λ is the coefficient of channel length modulation.

Among the above parameters, those which have large sensitivity towards temperature are μ, V_{th} and C_{ox}.Thus by adjusting these parameters with low sensitivity to temperature, the temperature compensation can be achieved. While *K* and λ are temperature independent constants.

The primary temperature dependent parameter is the threshold voltage, V_{th} [10] which has a negative temperature dependency as the following relation

$$V_{th}(T) = V_{th0} - \alpha_{V_{th}}(T\text{-}T_0) \tag{4}$$

where *T* is the absolute temperature, V_{th0} threshold voltage at nominal temperature T_0 and $\alpha_{V_{th}}$ is the temperature coefficient of the threshold voltage [11].

The relation between mobility and temperature can be represented as [11]

$$\mu(\mathrm{T}) = \mu_0 \left(\frac{T}{T_0}\right)^{3/2} \tag{5}$$

where *T* is the absolute value of temperature, μ_0 is the mobility at minimal value of temperature T_0 and α_μ is the temperature exponent of mobility.

In order to generate the reference voltage, a basic circuit of the proposed idea is shown in Fig.1 and was designed as follows.

The MOS transistors $M_{b1}$and M_{b2} are designed to operate in saturation and triode region, respectively. The value of current sources can be seen proportional to the drain-source voltage of M_{b2} i.e V_{DS2}. Thus the relation for output reference voltage can be calculated from (2) and (3) as,

$$V_{ref} = V_{th} + V_{DS2}\left[\frac{K_2}{K_1} + \sqrt{\left(\frac{K_2}{K_1}\right)^2 - \frac{K_2}{K_1}}\right] \tag{6}$$

From the relation (6), it is evident that the V_{ref} value is independent of μ and C_{ox}. Thus the next step is, to make V_{ref} less sensitive to temperature dependent parameter, V_{th}. It can be achieved by designing the current sources such that V_{DS2} is also dependent on temperature. Hence, the basic circuit was modified to the final circuit as shown in Fig.2.

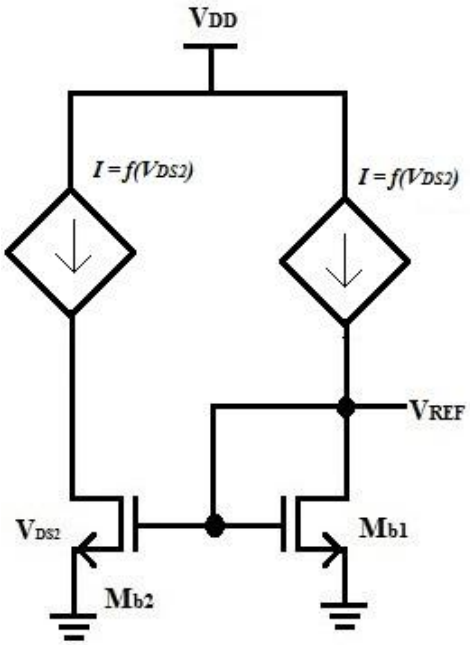

Figure 1: Basic Circuit of The Proposed Idea

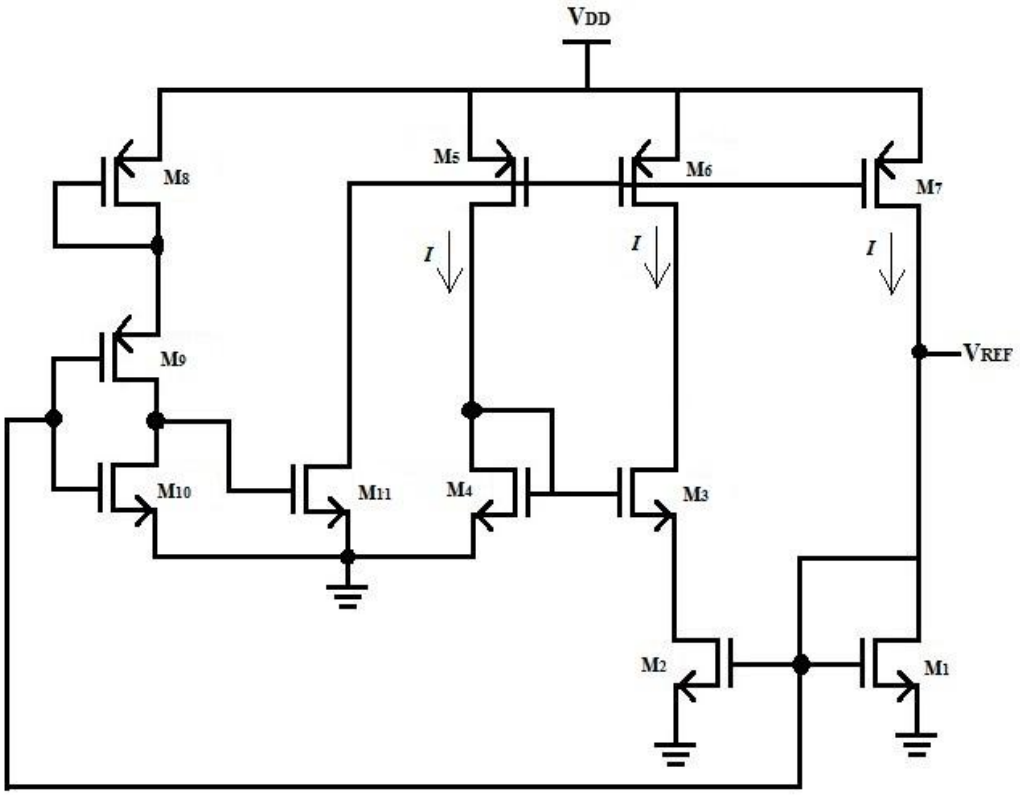

Figure 2: Proposed Voltage Reference Circuit

In Fig.2, Transistors M_3 to M_6 will serve as the current mirror circuit for generating the current *I*. Addition of M_7 transistor will provide V_{DS2} independent of supply voltage,V_{DD}. The bias current *I*, of M_5 to M_7 is determined by linear region operating transistor M_2, which acts as a resistor. Since, M_2 is designed with large channel length, M_3 and M_4 can be operated in sub-threshold region.

The transistors M_3 and M_4 are designed in such a way that their drain currents remains the same. Hence, V_{DS2} can be related as,

$$V_{DS2} = mV_T \ln\left(\frac{K_3}{K_4}\right) = m\frac{k_B}{q}Tln\left(\frac{K_3}{K_4}\right) \tag{7}$$

where, k_B is the Boltzman constant and q is the electron charge. Thus $V_{DS2}$is made independent of *T*.

Substituting (7) in (6), the voltage reference output can be obtained as

$$V_{ref} = V_{th} + m\frac{k_B}{q}Tln\left(\frac{K_3}{K_4}\right)\left[\frac{K_2}{K_1} + \sqrt{\left(\frac{K_2}{K_1}\right)^2 - \frac{K_2}{K_1}}\right] \tag{8}$$

Also the temperature coefficient of V_{ref} can be expressed as

$$\frac{\partial V_{ref}}{\partial T} = -K_{V_{th}} + m\frac{k_B}{q}ln\left(\frac{K_3}{K_4}\right)\left[\frac{K_2}{K_1} + \sqrt{\left(\frac{K_2}{K_1}\right)^2 - \frac{K_2}{K_1}}\right] \tag{9}$$

By equating (9) to zero, the following condition can be obtained

$$\frac{qK_{V_{th}}}{mk_B} = ln\left(\frac{K_3}{K_4}\right)\left[\frac{K_2}{K_1} + \sqrt{\left(\frac{K_2}{K_1}\right)^2 - \frac{K_2}{K_1}}\right] \tag{10}$$

Therefore, the transistors are designed in such a way that the above condition is satisfied and there by maintaining zero temperature coefficient for any temperature.

Experiment Results

The proposed voltage reference circuit has been implemented successfully in 90nm CMOS technology with a constant voltage of 1.03V as the output. For the analysis, the temperature range was taken as 0°C to 160°C attaining a low temperature coefficient of 4.2ppm/°C. A standard low supply voltage of 1.8V was used for the circuit analysis. The circuit displays a significant variation at temperatures less than 0°C and at temperatures greater than 160°C. The reason for the same is due to the huge variation in process dependent parameters of transistors beyond these temperatures. The variation of V_{ref} at different temperatures is plotted in Fig 3. Also the behavior of the circuit at V_{DD} values 1.5V, 1.8V and 2.5V is illustrated in Fig 4.TABLE 1 shows the clear evaluation on results of proposed voltage reference circuit and other recent voltage reference circuits.

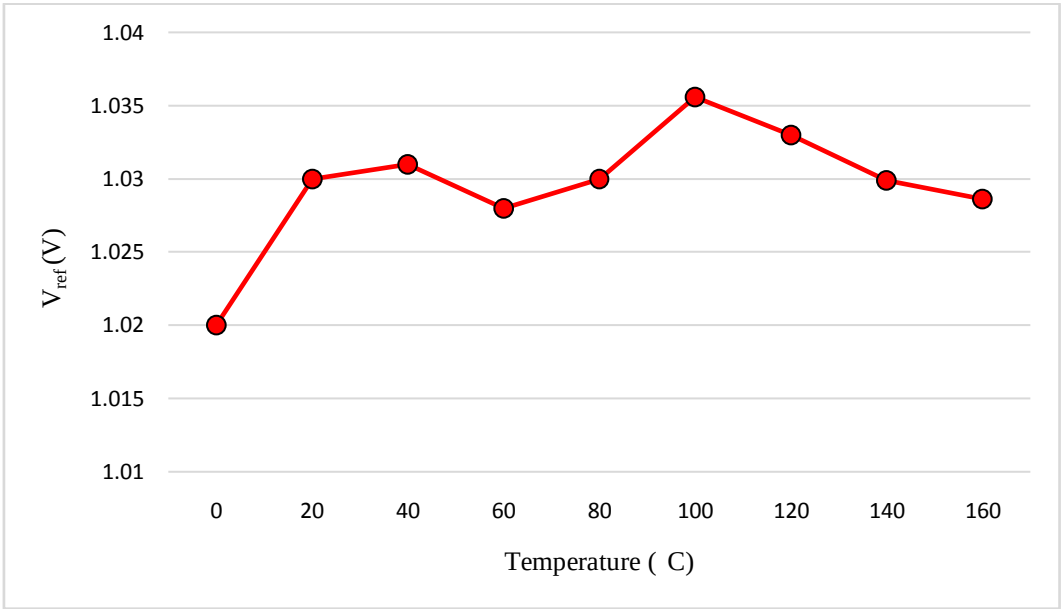

Figure 3: Measured Temperature dependence of proposed circuit using 1.8V supply

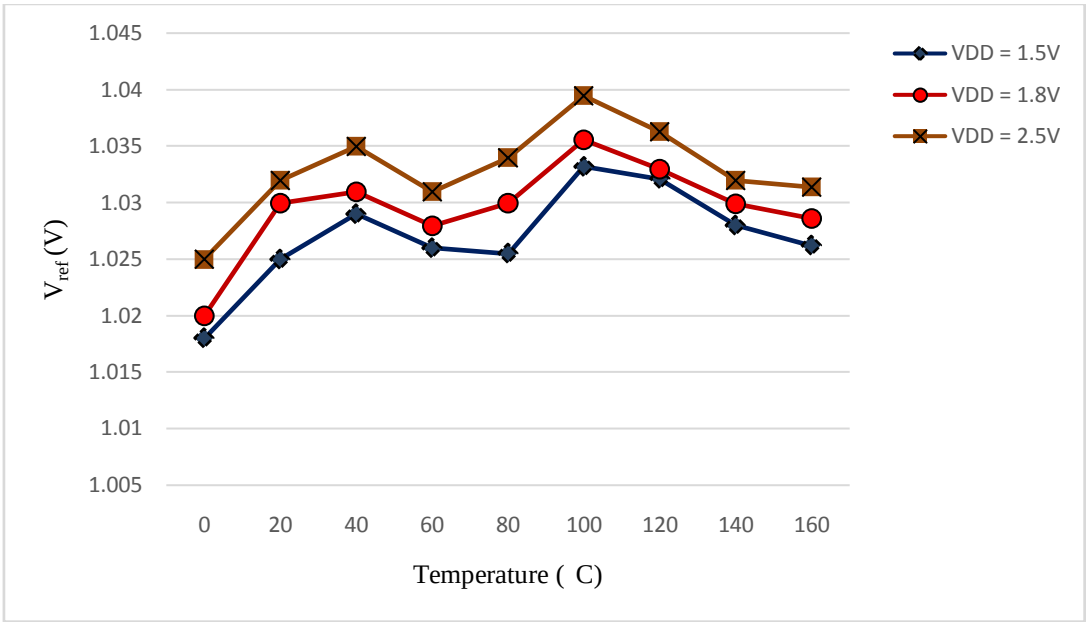

Figure 4: Temperature dependence of proposed circuit using different supply voltages

Table 1: Summary of The Performance of Proposed Voltage Reference Circuit

Parameter	**Proposed Circuit**	**She-Bin Lu et.al[1]**	**De Vita et.al[7]**	**Zhou et.al[5]**	**Zhou et. al[6]**
Technology	90nm	350nm	350nm	350nm	350nm
Supply Voltage (V_{DD})	1.8V	2.5V	1.9V	1.8V	3.3V
Vref (V)	1.03	0.915	0.670	0.847	0.905
Temperature Coefficient (ppm/°C)	4.2	19	10	11.8	14.8
Temperature range(°C)	0 - 160	0 - 80	0 - 80	0 - 130	0 - 100

From the evaluation table, it is obvious that the proposed voltage reference circuit is the supreme one with latest CMOS technology and with least temperature coefficient of 4.2 ppm/°C. Which means, the variation of proposed V_{ref} with respect to temperature is less compared to other recent circuits.

Conclusion

In this paper we have presented a temperature compensated stable voltage reference circuit. The soundness of the proposed work is that it has a very low temperature coefficient i.e it has consistency over a wide range of temperature. It also uses the latest CMOS process technology, which makes the work a relevant one too. The temperature dependencies of μ, V_{th} and C_{ox} were nullified by suitably designing the CMOS transistors. The proposed voltage reference circuit can be used for many mixed signal applications like in CMOS integrators, ADC's etc. Further research and works can be performed to increase the temperature range especially at negative values of temperatures.

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