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A New Approach on Three-Phase Three-Switch Buck-Type Rectifier For Variable-Frequency Drives Pre-Charging Application

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Abstract

This paper presents about a new approach on using three-phase three-switch buck-type rectifier for pre-charging circuits used in variable frequency drives. The main objective of a pre-charging circuit is to charge the dc link bus capacitor to its required charging level within possible allowed time and maximum converter current without any voltage overshoot. This input rectifier provides a dc-link output voltage of 775V at an input ac line to line voltage of 550V, 60Hz. In this paper we will discuss about operating principle and theory of operation of the converter, new control technique for pre-charging, voltage, current stress and losses of passive and power components.

Keywords: Variable frequency drives, Zero crossing detection, Peak current detection

Introduction

All variable-frequency drives (VFDs) available in market have large dc-bus filter capacitors to decouple the effects of inductance from the DC voltage source to the power bridge and also provide a low impedance path for the ripple current associated with hard switching of inverters. Inrush current is a maximum, instantaneous input current drawn by dc-bus capacitors when it first turned on. When a capacitor bank is initially connected to a voltage source a transient charging current will flow as shown in Fig. 1, 2.

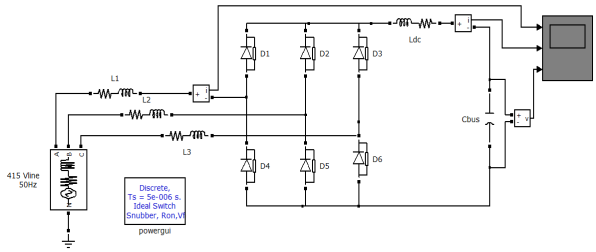

Figure 1: Three - Phase Bridge Rectifier Circuit For Capacitor Current Calculation

The magnitude and frequency of this charging current depends upon the total capacitance and inductance of the

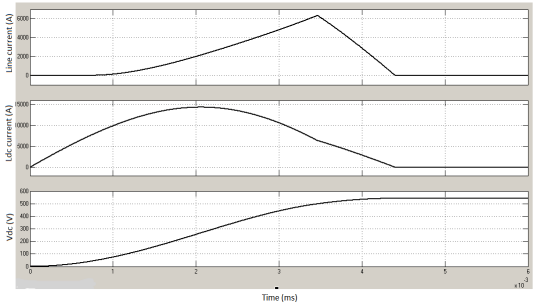

Figure 2: Three - Phase Bridge Rectifier Circuit In-Rush Current And Dc Bus Voltage

circuit as well as magnitude of the applied voltage. In practice the resistance is generally neglected. Experience has shown that inrush current of a single isolated bank normally range from 5 to 15 times the normal capacitor current. Existing variable frequency drives uses different pre-charging techniques like 1. Resistor-contactor arrangement, 2. Thyristor switch, 3. Thyristor Bridge as rectifier, 4. Magnetic resistive-element to charge the dc-bus capacitors. In this paper we will discuss about the design, working principle of three-phase three-switch buck rectifier Fig. 3 used for pre-charging application.

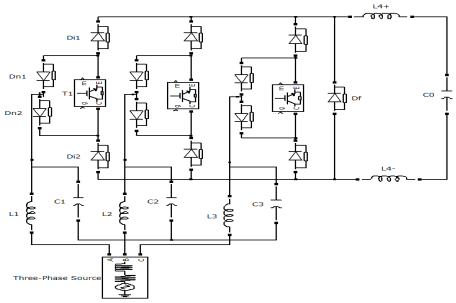

Figure 3: Three – Phase Three-Switch Buck Rectifier Circuit For Capacitor Pre-Charging

The main objective of pre-charging circuit is as follows;

- To charge the dc-bus capacitor within the allowed time (as per VFD system requirement ~4.5sec)
- To limit both the peak dc link and peak ac input line current to any desired limit.

Furthermore in this paper we will discuss about converter principle of operation, proposed new control technique in Section II, pre-charging operation and different switching intervals in Section III, and finally the voltage, current stress and losses of passive and active components.

Basic Principle of Operation

A. Assumptions

For the sake of simplicity we assume the following considerations [1]:

1. a purely sinusoidal shape of the filter capacitor voltage, $u_{CF,i} \approx u_{N,i}$ where the mains phase voltages were;

$$\begin{aligned} u_{N,R} &= U_N \cos(\omega_N t), \\ u_{N,S} &= U_N \cos(\omega_N t - 2\pi/3), \\ u_{N,T} &= U_N \cos(\omega_N t + 2\pi/3), \end{aligned} \tag{1}$$

   Where $\varphi_N = \omega_N t$, ω_N denotes the mains angular frequency
2. The dc current through the output inductor L_4 is assumed to be constant and output voltage U_0 across the output capacitor C_0 also constant, i.e., the high frequncy ripple due to swiching operation can be negleted.

Futhermore we will neglete the following;

1. the fundamental voltagedrop across the input filter inductors (L_1, L_2, L_3) can be negleted.
2. the input mains current are assumed to equal to the input rectifier fundamental current therefore the reactive currents due to the filter capacitors(C_1, C_2, C_3) can be negleted.

B. Principle of Operation

Based on the above assumption the basic operating priciple of three phase three switch buck rectifier for pre-charging application is similar to the standard three phase uncontrolled (or) controlled bridge rectifier. The main difference is number of controlled switches and control technique used for pre-charging the DC-link capacitor. A three-phase ac voltage of $U_{R,N,}$ $U_{S,N,}$ $U_{T,N}$ = 550V as shown in Fig. 4, is applied across the rectifier, according to the respetive peak ac-voltages and modulation individual switches will be turned on and off in a sequence(110-011-101) such as shown in Fig. 5, where i=R,S,T indicates a combination of three swiches S_i. When S_i=0 means the correcponding swicth in the bridge leg is turned off and S_i=1 indiates the switch is in turned on state. For example, by considering one swiching

sequence (101) the current flows in the bridge legs of the rectifier, dc link inductor and dc link capacitor S_R - L_4 - C_0 -S_T. With this, the input current can be calculated for each of the switching sequences.

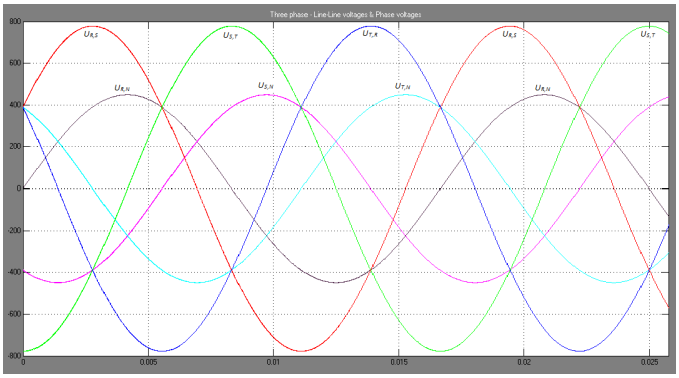

Figure 4: Mains phase voltage $U_{R,N,}$ $U_{S,N,}$ $U_{T,N}$ = 550V and line-line voltages are $U_{R,S,}$ $U_{S,T,}$ $U_{T,R.}$

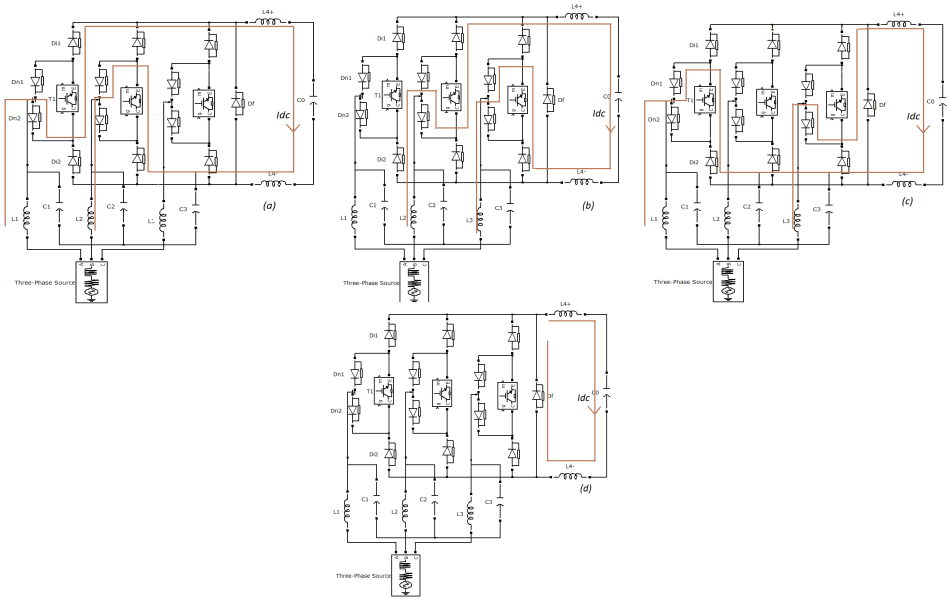

Figure 5: Conduction states of the Three phase Three switch buck PWM rectifier, (a) I_{dc} during switching sequnce(110), (b) I_{dc} during switcing sequence(011), (c) I_{dc} during switching sequence(101), (d) I_{dc} during freewheeling

Generally the three-phase rectifier input current is defined as

$$i_{rec} = \frac{2}{3}\left(i_{rec,R} + e^{j2\pi/3}.i_{rec,S} + e^{j4\pi/3}.i_{rec,T}\right) \quad (2)$$

For the switching state j=(101) the rectifier input currents are $i_{rec,R} = I$, $I_{rec,s} = 0$ and $i_{rec,T} = -I$, therefore the rectifier input current space vector for the switching states will be

$$i_{rec,(101)} = I.\frac{2}{\sqrt{3}}e^{j\pi/6} \tag{3}$$

$$i_{rec,(110)} = I.\frac{2}{\sqrt{3}}e^{-j\pi/6} \tag{4}$$

$$i_{rec,(011)} = I.\frac{2}{\sqrt{3}}e^{j4\pi/3} \tag{5}$$

C. Proposed Control Technique

The proposed control algorithm shown in Fig. 6 consists of two blocks i). Zero crossing detection (ZCD) and ii). Peak current mode control (PCM). The zero crossing detection circuit is

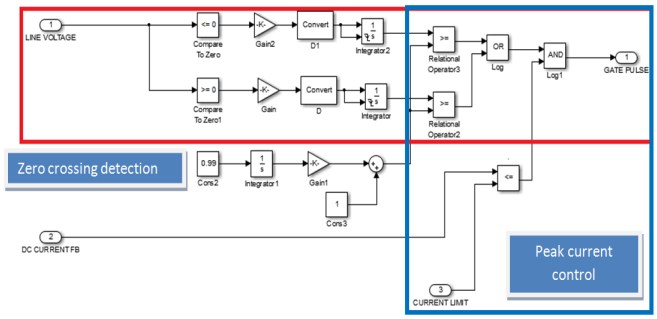

Figure 6: New Proposed Soft Charging Control Technique With Constant Current Control

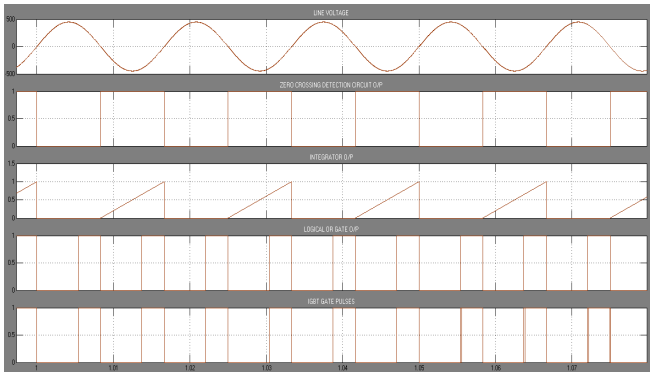

Figure 7: Waveforms at different stages of pre-charging control circuits, (a) Line voltage, (b) Zero crossing detection circuit o/p, (c) Logical OR gate o/p, (d) Logical o/p from current feedback, (e) IGBT gate pulses

used for generating PWM pulses required for normal operation of the converter. The basic switching operation of three phase three switch buck converter is similar to the standard three phase uncontrolled (or) controlled bridge rectifier. Since we are using the controlled three phase switches we required PWM gate pulses for turning on the IGBT switches. The required PWM gate pulses were generated through passing the input ac voltage in a zero crossing detector (ZCD) circuit, falling edge integrator and logical gate circuits. The three phase input ac voltages were applied to the ZCD circuits, series of pulses will be generated based on the zero crossing of ac input voltage. The pulses were further sampled through a falling edge integrator through which synchronized ramp signals will be generated based on the positive and negative ac voltages. Since we need to switch on two IGBT's during each cycle the ramp signal were compared through a comparator and logic gates through which two pulses were generated for each cycle of ac input voltage. In peak current mode control the DC inductor current was compared with the required reference set current, when the inductor current is less than the set current a pulse will be generated and vice versa. The resultant pulses from the zero crossing detection circuit and peak current control were logically compared through an AND gate and generates resultant PWM pulses for IGBT switches as shown in Fig. 7. Separate control circuits (zero crossing & peak current detection circuit) will be implements for individual three phases through which we will generate the individual gate pulses for each IGBT switches.

Pre-Charging Operations and Different Switching Intervals

The basic working principle of the converter was discussed in the preceding paragraphs; the dc link capacitor pre-charging is divided into three intervals Interval I, Interval II and Interval III as shown in Fig. 8. The intervals were differentiated based on the current limiting control technique used to control dc link current within the predefined set value. During interval I the dc link current was below the predefined set current value, assume if we are setting the current value as 200A, this interval specifies the time from starting of the converter till the dc link current reaches the value of 200A. During interval II the dc link current reaches the predefined set value of 200A, in this interval converter operates in constant current operating mode, due to the peak current detection circuit i.e.). DC link current will be limited to 200A. In this mode of operation the converter power switches will be operating in the switched mode of operation in order to maintain the dc link current constant. The interval III was similar to interval I, during this interval the dc link current started decreasing from the predefined set current value of 200A and the converter will be operating in the normal mode.

D. Interval I

In this interval the converter operates in the normal mode of operation same as standard three phase uncontrolled (or) controlled bridge rectifier. During this mode of operation converter dc link current does not reaches the predefined set current value of 200A, so the output from peak current detection circuit will be in logical HIGH and output from zero crossing detection circuit will be also in logical HIGH state. The

gate pulses for IGBT will be a logical AND operation of zero crossing detection and Peak current detection circuits output, so during this mode the IGBT switching is based the peak magnitude of input ac-voltage value as shown in Fig. 9. The average and rms values during this pre-charging interval for a mains period are;

$$I_{i,avg}=\frac{1}{2\pi}\int_0^{2\pi}\left(\frac{1}{T_p}\int_0^{T_p} i_i(\varphi_N,t_\mu)dt_\mu\right)d\varphi_N \tag{6}$$

$$I^2_{i,rms}=\frac{1}{2\pi}\int_0^{2\pi}\left(\frac{1}{T_p}\int_0^{T_p} i_i^2(\varphi_N,t_\mu)dt_\mu\right)d\varphi_N \tag{7}$$

Where, $\varphi_N=\omega_N t$ (8)

The average and rms current flows through the power semiconductor during this interval for a pulse period are [1];

$$i_{T,avg}=\frac{1}{T_p}\int_0^{\delta_R T_p} I\,dt_\mu = I.\delta_R \tag{9}$$

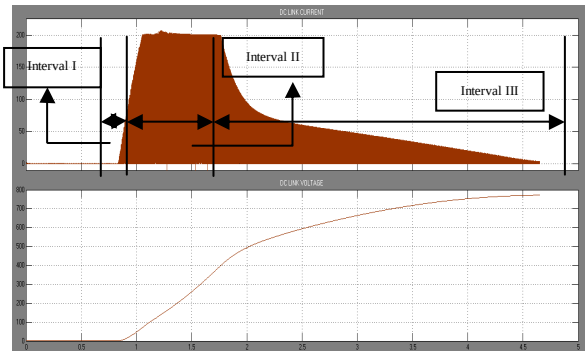

Figure 8: (a). DC link currnet limited to 200A, (b). DC link voltage of 770V across the capacitor

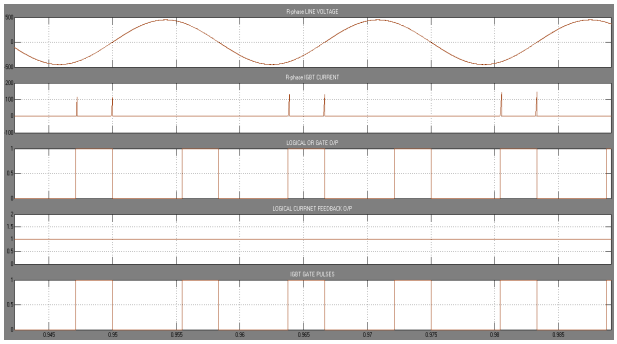

Figure 9: Waveform during pre-charging Interval I, (a) R-phase Line voltage $U_{R,N}$ = 550V, (b)R-phase IGBT current, (c)Zero crossing detection circuit logical OR gate o/p, (d) Peak current detection logical current feedback o/p, (e) IGBT gate pulses

$$i^2_{T,rms} = \frac{1}{T_p} \int_0^{\delta_R T_p} I^2 dt_\mu = I^2 . \delta_R \quad (10)$$

E. Interval II

During this mode converter operates in switching mode as the converter dc link current reaches the predefined set value of 200A. Once the dc link current reaches the predefined set current limit, peak detection circuit generates the logical LOW signal; meanwhile the output from zero crossing detector circuit will be a logical HIGH signal based on the magnitude of input ac-voltage. The gate pulses for IGBT will be generated based on the logical AND operation of zero crossing detection and peak current detection circuits. Let's assume, DC link current reaches the predefined set current value of 200A, the peak detection circuit generates a logical LOW signal. Since the predefined condition was if the dc link current is more than the set current it will generates a logical LOW signal, meanwhile when the dc link current is less than the set current peak current detection circuit will generates a logical HIGH signal. During this interval once the peak detection circuit logical level reaches the LOW state and the output from

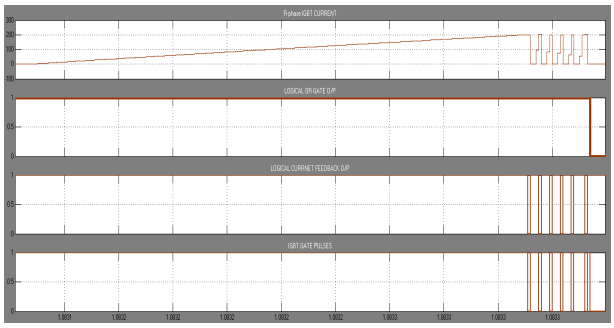

Figure 10: Waveform during pre-charging Interval II, (a)R-phase IGBT current, (b)Zero crossing detection circuit logical OR gate o/p, (c) Peak current detection logical current feedback o/p, (d) IGBT gate pulses

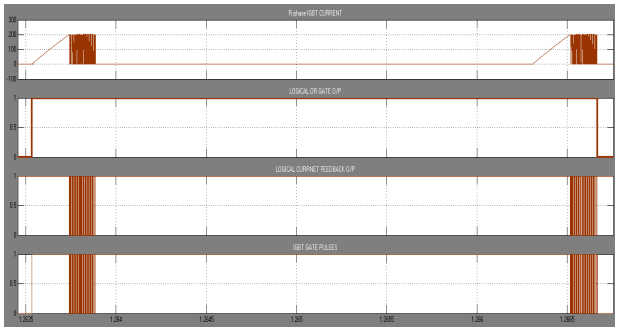

Figure 11: Waveform during pre-charging Interval II (Zoom-out version), (a)R-phase IGBT current, (b)Zero crossing detection circuit logical OR gate o/p, (c) Peak current detection logical current feedback o/p, (d) IGBT gate pulses

zero crossing detection will be logically HIGH based on the ac voltage peak magnitude, the IGBT gate pulses will be disabled as the IGBT gate pulses output is based on the logical AND operation of dc link current peak detection and zero crossing detection circuits outputs as shown in Fig. 10,11. During the switch OFF condition of IGBT the stored energy dc link inductor will be freewheeled through the freewheeling diode.

Total average current flow through the dc link inductor is the sum of current flows through switch and the current flows through the freewheeling diode. The average and rms current flows through the power semiconductor will be same as interval I.

$$I_{dc,avg} = \sqrt{3}\, I_{T,avg} + I_{Fd} \tag{11}$$

F. Interval III

In this interval the converter operates similar to the interval I, as the dc link current is less than the pre defined set value. During this interval the current required to charge the dc link capacitor started to decrease and the rms, average current will be remains same as interval I.

The summary of converter switching operations at different intervals was provided in Table.1.

Discussion

In the previous sections the operation and working principle of three-phase three-switch buck PWM rectifier at

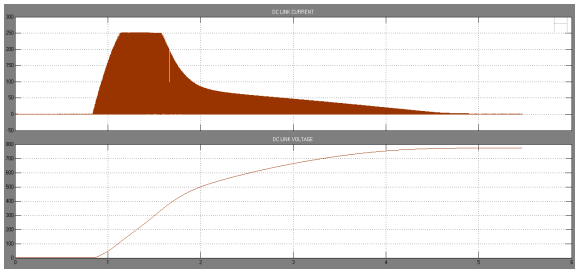

Figure 12: (a). DC link currnet limited to 250A, (b). DC link voltage reaches to 770V at t=4sec

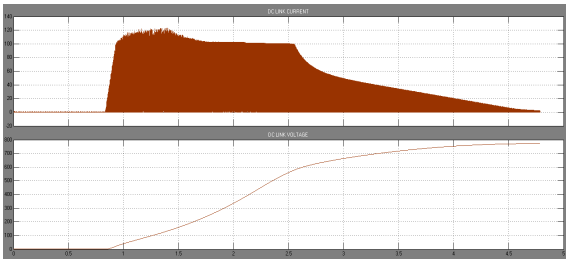

Figure 13: (a). DC link currnet limited to 100A, (b). DC link voltage reaches to 770V at t=4.5sec

different intervals were illustrated. As per the system requirement of VFD the dc bus capacitor should reach the maximum dc link voltage limit within 4.5sec and it should be possible to limit the dc link peak current to any predefined set current value to avoid blowing of mains fuse and reduction in usage of high current ac circuit breakers to reduce the cost and power density. The preferable selection of pre charging current limit is the rated current of the VFD, as this converter will be used during the pre-charging of dc bus

$$I(t) = V\frac{dV(t)}{dt} \tag{12}$$

capacitor and also for driving the VFD, through this we can avoid using a separate circuit mechanism (or) resistor bank network for pre-charging application. We can vary the pre charging time of dc-link capacitor by varying the allowable peak charging current as shown in Fig. 12, 13, if the allowable current is less the charging time for pre charging the dc-link capacitor will be more and vice-versa.

During pre-charging condition, based on the interval of operation the total loss will vary, e.g. during the interval I & III the conduction and switching losses of the IGBT is less, as the IGBT conducts for a smaller duration and the stored energy in the dc link inductor can have more time to dissipate it energy, so during this interval the major losses were from IGBT switching losses and freewheeling diode losses. In interval II the major losses were from IGBT switching, conduction losses and freewheeling diode losses. Since in this interval compared with conduction losses(even its not negligible) switching will be high as the dc link current reaches to the predefined set value the IGBT conducts in switch mode of operation.

The conduction losses were calculated based on the forward voltage drop and forward resistance of the semiconductor.

$$P_{Cond,T} = U_{ce} * I_{s,avg} + r_{ce} * I_{s,rms}^2 \tag{13}$$

$$P_{Cond,D} = U_f * I_{d,avg} + r_d * I_{d,rms}^2 \tag{14}$$

The total switching losses of the IGBT and diode are therefore given by [2]-[7];

$$P_{Sw,T} = P_{s,off,s-s} + P_{s,off,s-d} + P_{s,on,d-s} + P_{s,ons-s} \tag{15}$$

$$P_{Sw,Di} = P_{Di,rev,s-s} + 2 * P_{Di,fwd,s-s} + 4 * P_{Di,fed,s-s} \tag{16}$$

$$P_{Sw,DF} = P_{DF,rev,d-s} \tag{17}$$

For total loss calculation in addition to active components losses passive components losses also need to be considered. The losses of the input filter capacitor and filter capacitor can be neglected due to its low equivalent series resistance value. The main parameter required for selection of dc link inductor its allowable peak-to-peak ripple current;

$$\Delta i_{L,\,p-p\,\max} = 0.4 * I \tag{18}$$

The selected inductors core and copper losses were calculated based on below equations;

$$P_{L,core}\left[\frac{W}{kg}\right] = 6.5 * \left(\frac{B_{sat}[T]}{2}\right)^{1.74} * \left(f\,[kHz]\right)^{1.51} \tag{19}$$

$$P_{L,copper} = \frac{I_{Cu}}{\sigma_{Cu} * A_{Cu}} * I^2 \tag{20}$$

Conclusion

In this paper a design of three phase three switch buck type rectifier for pre-charging application was explained along with its working and theory of operation. The main advantage of proposing this converter and control technique for pre-charging application is its simple in operation, less power density compared with existing pre-charging concepts and possibility of using same converter for both operations, i.e.) for pre-charging application and driving the VFD. When we are comparing the total losses of different pre-charging circuits the losses were less when we uses converters for pre-charging applications compared with resistor banks. Further research on going on using three phase three switch converter for both pre-charging and driving the VFD. When we use single converter for both application, there will be two separate control mechanism to control the peak dc link current for pre-charging and to control and maintain the constant dc link voltage across the dc link capacitor during driving operation of the VFD.

Table 1: Connverter Operation At Different Switching Intervals

Converter operation intervals		***O/P of ZCD***	***O/P of PCM***	***IGBT On-state***	***Converter switching modes***
Interval I (DC inductor current < Pre defined set current)		High	High	ON	Normal mode of operation
Interval II	(DC inductor current < Pre defined set current)	High	High	ON	Switched mode of operation
	(DC inductor current > Pre defined set current)	High	Low	OFF	
Interval III (DC inductor current < Pre defined set current)		High	High	ON	Normal mode of operation

References

[1] Thomas Nussbaumer, Martina Baumann and Johann W. Kolar, " Comprehansive Design of a Three-Phase Three-Swith Buck-Type PWM Rectifier", IEEE Transaction on Power Electronics, Vol. 22, No. 2, March 2007.

[2] Martina Baumann and Johann W. Kolar, " Comparative Evaluation of Modulation Methods for a Three-Phase/Switch Buck Power Factor Corrector Concerning the Input Capacitor Voltage Ripple"

[3] Thomas Nussbaumer, Martina Baumann and Johann W. Kolar, "Design and Comparitive Evaluation of Three-Phase Buck+Boost and Boost+Buck Unity Power Factor PWM Rectifier System for Suppling Variable DC Voltage Link converter", 25th International Conference on Power Electronics, 25-27 May 2004.

[4] Kolar, J.W, and Zach, F.C," A Novel Three-Phase Three-Switch Three-level Unity Powerr Factor Rectifier", Proceeding of the 28th International Power Conversion Conference, Nuremberg, Germany, pp. 125-138, 28th-30th June 1994.

[5] IXYS Corporation,"Rectifier Moule for Three-Phase Power Factor Correction *VUI 31-12N1*, www.ixys.com

[6] Nussbaumer.T, and Kolar. J.W," Advanced Modulation Scheme for Three-Phase Three-Switch Buck-Type PWM Rectifier Preenting Mains Current Distortion Originating fom Sliding Input Filter Capacitor Voltage Intersecions". Proceedings of the 34th IEEE Power Electronics Specialists Conference, Mexico, Vol.3,pp.1086-1091, 15th-19th June 2003

[7] Infineon Technilogies,"Cool MOS Poer Transistor SPW47N60C3", www.infineon.com