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Design and Analysis of Unbuffered Amplifier Using 180nm Technology

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Abstract

The OTA (Operational Transconductance Amplifier) is a basic building block of analog integrated circuit. It is a combination of differential amplifier with current mirror as load. It is also called as unbuffered amplifier. Here we design a single stage OTA with Wilson current mirror to improve the gain. The circuit has been implemented with Cadence in 180nm technology. This tool is used to analyses the transient response, AC response gain and phase margin. The supply voltage is 1.8v with entire transistors working in saturation region. The gain obtained for the proposed OTA is 50dB.

Keywords- Single Stage OTA, Wilson Current Mirror, Gain, Phase Margin, Output Impedance, Power Dissipation.

I. INTRODUCTION

Operational amplifier is used in most electronic appliances, wide range of consumer electronics and many industrial applications. It has also been commonly used in audio, data transmission and in telephonic systems for many years because of its inherent resistance to external noise sources. Differential signaling is becoming popular in high-speed data acquisition. The gain of novel single stage OTA shown in Figure 1 is insufficient hence we design an OTA with Wilson load [3]. The OTA is an amplifier in which a differential input voltage produces an output current and hence it is called as Voltage Controlled Current Source (VCCS) [1] [2]. OTA is the most important building block of analog circuit with linear input-output characteristics [5]. It is similar to conventional operational amplifier that has high output impedance and

low input impedance and that it can be used with both positive and negative feedback [4].

The amplifier faces difficulties in achieving high gain, high output swing and low-power consumption with low-input voltage [3]. The usual way to boost the gain is by cascading the transistors, but is impossible in low voltage design due to its output swing limitation [4]. Hence we design a Wilson current mirror OTA to improve the gain of the circuit without cascading transistors.

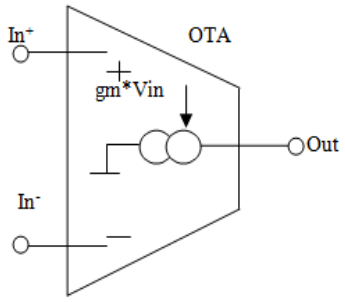

Figure 1 Ideal OTA

Voltage Gain = $V_{OUT}\ (Vin^{+} - Vin^{-}) = R_{Load} \cdot g_m$ (1)

The current mirror is a circuit which is simply called as Current Controlled Current Source (CCCS). It acts as a large resistor without consuming excessive voltage headroom to provide constant current [2] [12]. When the gate to source potential of two identical transistors are the same then the current flowing through a transistor is the replica of the current at the output of the other transistor. The NMOS transistor is used as current sink and PMOS transistor as current source [6] [8]. Every current mirror has three important parameters. (i) Current Ratio (ii) Output Resistance (iii) $V_{O\ min}$ Requirement.

In this work we design a single stage OTA with Wilson current mirror to improve the gain and to obtain high output swing. The motivation for using the Wilson current mirror configuration is its high output impedance. There are three ways in which is the gain could be increased. (i) Add additional gain stages (ii) Increase the transconductance (iii) Increase the output resistance. On increase of output resistance there will be a reduction in bias current in turn reducing increasing the overall gain.

The major advantage of Wilson current mirror over the basic and cascode current mirror is that they have higher output impedance.

The paper is organized as follows: analysis of Wilson current mirror and single stage OTA with Wilson current mirror are described in Section II. The simulation and layout design are discussed in Section III. The paper is concluded in Section IV.

II.ANALYSIS OF WILSON CURRENT MIRROR AND SINGLE STAGE OTA WITH WILSON CURRENT MIRROR

A. Modified Wilson Current Mirror

The Wilson current mirror shown in Figure 2 has four transistors M_1, M_2, M_3, and M_4 that are identical. In cascode current mirror the diode connected transistor is at the input side, whereas in Wilson current mirror the diode connected transistor is at its output side and this configuration is called as negative feedback because of which drain current is stabilized. The M_1 transistor is biased with V_{bias}. I_{D1} current flows through M_1 transistor and I_{D2} current through M_2 transistor. M_1 and M_3 transistors are identical connected in such a way that they have same $V_{gs.}$ They are maintained in saturation region. The I_{D3} current is equal to I_{D2} input current and hence I_{D1} equals I_{D4}.

$$I_{OUT} = \frac{(W/L)4}{(W/L)3}\frac{(W/L)2}{(W/L)1} I_{REF} \quad (2)$$

$$\frac{I_{OUT}}{I_{REF}} = \frac{(W/L)4}{(W/L)3}\frac{(W/L)2}{(W/L)1} \quad (3)$$

Where, W= Width of the MOS
L= Channel Length of the MOS

The equation for drain current of NMOS transistor is given by

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{Tn})^2(1+\lambda V_{DS2}) \quad (4)$$

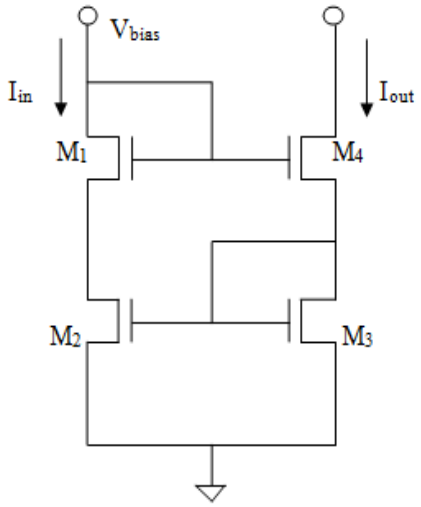

Figure 2 Wilson Current Mirror Schematic

The Wilson current mirror achieves high output impedance by using negative feedback. The current series sampling is used to increase the output impedance (1/β) times. It is directly proportional to the magnitude of the loop-gain because of the

feedback action at the output side from the output current to the gate of output transistor M_4. When V_O increase I_O also increases because of channel length modulation. Even though we apply the same gate to source voltage V_{GS}, V_{DS} increases.

The term r_o^2 in the output impedance and very high g_m eliminates the channel length modulation. So the Wilson output resistance is very high compared to other current mirrors.

$$R_{out} = r_o + g_{m2} \frac{ro^2}{2} \quad (5)$$

The minimum output voltage V_O is necessary to keep both M_3 and M_4 transistor in saturation region.

$$V_{O\,(min)} = 2\sqrt{2I_D} / \beta_{3,4} + V_{THN3} \quad (6)$$

B. Single Stage OTA with Wilson current Mirror

In this section we describe about the single stage OTA with Wilson current mirror. The differential amplifier does not provide high gain for which we add buffer stages but here without adding buffer stages we achieve more gain by using the Wilson current mirror as shown in Figure 3. The transistor sizes of M_3, M_4, M_5 and M_6 must be same in order to maintain its symmetrical structure.

First we have to decide the parameters. The current flowing through M_1 and M_2 are equal to M_3 and M_5 branches respectively and hence M_4 and M_6. I_O is the total current that flows through M_7 transistor which is divided into two branch currents $I_O/2$ that flows through M_3, M_5 and M_4, M_6 transistors respectively. Let the gain specification of the circuit be $A_V \geq 60$dB. We calculate the bias current I_O from the required slew rate. The current flowing through the transistor may be controlled by using bias voltage. This circuit takes differential input and provides a single ended output.

C. Design Parameters

(i) Gain

The gain is directly proportional to the output voltage V_{out} and inversely proportional to input voltage V_{in}. If the input voltage increases the gain decreases and if V_{in} decreases then gain increases. The gain of the amplifier is improved by increasing the output transconductance without adding cascade devices.

$$\text{Gain} = V_{out} / V_{in1} - V_{in2} \quad (7)$$

The DC gain is dependent on the output of M2 transistor. The transconductance of this transistor is very high by use of Wilson current mirror as load. The DC gain and phase margin achieved are also high.

(ii) Phase and Gain Margin

Phase margin is measured at the point of frequency where the open-loop voltage gain of the amplifier equals unity. The gain margin is observed at a point where the phase of the phase response curve is -180˚. Phase margin is of a safety factor which is used to obtain a controlled design.

(iii) Bandwidth

The transistor M_1 is given with the lowest differential input voltage V_+ and M_2 transistor has lowest differential input voltage V_-. The gain bandwidth product of the circuit depends on these two transistors. The bandwidth is measured at the point where gain falls of maximum signal 3dB. The open loop configuration are extremely limited the bandwidth and closed loop configuration is significantly increases an OTA bandwidth.

$$\text{Gain bandwidth} = g_{m4} / 2\pi c_L \quad (8)$$

(iv) Slew Rate

The slew rate is the rate of change of output voltage, the slew rate may distort the output signal if the input signal is changing very fast, and the output is linearly distorted. The load capacitor C_L at the output influences the slew rate. The Capacitor, C_L charges and discharges through M_4 transistor and M_2 transistor respectively. When we apply a differential voltage in an extreme case the one branch is completely ON and the other branch completely sinks all the current. The speed of the output voltage is limited by the biasing currents and the output capacitance.

$$\text{Slew Rate} = I_o/C_L \quad (9)$$

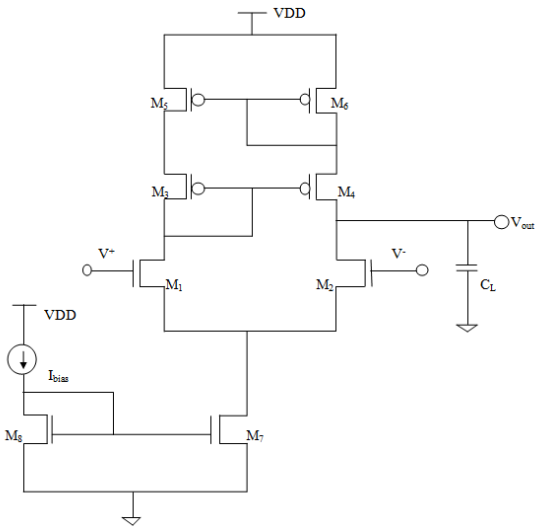

Figure 3 Proposed CMOS OTA with Wilson

(v) Output Swing

Output voltage swing defined how close to the op-amp output can be driven to rail to rail V_{DD} or V_{SS} under defined operating condition where the op-amp still can function correctly. The voltage output swing capability of an OTA is dependent on the circuit output stage design and the load current.

$$V_{in,swing} = V_{O,swing} \quad (10)$$

(vi) ICMR (Input Common Mode Range)

The sizes of M_3 and M_4 transistor depend on the $ICMR^+$ value and M_7 transistor dependent on the $ICMR^-$ value. The values of $ICMR^+$ and $ICMR^-$ are initially assumed depending on the power supply voltage.

III.SIMULATION RESULTS OF WILSON CURRENT MIRROR AND SINGLE STAGE OTA WITH WILSON

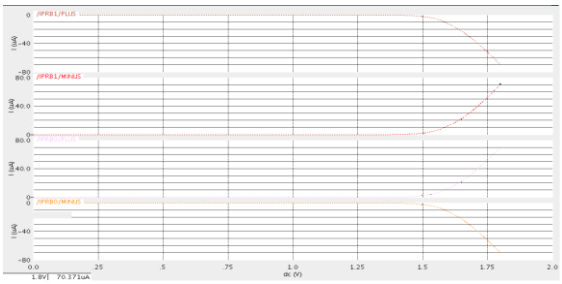

Figure 4 Wilson Current Mirror DC Responses

The simulation result of modified Wilson current mirror is shown in the Figure 4. The input voltage is 0.4mv and input current is 70μA, output current is 70.52μA, transconductance is 644μ.

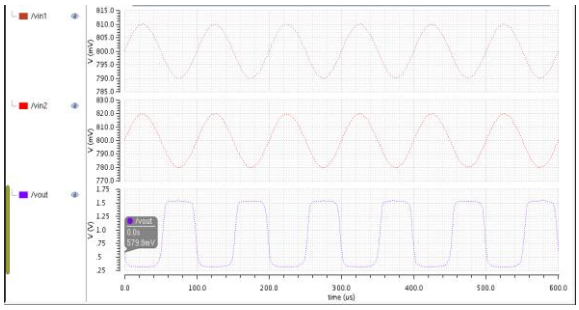

Figure 5 Result of Transient Response

The simulation result of Transient response for single stage OTA with Wilson is shown in Figure 5.

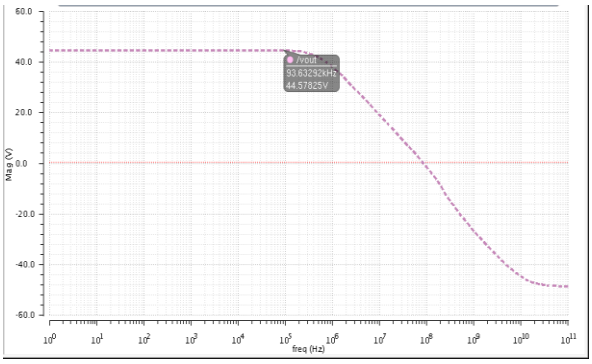

Figure 6 Result of AC Response

The simulation result of AC response of Single stage OTA with Wilson current mirror is shown in the Figure 6. The magnitude of the response is 43v.

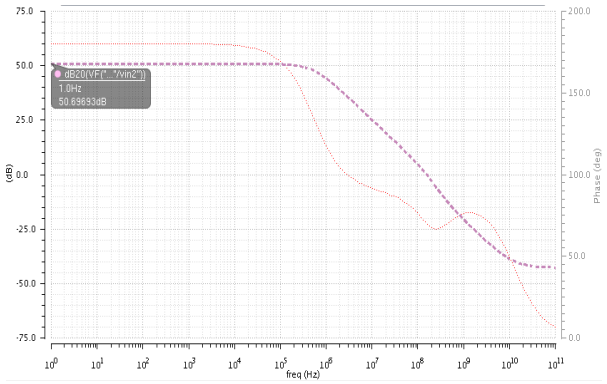

Figure 7 Result gain margin and Phase margin

The simulation result of gain and phase margin for single stage OTA with Wilson shown in Figure 7. On AC analysis waveforms of phase and gain are obtained. Then the phase at 0dB gain is measured that gives the phase margin. For the phase margin on 180^0 scale the achieved phase is 78^0, with the gain of50dB.

IV.SINGLE STAGE OTA WITH WILSON CURRENT MIRROR LAYOUT DESIGN

The layout has been designed in 180nm CMOS technology using cadence. The most important aspect of layout is the minimization of area. Here the final chip layout design has been completed with all the pad connections by the use of fingering that

reduces our area and wire lengths. Both resistive and capacitive parasitic are extracted from this layout thereby reducing the resistance and capacitance values.

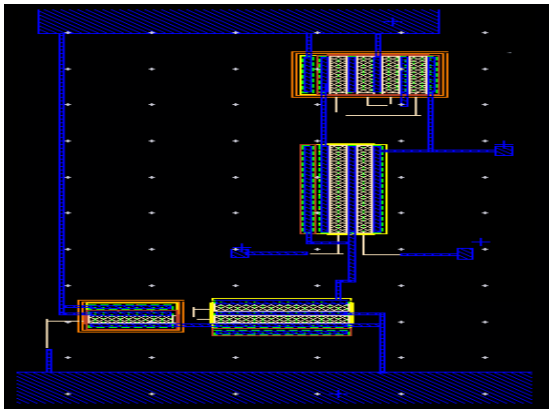

Figure 8 Proposed OTA with Wilson Layout

V. SIMULATED RESULTS

Table I Basic and Wilson current mirror

Parameters	Basic Current Mirror	Wilson Current Mirror
Power Supply	1.8V	1.8V
Drain Current -I_D	70µA	70µA
Transconductance-g_m	497µA	644µ
Power Dissipation	44.11µA	14.1µW
Output Resistance	12.5KΩ	15.85KΩ

Table II OTA with Basic and Wilson Current Mirror

Parameters	***OTA with Basic Current Mirror***	***OTA with Wilson Current Mirror***
Power Supply	1.8V	1.8V
DC Gain	31.5dB	50.68dB
Bandwidth	1.023MHz	3.84MHz
Phase Margin	61.46^0	78.79^0
Slew Rate	4.89 v/µs	9.24 v/µs
Power Dissipation	4.89µw	2.05mW
Gain Bandwidth	-	235MHz

VI. CONCLUSION

The main intension of this paper is to achieve high DC gain and bandwidth. The increase in output transconductance increase the DC gain. The transistor sizing is also

important to improve the gain of the circuit. The single stage OTA with Wilson load is optimized and simulated with 180nm technology using Cadence Spectre, and we have analyzed about modified Wilson current mirror and the parameters achieved are transconductance 644µ, DC gain is 50dB, Phase margin 78.79^0, Power dissipation 2.05mW.

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