International Journal of Applied Engineering Research
ISSN 0973-4562 Volume 10, Number 8 (2015) pp. 21361-21376
© Research India Publications
http://www.ripublication.com

Particle Swarm Optimization Based Neutral Point Potential Minimization For Neutral Point Clamped Inverter

Satheeshkumar R[1], Balasubramani M[2]and Gowri Shankar J[3]
[1]PG-Scholar, [2] Assistant Professor-III, [3]Assitant Professor-II
School of Electrical and Electronics Engineering, SASTRA University,
Thanjavur – 613401, Tamilnadu, India
Email: r.satheeshtvk@gmail.com

Abstract

This study propose the design of a Neutral Point Potential regulator (NPP) using PI controller technique and Particle swarm optimization (PSO) technique to balance the capacitor voltage for a three-level NPC inverter using closed loop control technique. The purpose of this regulator is to maintain the midpoint potential by adding offset voltage continuously. While using PI controller technique the offset voltage is calculated by using the magnitude of third order harmonic content, total harmonic distortions (THD), peak-to-peak value and the average value in NPP. In case of PSO technique the mathematical equation describing the general neutral point (NP) current for three level NPC inverter is derived, which is a function of modulation index, power factor angle and offset voltage. PSO algorithm is employed to obtain the offset voltage from the general neutral point current equation by keeping the neutral point current to the minimum value. In both the technique dc-link capacitor voltage is maintained constant and the distorted voltage at the neutral point (NP) and the switching losses in the inverter are reduced. NPP regulator designed using PI technique and PSO technique are Compared. The simulation is done with closed loop controller, simulation results verifying the approach is presented

Keywords: Particle Swarm Optimization (PSO),Neutral point clamped (NPC) inverter, Neutral point potential (NPP), Neutral point(NP), Total harmonic distortions (THD), Pulse width modulation(PWM) techniques

Introduction

Neutral Point Clampedinverter (NPC):

NPC inverter (three-level inverters) has been in the lime light in recent years.The NPC-inverter has wide range of applications because they have multiple advantages

like minimum switching losses,reduced current ripples in the output and harmonic reductions. Although it has several advantages, imbalance in the dc-link voltage has been reported to be a major disadvantage [1]. This is because the midpoint voltage is derived using capacitors and it carry load current. Unequal loading, unequal distribution of charges, non-identical ratings of capacitors leads to imbalance in the dc bus capacitor voltages and this will cause the dc midpoint voltage to drift. Due to imbalance in the capacitor voltage, the output voltage waveforms and current waveforms of the inverter are distorted and also results in oscillations in NP. This problem can be solved by maintaining dc capacitor voltage balance.

There are several technique to maintain the capacitor voltage balance in literature as mentioned below

1. Adding extra switching components such as inductance and capacitance to the circuit to balance the capacitor voltage.
2. There are several modulation techniques such as PWM, SPWM and SVPWM can be used in inverter control strategy.
3. Genetic algorithm based balancing technique and PI controller based technique are also used in inverter control strategy.

There are several techniques which tries to turn on and off the devices to keep the capacitor voltage in balance. In SVPWM technique it is quite complicated to derive the relationship between the switching state and the neutral point [2]. Therefore it is difficult to balance neutral point potential (NPP) exactly as required. In genetic algorithm based optimization technique the issue of voltage balancing technique and switching loss was not addressed [3]. In state space model, analysis of the harmonic distortion that is present in the NPP are not considered [4]. THD plays a major role in controller design for maintaining dc bus voltage balance. Soft switching technique proposes to minimize the switching loss of the inverter [5]. Various PWM and SPWM technique such as variable and constant switching frequency and phase shifted PWM and have been proposed [6, 7] but they don’t address the above mentioned problems in NPP. In PI controller technique the THD content in the output voltage is reduced down to 28%. Variation in the offset voltage is depend on the THD, average and peak to peak value of NP therefore it is necessary to minimize the THD content as much as possible.

The current study proposes the design of a NPP regulator using PI controller technique and Particle swarm optimization (PSO) technique to balance the capacitor. The purpose of regulator is to maintain the midpoint potential by adding offset voltage continuously. For PI controller technique the offset voltage is calculated by using the magnitude of third order harmonic content, total harmonic distortions (THD), peak-to-peak value and the average value in NPP. For regulator using PSO technique the mathematical equation describing the general neutral point current for three level NPC inverter is derived as a function of modulation index, power factor angle and offset voltage. PSO algorithm is used on the general neutral point current equation to obtain the offset voltage by keeping the neutral point current to minimum value. In both the technique dc-link capacitor voltage is maintained constant and distorted voltage at the neutral point (NP) and the switching losses in the inverter are reduced.

The main objective is to find the offset voltage using PSO algorithm and to form a closed loop control strategy by implementing PSO algorithm in the PI controller to maintain the capacitor voltage balance, here we are using two ways to minimize the NPP

1. NPP regulator designed using PI controller
2. NPP regulator designed using PI controller along with PSO technique

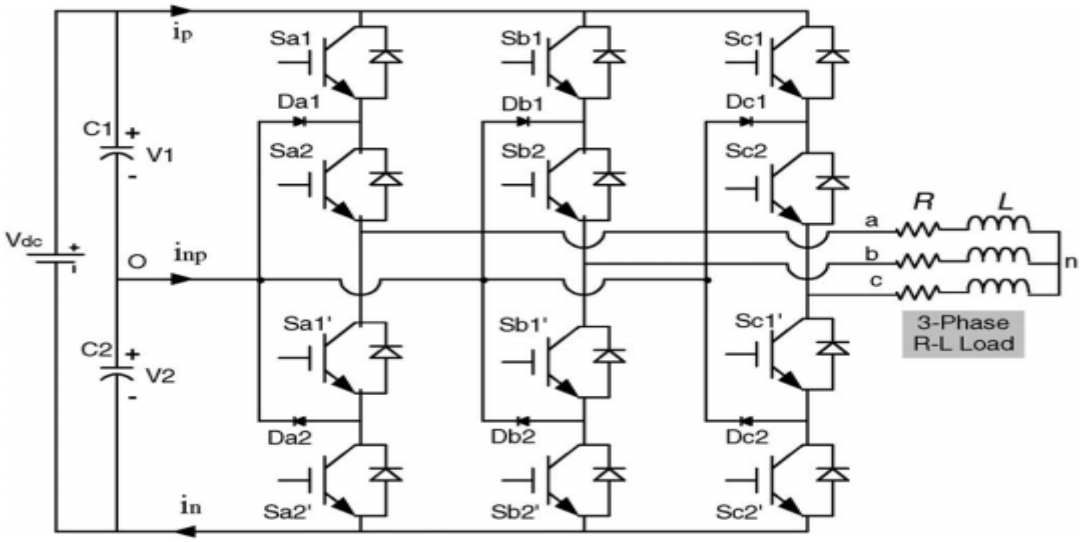


Figure 1(a): Three Phase NPC Inverter

Switching States of Three Level NPC Inverter

Table 1: Switching Sequence For Phase A

T1	T2	T1’	T2’	Output phase voltage (Va)
1	1	0	0	+Vdc/2
0	1	1	0	0
0	0	1	1	-Vdc/2

Section II presents the problem in the NPP due to unbalance dc-link capacitor voltage. Section III presents the control strategy of the inverter and procedure for design of the NPP regulator, PI controller and PSO controller. Section IV presents the simulation results.

Neutral Point Potential (NPP) Variation

Fig. 1(a)shows the three phase NPC inverter and Table. 1 shows the switching sequence for phase A.Due to unbalanced capacitor voltage inverter output current and

voltage waveforms are distorted. Switching stress also increases. Excessive imbalance in the capacitor voltage may lead to the failure of the inverter. Therefore it is necessary to control the NPP variation. To know the effect of imbalance the two capacitor values are intentionally made unequal and the results of output line voltage and phase voltage are compared with the balanced output voltage waveforms. Under the imbalance conditions second order harmonics and output voltage THD value are maximum.

A. Effect of NPP Variation

Phase voltage with large imbalance in dc-link

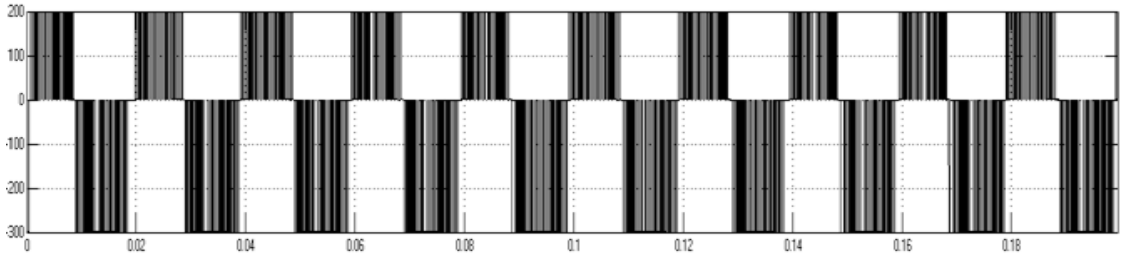


Figure 2(a): Phase Voltage with Large Imbalance In Dc-Link Without NPP Regulator

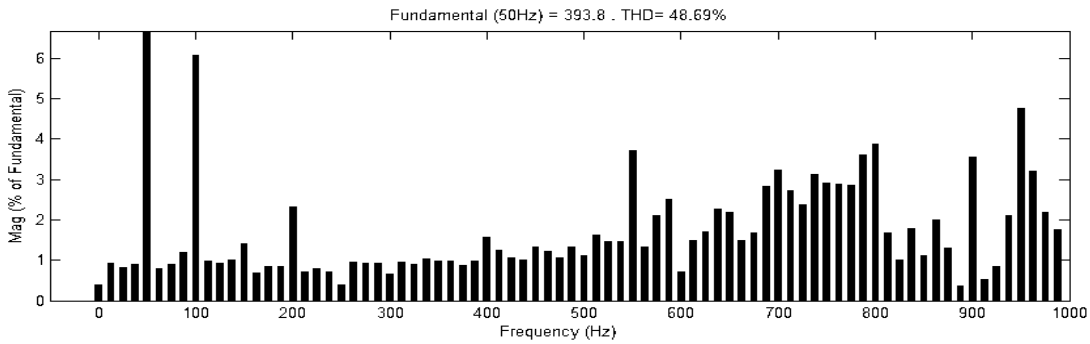


Figure 2(b): Total Harmonic Distortion (THD

Line voltage with large imbalance in dc-link

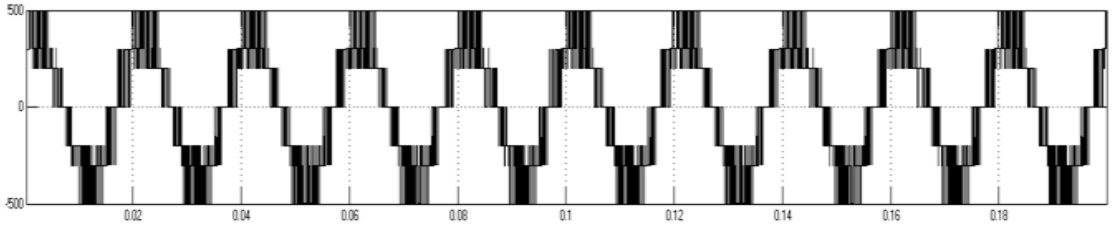


Figure 2(c): Line voltage with large imbalance in dc-link without NPP regulator

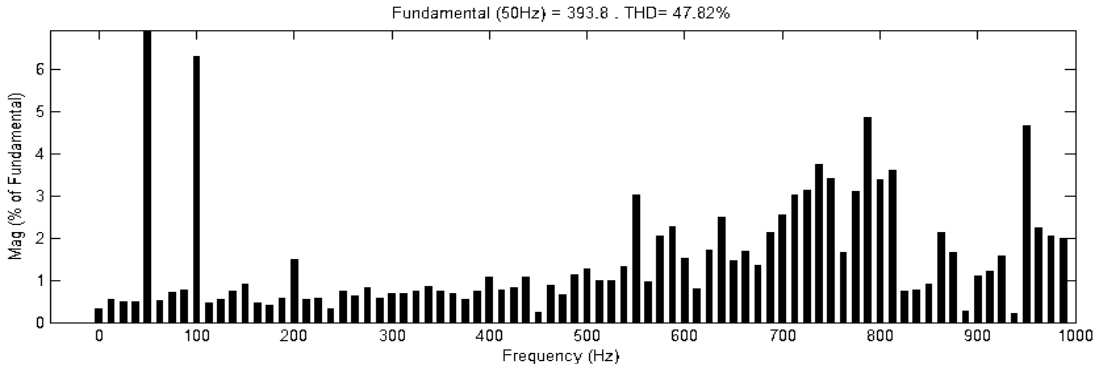


Figure 2(d): Total Harmonic Distortion (THD)

Fig. 2(a) and fig. 2(b) shows the outputwave form and THD of the phase voltage andFig. 2(c) and fig. 2(d) shows the outputwave form and THD of the line voltage under burst condition with imbalance in the dc-link voltage with Vdc1=200v and Vdc2=300v

Under imbalance conditions THD value of line voltage and phase voltage are tabulated below

Table 2: Shows The Effect of Imbalance on The THD

Vdc1(volts)	Vdc2(volts)	%THD Line voltage	% THD Phase voltage
200	300	47.82	48.69
250	**250**	**16.5**	**18.2**
300	200	54.6	59.1
400	100	63.7	69.16

From this study table. II clearly shows the effect of imbalance on the THD. The percentage value of THD in the line voltage is minimum for the balanced system when (Vdc1=250v and Vdc2=250v) and it has the maximum value for the unbalanced system (Vdc1=200v and Vdc2=300v)

Block Diagram

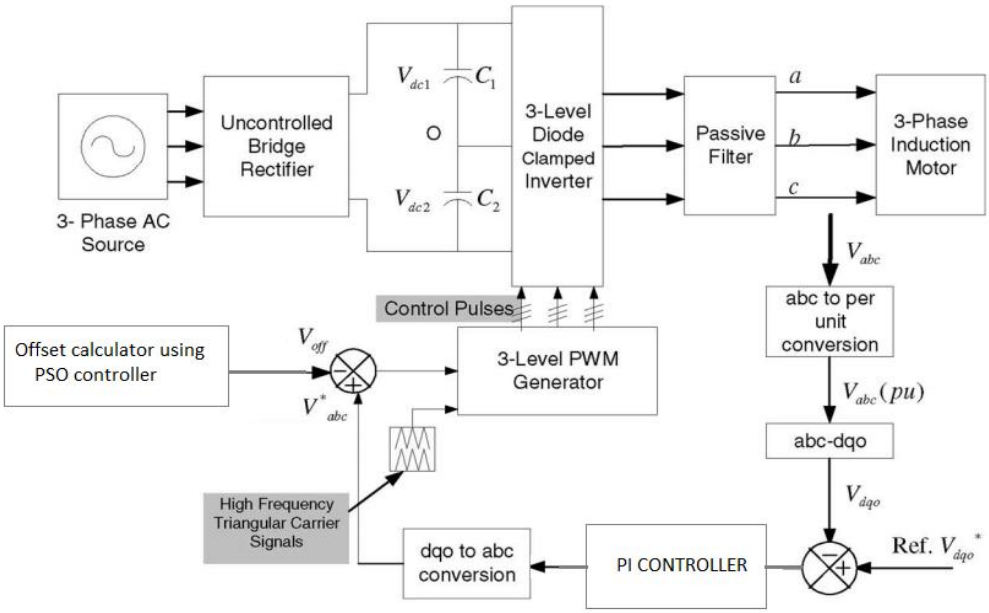


Figure 2(E): Block Diagram of NPC Inverter Using PI Controller Using PSO Technique

NPP Regulator

From [1] while design the control strategy of inverter the following aspects are consider 1) minimization of harmonics in the output voltage 2) switching loss should be reduced or reduce switching stress on the device and 3) ensuring voltage balancing of the capacitor

Fig. 2(e) consist of two control strategy one is NPP regulator using PI controller and other is NPP regulator using PI controller using PSO technique. In first control technique it consist of load side control loop and dc-link side control loop. Load side voltage is sensed and converted into per unit system by using two phase conversion per unit abc is converted into dqo-axis using following equations from [1]

$$Vd=2/3[VaSin(\omega t)+VbSin(\omega t-120^\circ)+VcSin(\omega t-240^\circ)]$$

$$Vq=2/3[VaCos(\omega t)+VbCos(\omega t-120^\circ)+VcCos(\omega t-240^\circ)]$$

$$Vo= (Va+Vb+Vc)/3 \quad (1)$$

Comparison between Vdqo with ref dqo voltage shows error signals in voltage which is given to the PI controller for generating command signals. Using three phase conversion dqo is converted into abc

$$Va=Vdsin(\omega t) + Vqcos(\omega t)+Vo$$

$$Vb=Vdsin(\omega t-120) + Vqcos(\omega t-120)+Vo$$

$$Vc=Vdsin(\omega t-240) + Vqcos(\omega t-240)+Vo. \quad (2)$$

The modulation index is calculated by using

m = (Vd² +Vq²)½

In dc side control loop both the capacitor voltage is sensed (ie.,Vnp = Vdc1 – Vdc2) and the error in the value is proposed through the PI controller. Offsetvoltage Voff is calculated in the offset calculator block by using following functions

Voff=f(NPPav, NPPp-p, NPPTHD, NPP3).

(Limits are set as 2% of the inverter line voltage for NPPp-p, 0.1% for NPPav, 1.5% for NPP3, and 4% for NPPTHD)

NPPav – average value of neutral point potential

NPPp-p – peak to peak value of NPP

NPPTHD – total harmonic distortion of NPP

NPP3 – third harmonic content in NPP

A. Design of PI controller

Complete block diagram of NPP regulator

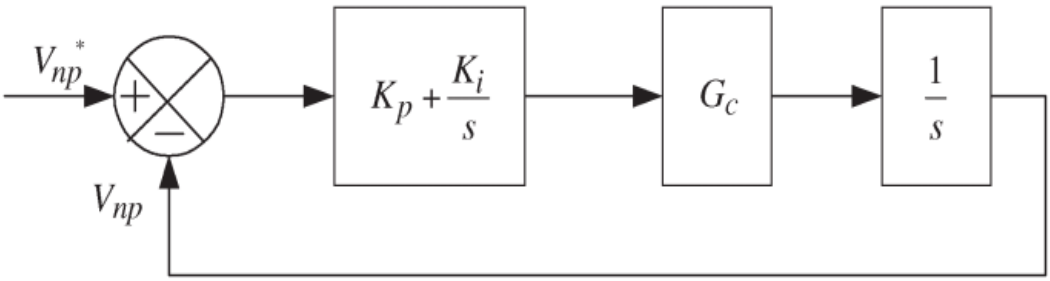


Figure 3(A): Simplified Block Diagram of NPP Regulator

The gain of the PI controller from[1]

G= Kp + (Ki / (sT+1))

The closed loop NPP regulator characteristic equation is given by

S + (Kp + Ki/s) əf /əVoff =0

For choosing the Kp and Ki value the complete closed block is tested with the step input to the transfer function. Transient step response for various PI controller parameter is shown in the table below from [1]

Table 3: NPP Regulator Performance Indices

S.NO	KpAC	KiAC	KpDC	KiDC	Settling Time(sec)	Overshoot %
1	10	50	0.1	0.1	2.0	20
2	50	0.01	0.1	0.01	0.06	9
3	0.1	10	1.0	0.01	0.18	12
4	100	0.01	10	0.1	2.1	15

From the table. III the value of Kp and Ki are determined for low % overshoot and settling time values where Kp denotes the voltage response and Ki denotes damping factor.

B. Design of PSO Controller

The theory of PSO lies in searching each particle toward itspersonal best (pbest) and the global best (gbest). It provides a population-based search proceduregetting the best solution from the problem by taking theparticle and searching them in the solution space with acceleration randomly weighted at each step. The particles searching in the solution space based on the simple mathematical equation describing the velocity and position of the particles. The best solution (fitness) achieved by any other particle in the solution space is called personal best (pbest) and another best overall achieved from neighbourhood valuein the pbest is called global best (gbest).

PSO gives better accuracy when compared to the other optimization techniques. Objective is to derive the offset voltage using PSO algorithm which is obtained by deriving the system transfer function. Overall fundamental period the average value of NP current is given by following equations from [1]

$$Inp = 2/3\int_0^{2\pi}[ua(t)ia(t) + ub(t)ib(t) + uc(t)ic(t)]\, dt \quad (3)$$

Ua(t), ub(t), uc(t) are the modulating signals. Neutral point current Inp also influenced by the three level modulating signal which adds offset voltage to the NPP regulator based on this effect the average NP current is given by

$$\mathbf{Inp=3/\pi\ cos(\varphi)[m\beta-(2Voff+msin\beta)cos\beta}(4)$$

Where, $\beta = \pi/2 - \cos{-1}(Voff/m)$

$$\mathbf{Inp=f(m,\ \varphi,\ Voff)}$$

Where m – Modulation index

φ – Power factor angle Voff – offset voltage

Therefore neutral point current NP is the function of modulation index, offset voltage and power factor angle. Variable offset voltage signal are calculated by using the equation (4) by minimizing the function parameters such as modulation index, load power factor angle and neutral point current.

The velocityequation according to mathematical model is given by

$$\mathbf{U_i^{k+1} = mU_i^k + w_1\ randm_1\ (\ldots) * (pbest_i - s_i^k) + w_2\ randm_2\ (\ldots) * (gbest - s_i^k)}$$

Where, u_i^k - velocity of agent i

m -weighting function

w -weighting factor

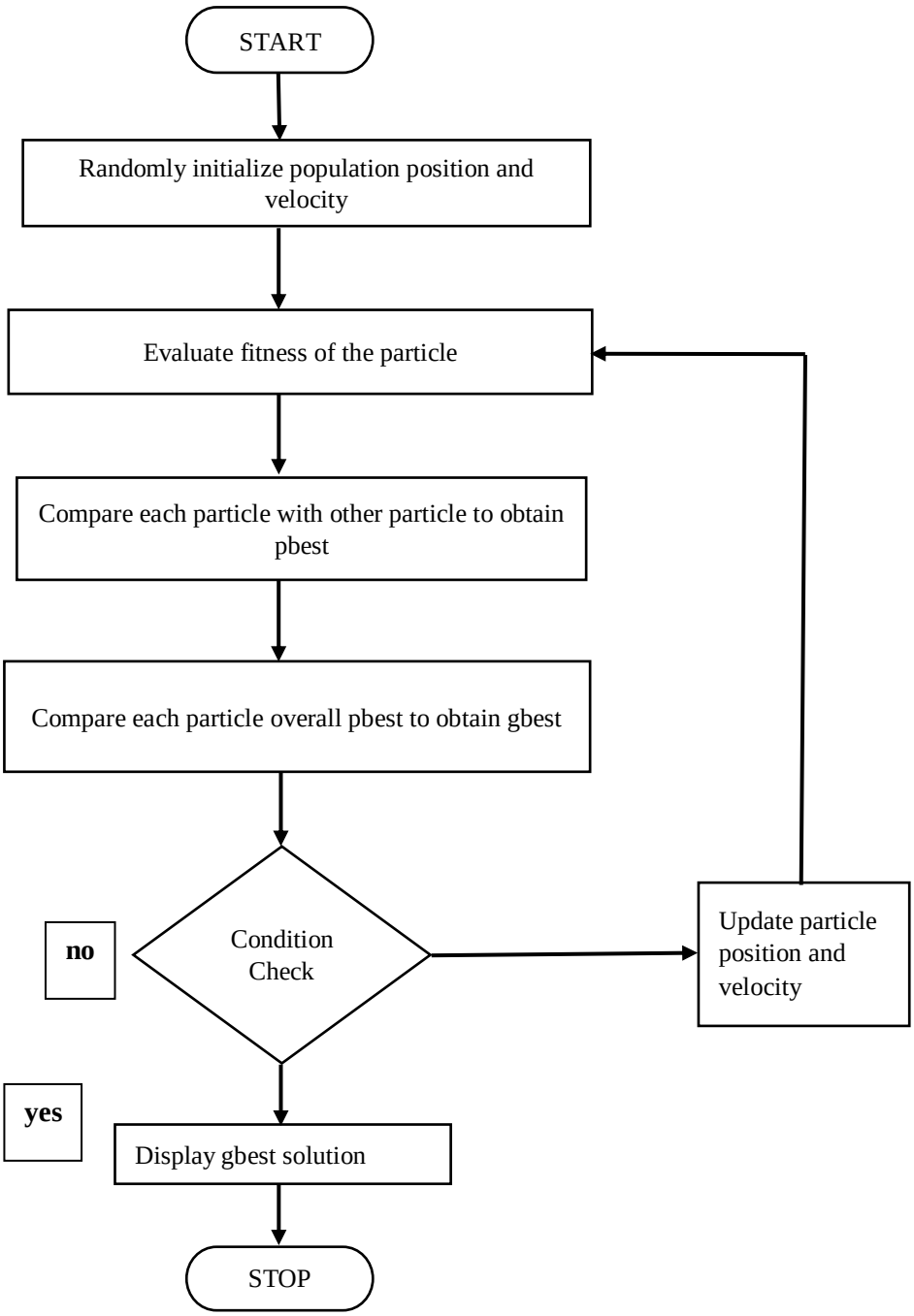
randm-uniform random number between 0 and 1

s_i^k - current position of agent i at iteration k

$pbest_i$– personal best solution of agent i

gbest – global best solution

PSOALGORITHM Flowchart



Offset Voltage Calculation Using PSO Algorithm

Under loaded conditions by taking modulation index (m=1) and power factor angle (φ=.85) the offset voltage are calculated using Particle Swarm Optimization (PSO) algorithm with reduced NP current are shown below

```
Iteration 100    4.124494253782226e-004

Offset Voltage :  0.088249
Elapsed time is 4.976350 seconds.
>> pbestsolution

pbestsolution =

   0.174885437171165
   0.282251958602934
   0.356965081130475
   0.080884909928809
   0.215080420522664
   0.093351557269829
   0.179792661770671
   0.207795710216063
   0.288176542085365
   0.236241257181881

>> gbestsolution

gbestsolution =

   0.088248630740030
```

For different values of modulation index the variable offset voltage under loaded condition and unity power factor angle with reduced NP current are tabulated in table

Table 4: Calculation of Offset Voltage

Modulation index (m)	Load angle	Offset voltage
1	0.85	0.088
0.9	0.85	0.156
0.8	0.85	0.212
0.7	0.85	0.295
0.6	0.85	0.402

Form the table. IV it shows that the offset voltage is varied from the range of 0 to 0.4 for the unity power factor angle with different values of modulation index

Simulation Result

A. Simulation Result of Three level NPC inverter using Neutral Point Potential Regulator using PI controller

Closed loop simulation has done for NPC inverter using NPP regulator using PI controller. By adding continuous offset voltage midpoint potential is regulated using NPP regulator. By comparing the dc side controller and ac side controller switching sequence is produced for the inverter using PWM technique.

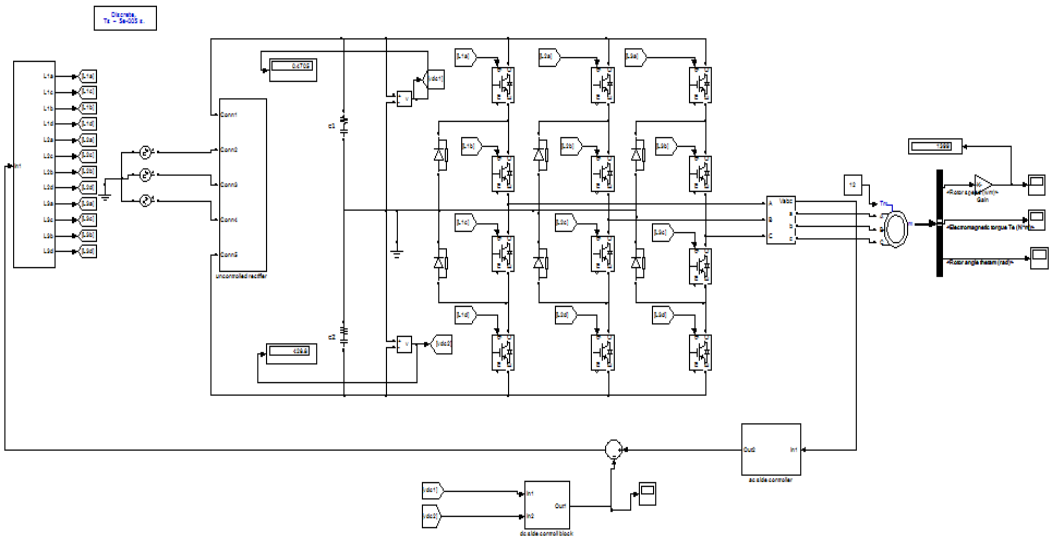


Figure 4(a): Three level NPC inverter with NPP using PI controller

Fig. 4(a) shows the simulation block diagram for NPC inverter using NPP regulator using PI controller. The operation ofthe closed loop controller is described in the chapter II

Effect of NPP when Regulator Using PI Controller:

Line voltage waveform for phase A

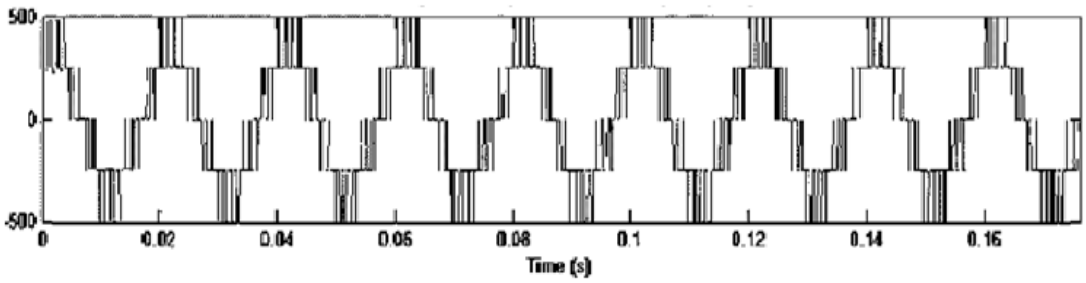


Figure 4(b): Line voltage with large imbalance in dc-link with NPP regulator using PI controller

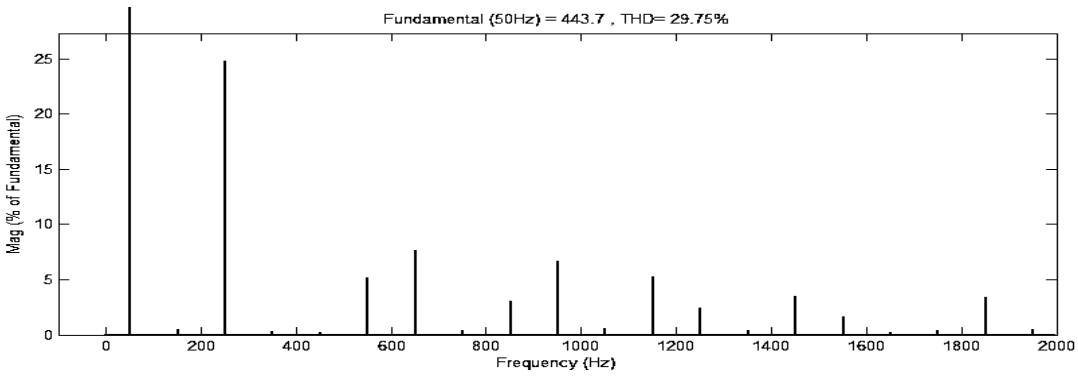


Figure 4(c): Estimation of THD

Fig. 4(b) and fig. 4(c) shows the output line voltage waveform and THD percentage when large imbalance in the dc link capacitor voltage. NPP without the regulator has a nonzero average value and contains 47.82% THD. The distortions present in NPP also affect the inverter performance. When the capacitor voltage Vdc1=200v and Vdc2= 300 the line voltage waveform and THD for NPPwith regulator using PI controlleris shown in the fig 4(b) and fig 4(c)even though the capacitor voltage are imbalance, a balanced line voltage waveform without distortion is generated using PI controller which contains THD of 29.75%

B. Simulation Result of Three level NPC inverter using Neutral point potential regulator using Particle Swarm Optimization (PSO)

Closed loop simulation has done for three level NPC inverter with NPP regulator using PI controller along with PSO technique.by minimizing the neutral point current equation using PSO, the desired offset voltage is calculated and comparing these offset voltage with the NPP regulator switching sequence are produced for the inverter using PWM. Which maintains the capacitor voltage balanceFigure 4. (d) Shows the simulation block diagram of three level NPC inverter with NPP regulator using PSO technique the operation of the closed loop controller is described in the chapter III

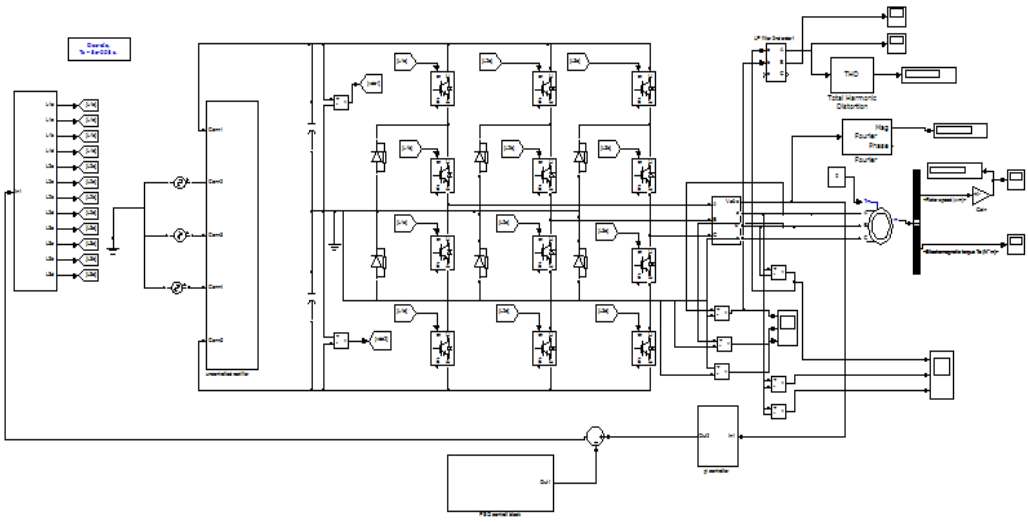


Figure 4(D): Three Level NPC Inverter With NPP Regulator Using PSO Technique

Effect of NPP when regulator using PSO technique:
Line voltage waveform for phase A

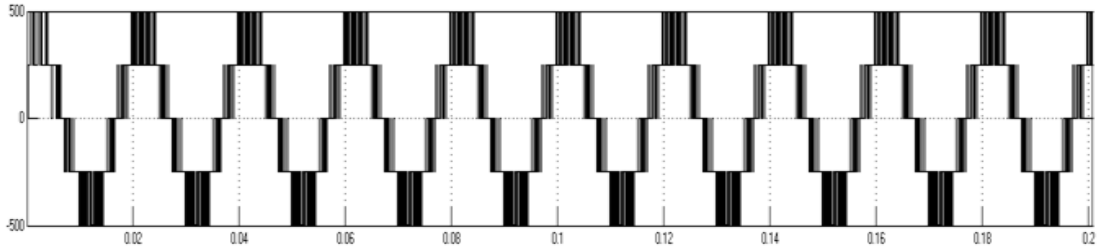


Figure 4(e): Line voltage waveform with large imbalance in dc-link with NPP regulator using PSO

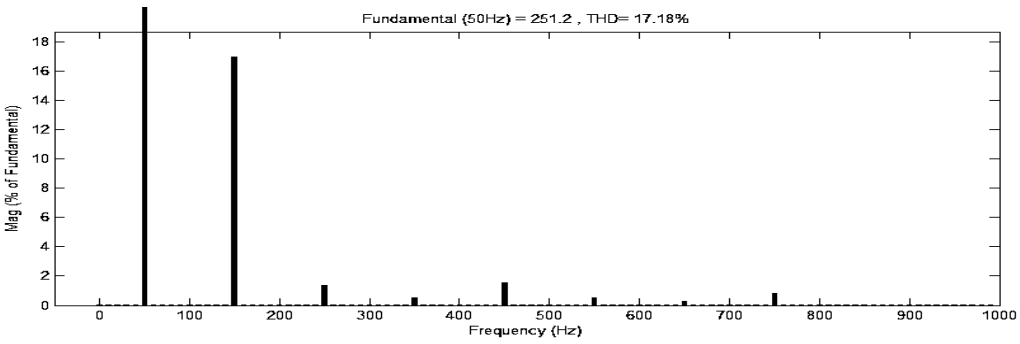


Figure 4(f): Estimation of THD

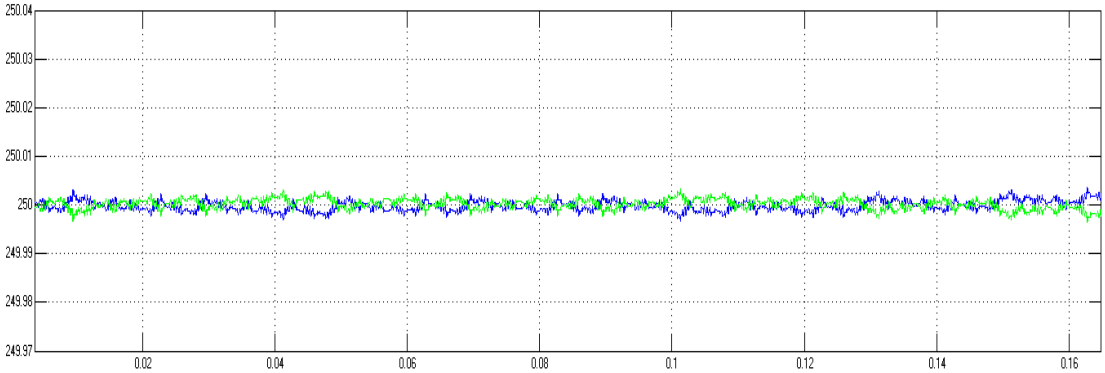


Figure 4(g): Dc-link voltage (Vdc1 and Vdc2) with proposed regulator using PSO

The line voltage waveform and harmonic spectrum of NPP regulator using PSO technique is shown in Fig. 4(e) and fig. 4(f) and dc link capacitor voltage waveform with proposed regulator using PSO are shown in fig. 4(g)The important outcome from the proposed NPP regulator using PSO is to minimize distortions and voltage present in NPP, even though the capacitor voltage are unbalanced a balanced voltage level in the output line voltage with minimum THD value are obtained. NPP without PSO technique has a nonzero average value and contains 29.75% THD. The distortions present in NPP also affect the inverter performance. NPP regulator using PI controller using PSO technique contains the minimum value of THD 17.18% in the line voltage

Simulation Results

Table 5: Tabulation of Simulation Results

NPC INVERTER	Vdc1	Vdc2	% THD (line voltage)
Without NPP regulator	200	300	47.82
NPP regulator using PI controller	200	300	29.75
NPP regulator using PI controller using PSO technique	200	300	17.18

Conclusion

The objective of the present work is to control THD percentage content of the inverter by reducing the Neutral Point Potential. Three level NPC inverter with NPP regulator using PI controller and NPP regulator using PI controller using PSO technique is simulated and the THD values for the line voltage are listed in the table. V From the simulation results it clearly indicates that the NPP regulator using PSO has the

minimum THD of 17.18% when compared to the simulation results with NPP regulator without PSO technique has the THD of 29.75%. The imbalance presented in dc link with the proposed NPP regulator using PSO is symmetrical and reduce the Neutral Point Potential to the minimum value. The dynamic performance of the proposed regulator using PSO is studied by changing the load. The THD can be further reduced by adding filter circuits

References

[1] PradyumnChaturvedi, Shailendra Jain, and Pramod Agarwal, Feb. 2014, ‘’Carrier-Based Neutral Point Potential Regulator With Reduced Switching Losses for Three-Level Diode-Clamped Inverter, ”IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, 61(2).

[2] E. Sakasegawa and K. Shinohara, 2001, “Compensation for neutral point potential in three-level inverter by using motor currents,”Trans. Inst. Elect. Eng. Jpn.,121-D (8), pp. 855–861.

[3] N. Yousefpoor, S. H. Fathi, N. Farokhnia, and H. A. Abyaneh, Jan. 2012,“THD minimization applied directly on the line-to-line voltage of multilevel inverters,” IEEE Trans. Ind. Electron., 59(1), pp. 373–380.

[4] A. Yazdani and R. R. Iravani, Apr. 2005, “A generalized state space averaged model of the three-level NPC converter for systematic DC voltage balancer and current controller design,”IEEE Trans. Power Del., 20(2),pp. 1105–1114.

[5] P. Kollensperger, R. U. Lenke, S. Schroder, and R. W. De Doncker, Sep. 2007, “Design of a flexible control platform for soft-switching multilevel inverters, ”IEEE Trans. Power Electron., 22(5), pp. 1778–1785.

[6] P. Palanivel and S. S. Dash,Sep. 2011, “Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques,”IET Power Electron., 4(8), pp. 951–958.

[7] P. K. Chaturvedi, S. Jain, and P. Agarwal,Apr. 2011, “Reduced switching loss pulse width modulation technique for three-level diode clamped inverter,”IET Power Electronics. 4(4), pp. 393–399,

[8] R. Maheshwari, S. Munk-Nielsen, and S. Busquets-Monge,May 2013, “Design of neutral point voltage controller of a three-level NPC inverter with small DC link capacitor,” IEEE Trans. Ind. Electron., 60(5), pp. 1861–1871.

[9] P. M. Meshram, Associate professor, Y.C.C.E, May 2012 “Optimal Tuning of PI Controller for Speed Control of DC motor drive using Particle Swarm Optimization, ” International Conference onElectrical Machines and Systems.

[10] A. K. Al-Othman and Tamer H. Abdelhamid, 2008, ”Elimination of Harmonics in Multilevel Inverters with Non-Equal DC Sources Using PSO2008 13th” International Power Electronics and Motion Control Conference (EPE PEMC).