International Journal of Applied Engineering Research
ISSN 0973-4562 Volume 10, Number 7 (2015) pp. 16475-16482

http://www.ripublication.com

Dynamic Power Reduction For VLSI Circuit Using Delay Insertion Methodology

Suganya.S, Aravind. T and Sivakumar.D

ME-VLSI Design Saveetha Engineering College
2suganya2@gmail.com
Department of ECE Saveetha Engineering College
aravindthangavelme@gmail.com
Assistant Professor Kings Engineering College
janeshsivakumar@gmail.com

Abstract–

The important design specification in digital designs in terms of area and throughput is power consumption. Requirementof low power is a mandatory criterion in many applications. In much digital designsdynamic power consumption is high due to unwanted switching activity. The propagation delay is occurred during the data transmission, limits the performance due to non-uniform interconnection paths between the circuits. This results in glitches on the outputof the circuit. Glitching problem is a resultant of NAND-based digitally controlled delay-lines (DCDL). Currently a glitch-free NAND-based DCDL is used to overcome the limitation of glitching problem. However when the number of nDCDL is increased, the number of gates should be increased with propagation delay. The increase in number of gates can be reduced by replacing with Razor flip flop consists of single flip flop with loop based logic.

Index- DELAY, DCDL, RAZOR FLIP FLOP, nDCDL

I Introduction

Power consumption holds the key in utilising the area and throughput in digital designs. It is remarkably important for field programmable gate arrays (FPGAs). FPGA designs consume more power than application-specific integrated circuits (ASICs) .The impact of power must have to be known to all digital circuit designers. The attempt to reduce the power at the design level or at the mapping of technology

level is evident in recent times. The control over the gate gives exceptional reduction in the power consumption.

By reducing the signal glitching considerable amount of power can be reduced in FPGAs. Path balancing is an effective method for minimising signal glitches in digital design.

Some of the techniques reduce the propagation delay, infinite DCDL is used to reduce the delay with two control signals [1]. The power consumption is 51.7mw. Delay can be avoided by driving two delay lines which are digitally controlled and synthesized by a modulator [2]. An inverter along with an inverting multiplexer operating in the certain frequency is used to construct the above mentioned technique. The power dissipation is 44 mW @ 1.27 GHz. This technique uses the coarse as well as the fine delay blocks of the digitally controlled oscillator [3]. Three-state inverters (TINV) are used to enable the connection between each element. The power consumption is 15.7mW. A digital control mechanism in addition to a ring oscillator is used in All-Digital Phase-Locked Loop (ADPLL) architecture [4] to reduce the delay operates with in the certain frequency range. With a 3.3-V power supply the ADPLL dissipates power in the range of 100mW (at 500MHz)..

II Power dissipation

The CMOS circuits consume power in both static and dynamic modes.

1. **Leakage current** depends on the technology used in its construction, and parasitic diodes contribute for the reverse bias current occurs between source and drain diffusions and the bulk region in case of a MOS transistor.
- Sub-threshold current is a major criterion in submicron fabrication process. This current is the resultant of the inversion charges that occur at the gate voltages way below the threshold voltage.
2. **Short-circuit current** is a resultant of the DC path between the supply rails throughout output transitions,
3. **Switching current**: it is dissipated during the charging of the capacitive loads first and then the discharging of capacitive loads as resultant of change in logics.

III Switching Activity and Dynamic Power

The modeling of Dynamic power can be done by [5]:

$$P_{Dynamic} = 0.5 f V_{dd}^2 \sum_{i=1}^{n} C_i S_i$$

where,

n - Total number of gates,
f - Clock frequency,
V_{dd} - supply voltage,
C_i - load capacitance for gate *i*, and

S_i - switching activity for gate *i*.

Whenever a signal switches from 1 to 0 or 0 to 1 it is accounted for switching activity. The functional transitions and glitches both are included in switching activity. Therefore, reducing glitches is one method which reduces dynamic power.

IV Path Balancing

The interconnection between the circuits is non-uniform due to variation that occurs in the input signal. Delay occurred due to variation in the arrival time of the input signals. Delay between the circuits creates unwanted switching activity this introduces glitches. The glitches increase the total dynamic power consumption of the circuit

To overcome this problem path balancing technique is used. In path balancing technique non-uniform interconnection between circuits are made regular by delay insertion methods. Sense amplifier senses the non- uniform data transmission and activates the control signal, depends on the propagation delay of data. Sense amplifier is used to find the delay value. Unwanted switching activity is reduced by inserting the delay in the non-uniform circuit. By using delay insertion methodology technique dynamic power consumption is reduced.

The Architecture overview is show in Fig. 1.

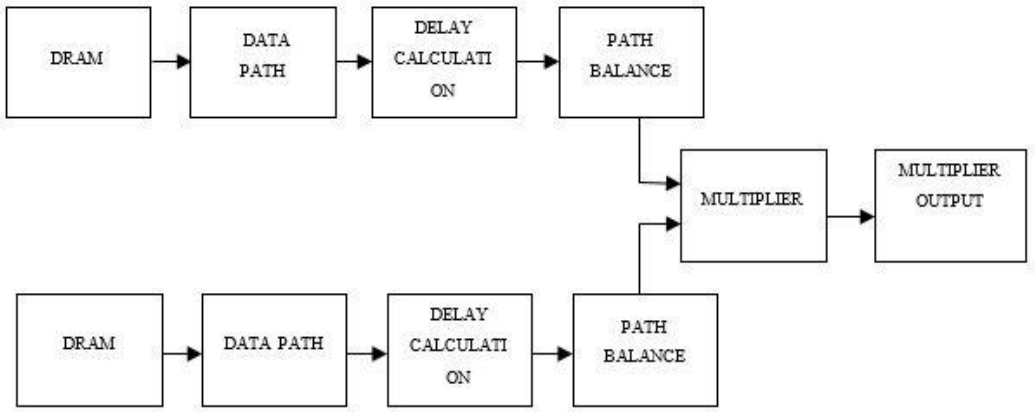

Fig.1.Architecture overview

Interconnections between LUT's:

- Below circuit shows interconnection between three CLB units.
- CLB1 and CLB3 has equal width whereas CLB1 and CLB2 has different sizes of width.
- Time delay between CLB1 and 2 has been calculated as follows:

$$T_{delay} = T_H - T_L$$

Every bit that transfers from CLB1 will reach CLB3 at same time delays because there exists uniform wire interconnect between CLB1 & CLB2. But for CLB1 & CLB2, there are non-uniform interconnections so that data transfer between these two blocks became non-uniform. The 1st interconnect has shortest length and final has long interconnect. The Block diagram of non-uniform data transmission is show in Fig. 2. Thus time delay between B_0 and B_3 should be as follows:

$$T_{delay} = T_H - T_L$$

From above discussions, it is clear that if data transmitted from CLB1 to CLB2 time delay should be non-uniform that's leads four time's excitation for CLB2 that increases switching property. Although switching activities leads to more power consumption. Thus conventional FPGA design has more interconnection delays that increase both static and dynamic power. Reduce non uniform switching activities between CLB's, we add a delay insertion circuit that can calculate delays between transferred bit and insert delay buffers between considered logical units. The sensing unit always scans bit lines for data transfer occurrence. While data reaches sensing unit, it is estimated for the number of delay elements to be insert across interconnects. Its barely reduces switching activity between CLB's that reduces state excitement of FPGA's to reduce total thermal power consumption.

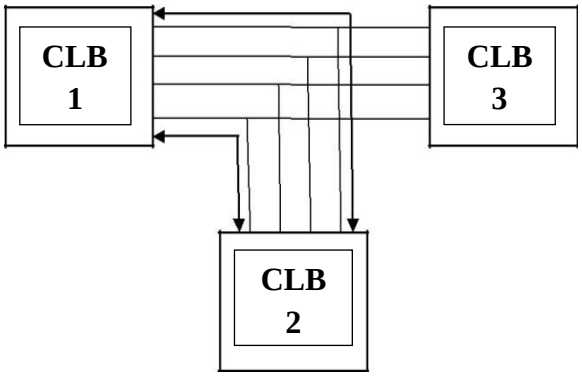

Fig. 2. Delay calculation between CLBs

The circuit shown above describes the insertion of delay elements between various interconnects.

V DCDL TOPOLOGY

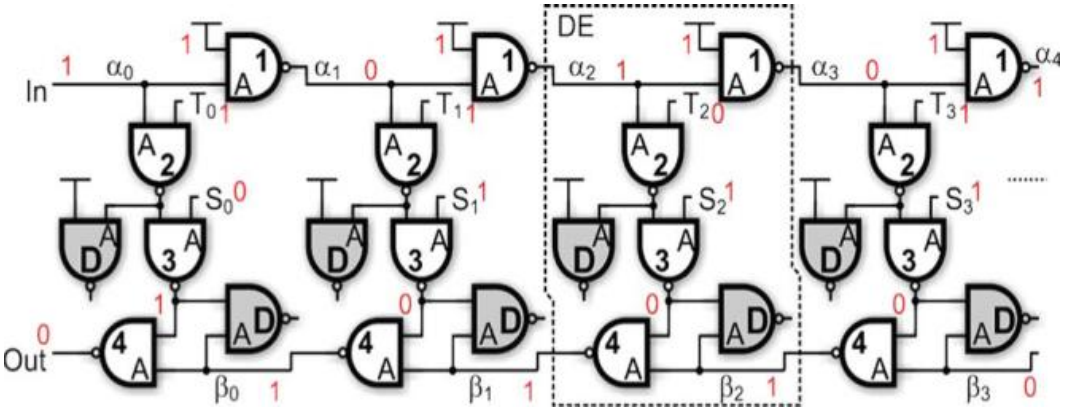

Fig. 3.DCDL Topology (a) inverting topology

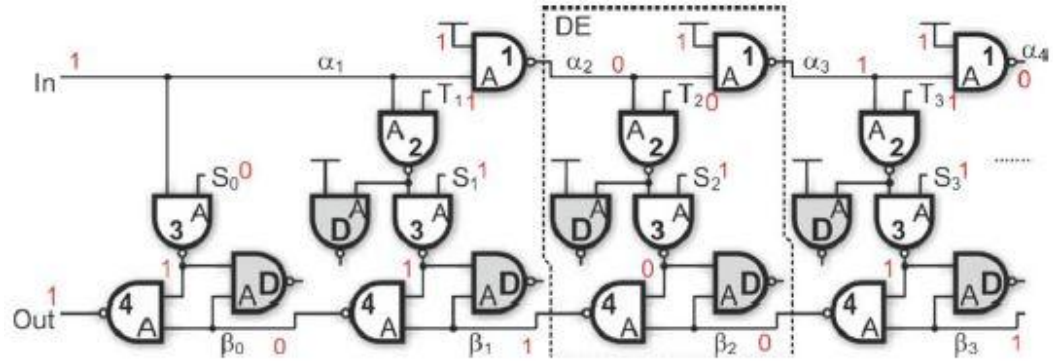

Fig. 4.DCDL Topology (b) non-inverting topology

This circuit consists of sequential equal delay elements, each comprises of sixNAND gates. The Block diagram of DCDL Topology is show in Fig. 3. In the figure "A" represents the swift input whereas "D" represents the dummy cell which is added balance the load. The Block diagram ofDCDL Topology is show in Fig. 4. All NAND gates get the same load and delay. By using DCDL topology can evade glitching problem, when the activity of delay control-bits is correlated with the activity of inputsignal. The glitching problem is completely evaded. The control bits consists of [1] pass state, turn state ad post- turn state with S_i and T_i. The DCDL topology acts as a delay insertion methodology by using delay insertion method. We can reduce glitching problem but simultaneously increases the number of gates with respect to propagation of delay. So that power consumptin also increases

VI RAZOR FLIP FLOP TOPOLOGY

Razor flip flop is proposed to afford error-free operation between logical block.Delay insertion methodology uses Razor flip flop for uniform data transmission.Razor flip flop consist of multiplexer, latch, single flip flop with feedback loop, controller, switch. The Block diagram of razor flip flop is exposed in Fig 5

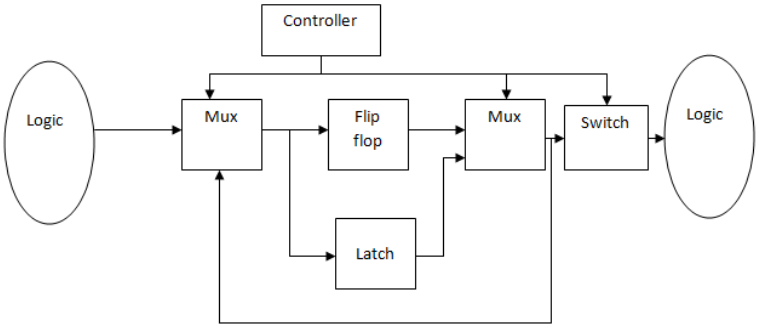

Fig. 5. Block diagram of razor flip flop

- The controller module controls number of loops based on delay value defined by sense amplifier.
- Multiplexer will take decision to by-pass data or loop back the data between logical units.
- Flip flop is edge sensitive so it inserts delay for one clock pulse.
- Latch is level sensitive, that adjust phase delays.

ANALYSIS OF MODEL SIM

In the existing process, four DCDL is considered to reduce the glitches. If only two DCDL is turned ON among the four DCDL present, then some of the glitches produced in the circuit is reduced. If all DCDL is turned ON then total glitches produced in the circuit gets reduced. The simulation waveform of DCDL Topology is show in Fig. 6.Since number of DCDL increases to reduce the increasing glitches power consumed by the DCDL to turn ON and area occupied by DCDL also gets increased.

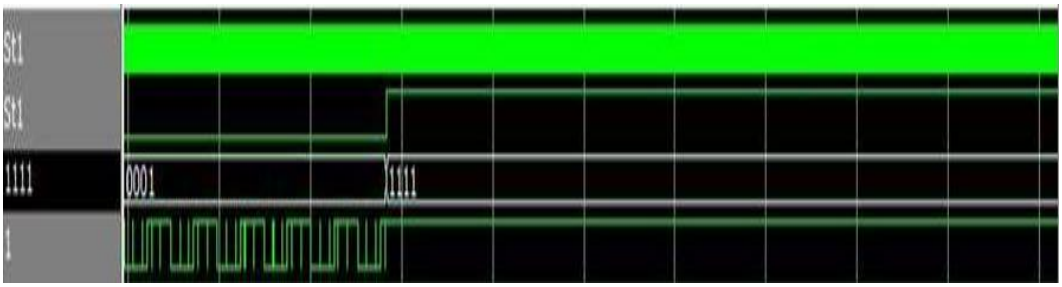

Fig. 6.Existing system simulation waveform

Razor flip flop is used to reduced glitches using feedback loop. This process depends on the control code value. The simulation waveform of Razor flip flop is show in Fig. 7.

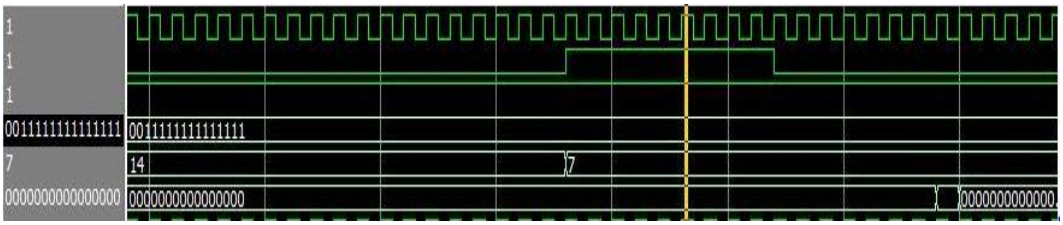

Fig.7.Proposed system simulation waveform

DCDL AND RAZOR ANALYSIS REPORT

TABLE.1 COMPARISON RESULT DCDL AND RAZOR FLIP FLOP

PARAMETER	DCDL	RAZOR FLIP FLOP
DYNAMIC POWER REDUCTION	51.7 mw	14.19mw
TOTAL LOGIC ELEMENT	17%	10%
PROPOGATION DELAY TIME	1.3%	1.1%

Delay insertion methodology using razor flip flop occupies 7% less area and 37.51Microwatt less power compared to existing method. Also delay of the proposed system is reduced to 0.2% than DCDL.

CONCLUSION

Dynamic power is reduced by using delay insertion methodology of razor flipflop, also total area of delay insertion methodology using Razor Flipflop Topology is low compared to the existing DCDL topology.

The existing delay insertion methodology of DCDL is compared to the proposed delay insertion methodology of razor flip flop in terms of area and power. Delay insertion methodology using razor flip flop occupies 7% less area and 37.51Microwatt less power compared to existing method. Also delay of the proposed system is reduced to 0.2% than DCDL.

Further power consumption can be reduced by using Embedded Transition Inversion

REFERENCES

[1] Davide De Caro, Senior Member, IEEE Glitch-Free NAND-Based Digitally Controlled Delay-Lines, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 21, NO. 1, JANUARY 2013

[2] D. D. Caro, C. A. Romani, N. Petra, A. G. M. Strollo, and C. Parrella, "A 1.27 GHz, all digital spread spectrum clock generator/synthesizer in 65 nm CMOS," IEEE J. Solid-State Circuits, vol. 45, no. 5, pp. 1048–1060, May 2010.

[3] K. H. Choi, J. B. Shin, J. Y. Sim, and H. J. Park, "An interpolating digitally controlled oscillator for a wide range all digital PLL," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 56, no. 9, pp. 2055–2063, Sep.2009..

[4] C.C.Chung and C.Y.Lee ,"An all-digital phase-locked loop for high speed clock generation," IEEE J.Solid-State Circuits, Vol.38,No.2,pp.347-351,Feb.2003

[5] QuangDinh and demingchen,"A routing approach to reduce glitches in low power FPGAs"

[6] F. Lin, J. Miller, A. Schoenfeld, M. Ma, and R. J. Baker, "A register controlled symmetrical DLL for double-data-rate DRAM," IEEE J. Solid-State Circuits, vol. 34, no. 4, pp. 565–568, Apr. 1999.

[7] L.Wang, L. Liu, and H. Chen, "An implementation of fast-locking and wide-range 11-bit reversible SAR DLL," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, no. 6, pp. 421–425, Jun. 2010.

[8] J. S. Wang, C. Y. Cheng, J. C. Liu, Y. C. Liu, and Y. M. Wang, "A duty cycle distortion tolerant half delay line low-power fast lock in all digital delay locked loop," IEEE J. Solid-State Circuits, vol. 45, no. 5,pp. 1036–1047, May 2010.

[9] B. M. Moon, Y. J. Park, and D. K. Jeong, "Monotonic wide-range digitally controlled oscillator compensated for supply voltage variation,"IEEE Trans. Circuits Syst. II, Exp. Briefs, Vol. 55, No. 10, pp.1036–1040, Oct. 2008.

[10] S. Damphousse, K. Ouici, A. Rizki, and M. Mallinson, "All digital spread spectrum clock generator for EMI reduction," IEEE J. Solid- State Circuits, vol. 42, no. 1, pp. 145–150, Jan. 2007. 46

[11] C.C.Chung and C.Y.Lee ,"An all-digital phase-locked loop for high speed clock generation," IEEE J.Solid-State Circuits, Vol.38,No.2,pp.347-351,Feb.2003

[12] T. M. Matano, Y. Takai, T. Takahashi, Y. Sakito, I. Fujii, Y. Takaishi, H. Fujisawa, S.Kubouchi, S. Narui, K.Arai,M.Morino, M.Nakamura, S. Miyatake, T. Sekiguchi, and K. Koyama, "A 1-Gb/s/pin 512-Mb DDRII SDRAM using a digital DLL and a slew-rate-controlled output buffer," IEEE J. Solid-State Circuits, vol. 38, no. 5, pp. 762–768, May2003.