Design and Simulation of A New Topology Boost Inverter To Run Home Load Appliances

Pasupulati Babu Rao¹, F. T. Josh²

¹PG Student, Dept. Electrical & Electronics Engineering, Karunya University
²Asst. Professor, Dept. Electrical & Electronics Engineering, Karunya University
¹baburao.p999@gmail.com
³josh@karunya.edu

Abstract

The generation of a voltage range using renewable energy sources, like PV CELL, is influenced by environment, temperature, light, and so on. The System should adapt to wide input voltage and have buck boost ability. Based on the structure of AC/AC unit. In this paper presents a novel active buck boost inverter network for wide input voltage, by this we can say that buck boost conversion can be done in a quasi-single stage inverter. The ac/ac unit composed of active switches is utilized to perform boosting the voltage without introducing passive elements, which favors the system efficiency and power density.

Keywords: Photovoltaic, Single stage inverter, AC/AC unit, buck boost.

Introduction

Traditionally DC to AC power conversion can takes place in two ways. One is voltage source inverter (VSI) and other one is current source inverter (CSI).VSI having its own limitations, like output of AC is less than the input of DC. To overcome this drawback we are using a technique called Unipolar with PWM technique it will doubling the switching frequency. But conventionally we are having two techniques they are using cascaded structure and line frequency transformer.

Recently various single stage inverter have been proposed Z-Source inverter can boost the voltage using the additional passive network and advantage of shoot through problem [1]. Active Buck Boost inverter have the advantage of buck and boost the voltage with in a quasi-single stage inverter using a using a logic control circuit [2].

The previous solutions having their own limitations like additional passive network, logic gate control circuit etc.to overcome these problems we wrote a program instead of control circuit by this complexity of control circuit design will eliminated. And efficiency will same.

Block Diagram

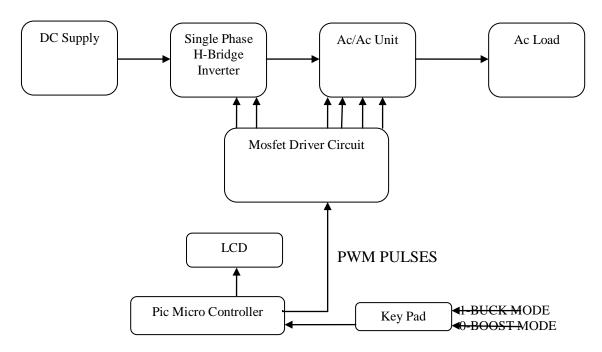


Figure 1: Block Diagram For Hardware Model

The above block diagram shows the hardware implementation model. Supply is DC is given to single phase H-Bridge inverter from inverter to load through AC/AC unit. Here we are using mosfet switches in both inverter and unit. For the inverter and unit we built the driver circuit named as mosfet driver circuit. Input for driver circuit is taken from PIC microcontroller. Input of PIC microcontroller is KEYPAD. If KEYPAD high then it will acts as a buck mode, if KEYPAD is low then it will acts as a boost mode, monitoring will be done using LCD display.

Circuit Diagram

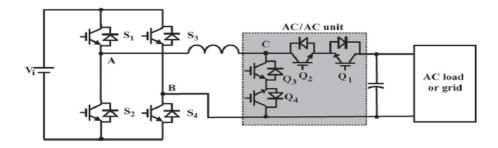


Figure 2: Active Buck Boost Full Bridge Inverter

The above circuit diagram describes single phase full bridge inverter (DC to AC) and AC/AC unit through inductor and capacitor connected to load. Pulses can be generated using program instead of control circuit. So, by this we can say that complexity of designing the control circuit will reduce and improving the performance of overall system.

```
Program
  #include<pic.h>
  #include"pic_lcd8.h"
  #define pulse1 RB0
  #define pulse2 RB1
  #define pulse3 RB2
  #define pulse4 RB3
  #define pulse5 RB4
  #define pulse6 RB5
  #define button1 RE0
  #define button2 RE1
  unsigned int i,x;
  void main()
  ADCON1=0x02;
  TRISB=0x00;
  TRISC=0x80;
  TRISD=0x00;
  TRISE=0X07;
  GIE=1;
  PEIE=1;
  TMR1IE=1;
  TMR10N=1;
  TMR1H=0xFe;
  TMR1L=0x0b;
  Lcd8_Init();
  while(1)
  Lcd8_Decimal3(0x80,i);Lcd8_Decimal2(0x88,x);
  if(!button1){while(!button1);x=0;Lcd8 Display(0xc0,"BOOST MODE ",16);}
        if(!button2){while(!button2);x=1;Lcd8_Display(0xc0,"BUCK
  else
                                                                   MODE
  ",16);}
  void interrupt pulse ()
      if(TMR1IF)
```

```
if(!x)
             i++;if(i>20)i=0;
             if(i>=0\&\&i<=10)\{pulse1=1;\}
             else pulse1=0;
             if(i>=11){pulse2=1;}
             else pulse2=0;
             if(i>=0&&i<=20)pulse3=1;
             else pulse3=0;
             if(i>=0&&i<=20)pulse4=1;
             else pulse4=0;
             if(i>=13&&i<=17)pulse5=1;
             else pulse5=0;
             if(i>=3&&i<=7){pulse6=1;}
             else pulse6=0;
             TMR1IF=0;
             TMR1H=0xF0;
             TMR1L=0x00;
             if(x)
             i++;if(i>40)i=0;
             if(i>=5&&i<=15){pulse1=1;}
             else pulse1=0;
             if(i>=25&&i<=35){pulse2=1;}
             else pulse2=0;
      if(i==1||i==3||i==5||i==7||i==9||i==11||i==13||i==15||i==17||i>=20)pulse3=1;
             else pulse3=0;
      if(i=21||i=23||i=25||i=27||i=29||i=31||i=33||i=35||i=37||i<20)puls
e4=1;
             else pulse4=0;
      if(i=2||i=4||i=6||i=8||i=10||i=12||i=14||i=16||i=18||i>=20)pulse5=1;
             else pulse5=0;
      if(i=22||i=24||i=26||i=28||i=30||i=32||i=34||i=36||i=38||i<20)puls
e6=1;
             else pulse6=0;
             TMR1IF=0;
             TMR1H=0xf6;
             TMR1L=0x80;
             }
             }
             }
```

Hardware Prototype

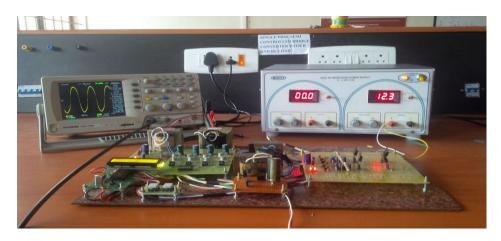


Figure 3: Hardware Prototype For Boost Mode



Figure 4: Hardware Prototype For Buck Mode

Triggering Pulses For Ac/Ac Unit

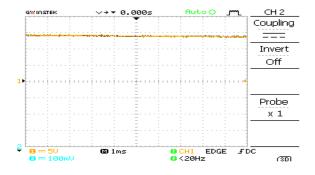


Figure 5: Triggering pulse for Q1

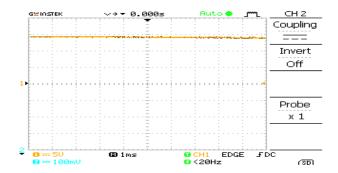


Figure 6: Triggering pulses for Q2

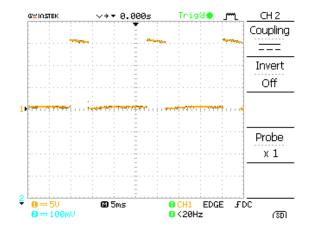


Figure 7: Triggering pulses for Q3

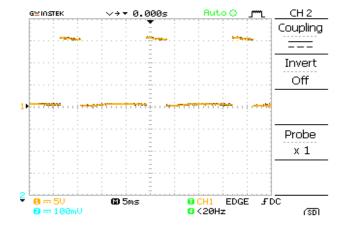


Figure 8: Triggering pulses for Q4

Hardware Results

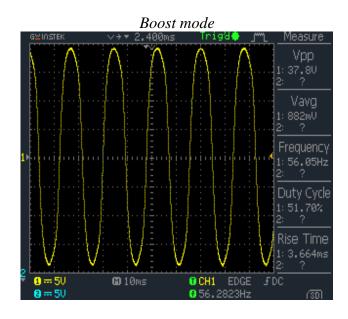


Figure 4: Output voltage

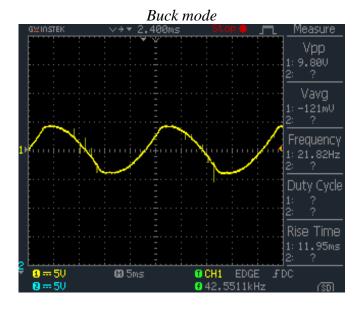


Figure 5: Output voltage

Conclusions

The BBFBI has been proposed in this paper. Block diagram, circuit diagram and hardware prototype have been presented. Active switches are utilized for voltage buck and boost conversion process without additional elements, therefore high efficiency can be achieved.

References

- [1] F. Z. Peng, "Z-source inverter," IEEE Trans. Ind. Appl., vol. 39, no. 2,pp. 504–510, Mar./Apr. 2003.
- [2] Y. Tang, X. Dong and Y. He," IEEE TRANS.IND. APPL, VOL.61,NO.9, SEP 2014.