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Design of Low Leakage Power Wallace Tree Multiplier Using SVL Circuits

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Abstract

In this research work a Wallace tree multiplier is proposed. The Multiplier is the key block and decides the processors efficiency. The objective of this work is analysing different powers in Wallace Tree multiplier, which is implemented using 8Transistor (T), 28T Standard Complementary Metal Oxide Semiconductor (CMOS) full adder and 28T, 8T full adders with Self Controllable Voltage (SVL) circuits. As the transistor sizes are shrinking down to improve integration density and performance, the threshold voltages also being reduced [11]. With the reduction of threshold voltages leakage current is increasing more, especially when the device is in idle mode. The proposed SVL circuits supplies maximum dc voltage to the logic design (load circuit), when the device is in active mode to give normal operation and minimum dc voltage when the device is in standby mode, to reduce leakage power [1]. The proposed SVL circuits minimized power consumption compared to standard CMOS Technique with the minimal area overhead and speed degradation. Wallace tree multiplier realized using 28T full adders with SVL circuits reduced 72.3% leakage power, 8T full adders with SVL circuits minimized 34% leakage power compared to Wallace tree multiplier realized using CMOS 28T, 8T full adders respectively. All simulations done using CADENCE Tool in 180nm CMOS technology.

Keywords— Leakage power; CMOS; SVL circuits; 3T XNOR; 8T full adder;

I. INTRODUCTION

With the prolific growth in the CMOS Technology, Semiconductor industries have been challenged to develop low power dissipation and high performance systems [2].

In Deep Submicron Regions (DSR) with the reduction of threshold and supply voltages, leakage power is increasing drastically [6]. Leakage power is the main energy consumption due to subthreshold leakage when the logic circuit is in standby mode (turned off). It means if a fully charged device is not used for long time it becomes inefficient. This effects the performance of systems, especially portable devices and mobile phones. Therefore low power digital IC design demands various methodologies, which minimizes leakage power [10]. Many methodologies were proposed to minimize leakage power. Mainly two techniques 1. Variable Threshold CMOS 2. Multi Threshold CMOS. In VTCMOS leakage power reduction is done by increasing substrate to bulk voltage. This technique has drawbacks like more area and more power requirement because of additional substrate to bulk circuitry. MTCMOS technique uses both low and high threshold voltages on the same circuit and reduces the leakage power by disconnecting the load circuit from power supply rails [7]. The main disadvantage of this methodology is retaining the data from storage elements is not possible. One more it needs extra fabrication to incorporate two threshold voltages on the same circuit. So inorder to overcome the above drawbacks SVL circuits proposed. SVL circuit minimizes leakage power dissipation and maintains the performance as well.

The outline of the paper is as mentioned below : section II explains the implementation of SVL circuits, section III describes the implementation of Wallace tree multiplier design with and without SVL circuits, The simulation results of two designs is presented in section IV, conclusion of this paper is given in section V.

II. IMPLEMENTION OF SVL CIRCUITS

A. SVL circuit operation:

When the logic design is in switching activity i.e. active, SVL circuit delivers maximum supply voltage (Vdd) and minimum GND voltage (0v) to the logic design. When there is no switching activity in the logic design i.e. inactive, SVL circuit gives relatively less supply (<Vdd) and slightly higher ground voltage level (>0v) to the logic design.

B. Circuit Architecture:

Three different types of SVL circuits are given in Fig 1. Fig.1 shows (a) Upper SVL circuit, (b) Lower SVL circuit, (c) Combination of both USVL & LSVL.

The Type 1 circuitry consists of one PMOSFET switch and a series of nNMOSFET switches (n=1,2...M) connected in parallel. When device is ON, ONPMOS switch connects supply voltage to the load circuit, when device is OFF, Weakly ON NMOS switches gives connection between supply voltage and load circuit. Note that except the first NMOSFET switch which is connected to Vdd, connect gate and drain terminals of remaining series NMOS switches.

Type 2 circuit consists of one NMOSFET switch and a series of nPMOSFET switches connected in parallel. During active mode ON NMOS switch connects load circuit and ground voltage. During standby mode series connected weakly ON PMOS switches gives the ground voltage to the standby load circuit. Connect drain and gate

terminals of all PMOS switches connected in series except the PMOS switch which connected to ground.

Type 3 circuit includes both Type 1 and Type 2 circuits.

Fig.1 (a) USVL (Type 1) Circuit Fig.1 (b) LSVL (Type 2) Circuit. Fig.1(c) Combined (Type 3) Circuit

C. Impact of SVL Circuit on leakage current:

How the SVL circuit minimizes leakage current in the load circuit is described below. Let us assume Inverter as load circuit for easy analysis.

Case (1) OFF NMOS:

Type 1 circuit:

When Vin of inverter is zero in type1 circuit, PMOS in the inverter goes into linear region and NMOS goes into cut-off region i.e. turn off. When sleep signal is high the PMOSFET (pSW) turned off. NMOSFET (nSW) switch1 weakly turn on.Vdd goes through n weakly on nSWs. Therefore output voltage (Vd) of type1 circuit is given as below

$$Vd = Vdd-Vn \quad (1)$$

Where Vn = Voltage drop of n weakly on nSW's.

The drain to source voltage Vds of "OFF NMOS" in the idle inverter is given by

$$Vds = Vd-Vss = Vd \quad (2)$$

Equation tells that Vds can be changed by increasing n or by varying channel widths of nSW's. Decrement in Vds, with the increment of Vn, increases the barrier height of OFF NMOS. Which means it lowers the Drain induced Barrier Lowering (DIBL) effect, which further leads to increase in the threshold voltage of NMOS. The sub threshold current of NMOS decreases with the result in the increased threshold voltage. That means leakage power in standby inverter minimized.

Type 2 circuit:
In Type 2 SVL circuit sleep bar signal turn OFF the nSW and weakly turn ONs the pSW's. Through these pSW's Vss is supplied to inverter circuit. So source voltage Vs of inverter is expressed as

$$Vs = Vp \tag{3}$$

Where VP= Voltage drop across n weakly on pSWs. Then Vsb (Substrate to bulk voltage) of OFFNMOS in the inverter is as follows

$$Vsub = -Vp \tag{4}$$

Increases and Vds is expressed as

$$Vds = Vdd - Vp \tag{5}$$

As Vsb increases, Vth increases and it also minimizes the DIBL effect. As Vth increases, leakage current decreases.

Type 3 circuit :
In Type 3 circuit as Type 1 and Type 2 circuit both are added, Vds of NMOS is given by

$$Vds = Vdd-Vn-Vp \tag{6}$$

Which further minimizes leakage power by keeping Type 1 circuit on top and Type 2 circuit on bottom of the load circuit. So in this case leakage current further decreases compared to case 1 and case 2. One more as Vd and Vs are connected to the standby load circuit retaining data in storage circuits also possible. Likewise it overcomes the disadvantages of previous techniques.

Case (2): OFF PMOS
Similarly in this case also functionality can be analysed.

III. IMPLEMENTATION OF WALLACE MULTIPLIER

The need for high performance systems, challenging the development of low power modules like multiplier and adder blocks. These are the basic modules in any digital

circuits. Multiplier is the array of adder blocks. So efficiency of multiplier depends on the performance, power, and complexity of adder cells. In this work, first 4-bit by 4-bit Wallace tree multiplier is implemented using 28Tfull adder and 8T full adder. Then SVL circuits are incorporated into that adder modules and Wallace tree multiplier is designed through these SVL adder modules.

A. Implementation of 28T Full adder:

Full adder is implemented using 28 Transistors in Standard CMOS technique with the equal number of NMOS and PMOS transistors [3].

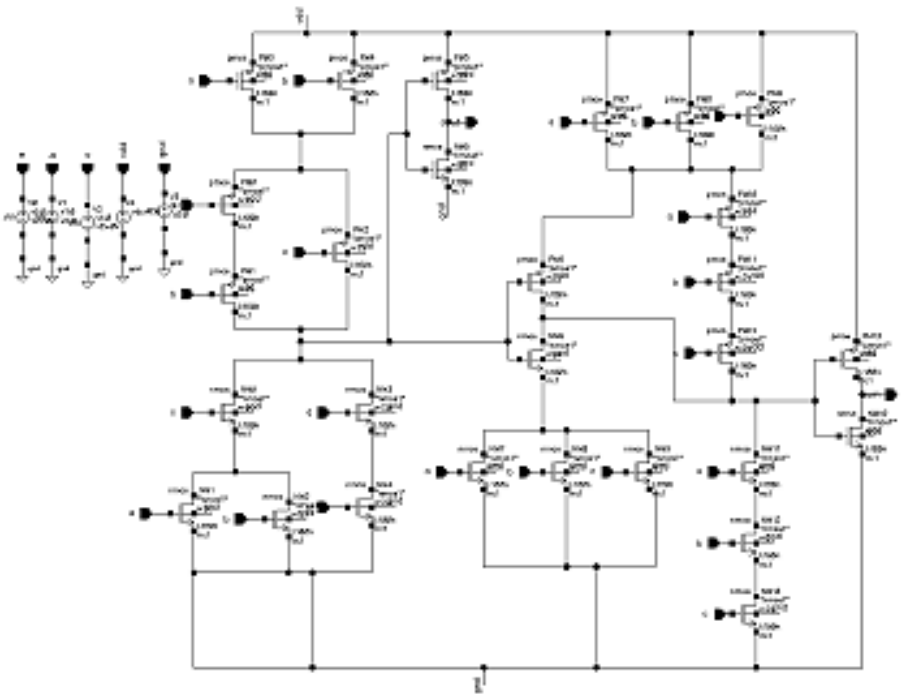

Fig.2 Schematic of Full adder using 28 Transistors

Fig. 2 shows the realization of full adder using 28 transistors. Full adder outputs sum and carry is expressed as

SUM = A xor B xor C (7)

CARRY = (A and B) or (Cin and (A xor B)) (8)

B. Implementation of 8T Full adder:

This full adder uses two XNOR gates and one multiplexer, where as conventional full adder uses 2 XOR, 2 AND,1 OR gate. Design of basic blocks like XOR, XNOR gates with less no of gates increases the performance of the full adder [4]. Here XNOR gate

is realized using 3 transistors (2XNOR = 6T), MUX using 2 transistors [8]. Fig.3 shows the 8 transistor full adder using 2 XNOR and one multiplexer. In this case Full adder outputs are as given below.

SUM= (A xnor B) xnor Cin (9)

CARRY= (A xnor B) and Cin + (A xnor B) and A (10)

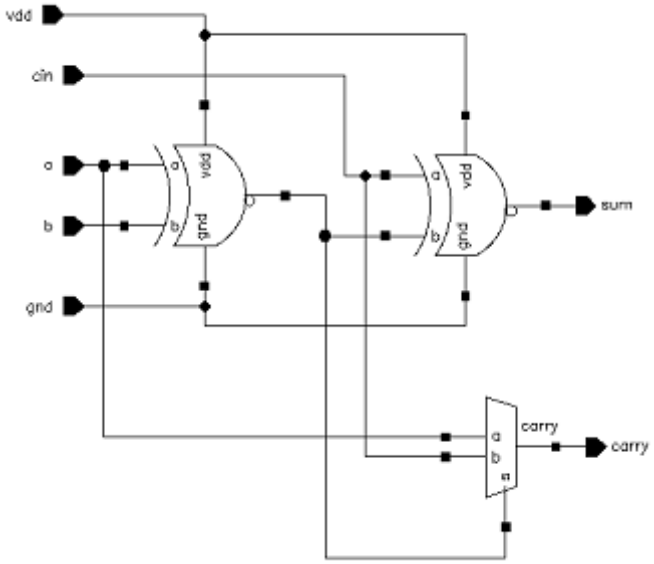

Fig.3 Schematic of Full adder using 8Transistors

C. Implementation of XNOR using 3T:

Fig.4 gives XNOR realization using 3 Transistors [9]. It combines the CMOS and Pass Transistor Logic (PTL).

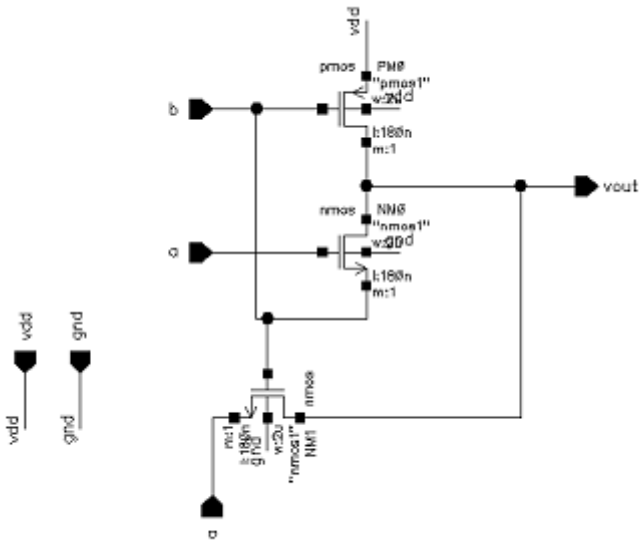

Fig. 4 XNOR implementation using 3T

D. Implementation of full adders using SVL:

Include Upper SVL circuit on the top and Lower SVL circuit on to the bottom of CMOS 28T full adder. Similarly realize 8T full adder with SVL circuit. Fig.5 represents 28 transistor full adder with USVL and LSVL circuits.

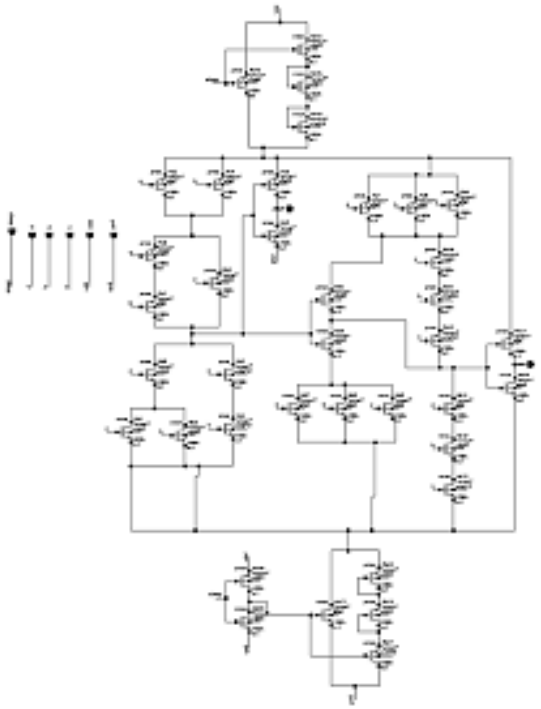

Fig.5 Schematic of 28T full adder with SVL circuits

E. Wallace Tree Multiplier:

Wallace tree multiplier is faster when compared to array multipliers. In this multiplier first calculate partial products. Then rearrange the partial products into a tree like structure to find the depth of the tree. Then realize the tree structure with Full adders and half adders by reducing the depth of tree. The advantage of Wallace tree multiplier is high performance, because the summation of partial products is O (logN), where N represents summands number. The propagation delay of Wallace tree is O $(\log_{3/2}N)$[10] [5]. However in Wallace tree multiplier high performance is obtained with high cost and it has highly complex structure; Due to the irregular structures drawing layout becomes difficult. And this irregular shapes lead to wastage of chip area and power [5]. Fig.6 shows the Wallace tree multiplier with 28T full adder blocks. Similarly realized using 8T full adder and with SVL full adder circuits.

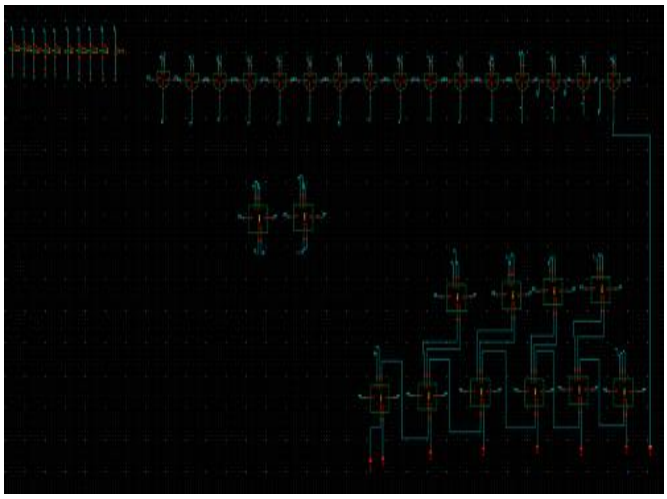

Fig.6 Schematic of Wallace tree multiplier with SVL 8T full adder

Fig.7 shows the Wallace tree multiplier output for 4bit *4bit input pattern.

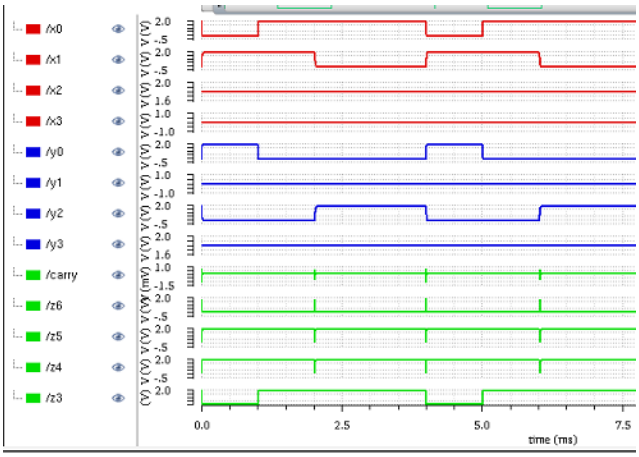

Fig. 7 Output waveform of Wallace tree multiplier

IV. RESULTS AND DISCUSSIONS

In this work, the simulations of Adder modules and multiplier blocks were done in 180nm technology using CADENCE tools.

TABLE I LEAKAGE AND TOTAL POWER OF 28T FULL ADDER

Adder/Power	Leakage Power (pW)	Total Power (nW)
28T Full adder	97.54	534
28T Full adder with SVL	11. 06	393

TABLE II LEAKAGE AND TOTAL POWER OF 8T FULL ADDER

Adder/Power	Leakage Power (pW)	Total Power (nW)
8T Full adder	86. 39	517
8T Full adder with SVL	57. 11	442

TABLE I shows that 28T full adder with SVL circuit reduces 88% leakage power, 26 % total power compared to CMOS 28T Adder

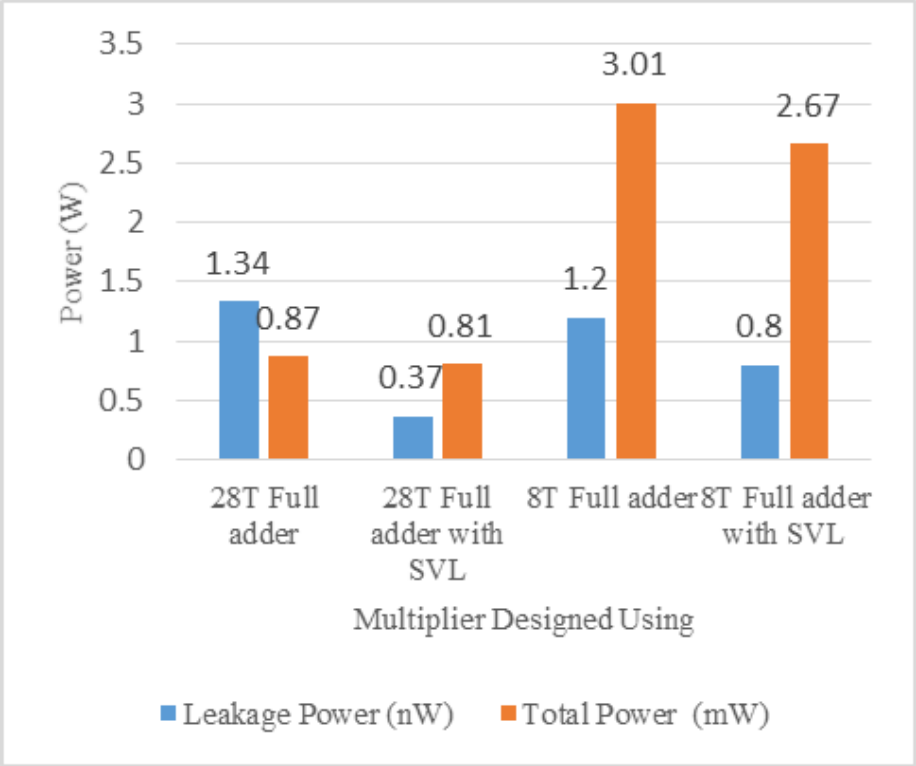

Fig.8 Leakage and Total Power of Wallace Tree Multiplier Using various Adder Blocks

TALE II shows that 8T full adder with SVL circuit reduces 34% leakage power, 14.5% total power compared to 8T Full adder.

Fig.8 shows that Wallace Tree Multiplier using 28T Full adders with SVL circuits minimizes 72.3%leakage power, 7.1% total power compared to Wallace Tree Multiplier with 28T Full adders. Wallace Tree Multiplier using 8T full adder with SVL circuits reduces 34% leakage power compared to Wallace Tree Multiplier using 8T full adders.

V. CONCLUSION

From the obtained simulation results it is concluded that the SVL technique is better in the reduction of leakage power, there by total average power reduction when compared to standard CMOS technique, with minimum area overhead and performance degradation [12]. One more advantage of this technique is data retention from sequential circuits in standby mode. However transistor count is more in this technique, which limits the high performance.

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