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Enhanced Built-In Self Test For MSP 430

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Abstract

The enhanced Built in self test (BIST) is a combined form of both hardware and software together to resolve the memory problem in self testing. So it automatically comprises own test using self test pattern generation. The implementation can be done using the microcontroller MSP 430 series. Here we are using the Xilinx software for compilation in the design implementation. Also its functional can be done using dynamic RAM and reduces the external testing methods also includes diagnosis of test.

Keywords- BIST, ATE, DRAM

Introduction

BIST is a perfect solution for automatic generation of an address and data, performing a write to memory, and afterwards performing read and comparing to the expected content of memory cells. It also used in critical circuits directly we cannot involve memory based functions. Better fault coverage can be done. The evolution of BIST is shown in figure 1.

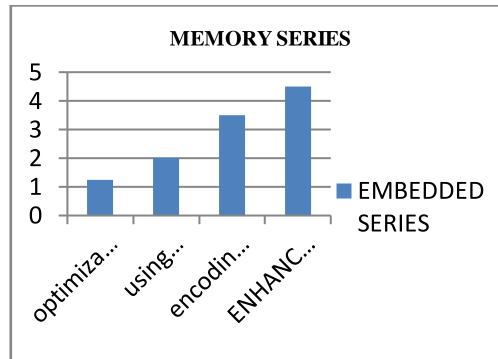

Figure 1: evolution of built-in self test

So the special test structures will be produced in the chips. In shorter test times BIST structure can be designed. Capability to produce some testing environment tests in the electrical testing zone. The last merit ensures actually allow the user to produce some more change in functional structure towards the short design implementation. It utilities algorithm such as March c, March c+.the enhanced BIST will be implemented in a internal microcontroller as specified Msp 430 series.

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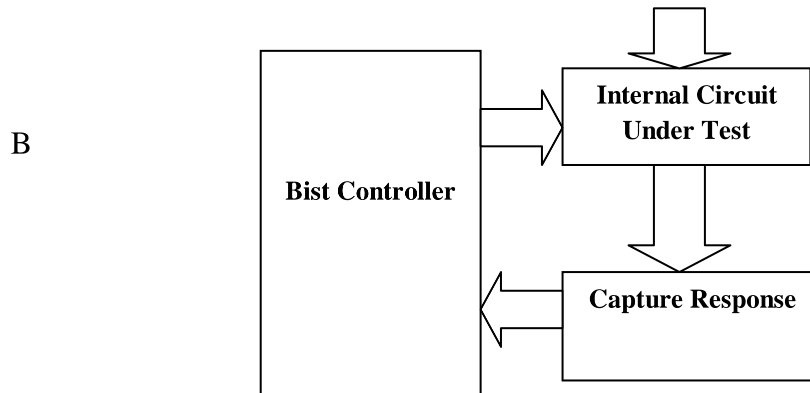

Figure 2: Basic Diagram Of BIST

Proposed System

The proposed work contains of enhanced built in self test architecture which automatically generates test pattern and increases speed thereby reduces cost. Here the input test pattern will be generated by its own as in enable value based on the clock pulse functional. The signature gathers the circuit under test to the test pattern as signature. The tests a controller coordinates the actions of the test circuitry and provides a simple external interface.here the test output will be produced towards the pattern generator and introduce a circuit under test hence produce output. Here the enhanced built in self test mentions the automated test pattern generation using the

LFSR (linear feedback shift register) produces a automated test generation in 64 bit memory processing in an instant. Now it can be designed to merge the LFSR coding in Xilinx workbench to produce a schematic to generate a automated test pattern generated. Now mingle the concept of microcode built in self test in main course Msp series.

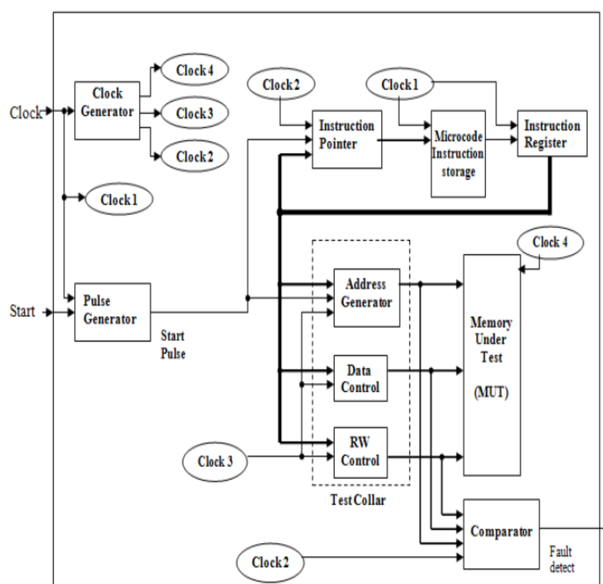

Figure 3: proposed block diagram of Enhanced BIST

Methodology

In this enhanced BIST the 64 bits LFSR pattern will be produced and then the value can be denoted. In LFSR pattern generator the test pattern will be produced and the variation of the systematic test pattern generator will be designed. Now the memory value and criteria value can be done towards the system.

Now the microcode BIST architecture will be designed in the functional variations are noted.

Memory Bist

Memory BIST is a functional classification which allows the March blc algorithm that enables in towards a checking and correction of a algorithm. This MBIST acquires a predefined values to assign the functional system to produce a value regarding. This allocates a special memory test procedure to enable a speed memory processing. Conventional block diagram is shown in figure 4.

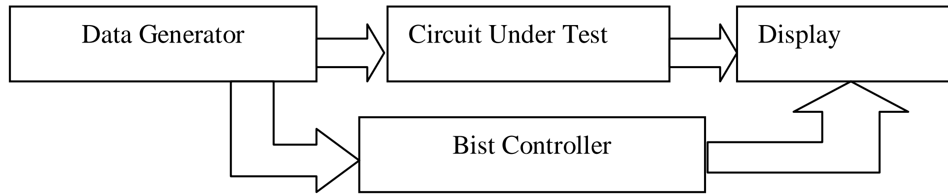

Figure 4: conventional block diagram for memory BIST

March BLC Algorithm

This algorithm supports a multiple values to be checked with in a given source of time thereby produce a functional binary logic code that generated as enable, clock values, input and output values. This enables a cyclic redundancy coded values the supports a binary error code checking. Clears the faults address and create a redundancy to cyclic checking.

Real Time Significants

1. Produces Lower cost of test and avoids external testing equipments
2. Better fault coverage so enables a new structure in the memory unit of microcontroller.
3. Consumes low power so external testing will also be produced internally.
4. Consumers can easily access this system .
5. It can support both internal and external enable structure for testing.

LFSR Pattern Generator

The enhanced BIST produce a variable that can enable a connection design. The output contains a connection in the enable unit that can produce a change in clock values and enable bit values. By changing the binary values towards the system this can be producing the systematic pattern generated in a output. This function LFSR output waveform is shown in below output unit.

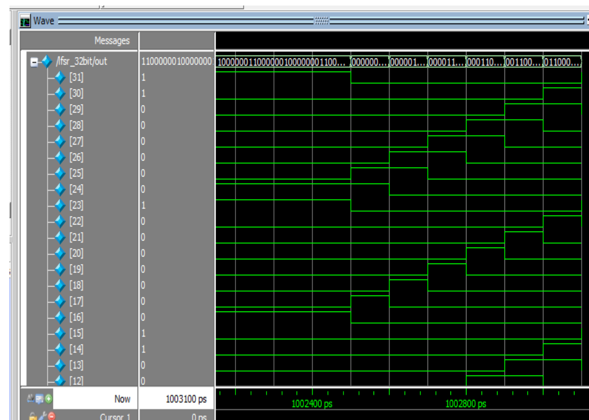

Figure 5: LFSR pattern generation output

Comparison Table:

S.No	Methodology	Critical Issues	Solution
1.	Optimization of Microcode Built-In Self Test By Enhanced faults Coverage for Embedded Memory	Poor performance by external feedback, redesign is required to change the test controller.	Using march BLC algorithm for microcode BIST architecture.
2.	New OBIST Using On-Chip Compensation of Process Variations Toward Increasing Fault Delectability in Analog ICs	A new on-chip oscillation test strategy produces the time consumption, power consumption.	On chip Schmitt trigger is used as the on-chip frequency

Simulation Parameters

The parameters to be considered are enable, reset, input, clock, reset, linear feedback. These parameters are functionally produced in the process towards the built in self test memory so it can be fascinated in the memory.

The modified enhanced built in self test can be probably in the functional systematic memory allocation procedure.

This will consider the power consumption, speed of the processor. Here this consider the functionality endures the memory blocks in the command lines towards the various line of memory values.

Now its is considered to have the systematic linear feedback towards the input selection lines in the main value. then the output can be done through the various analogy of the memory line as shown in figure 6

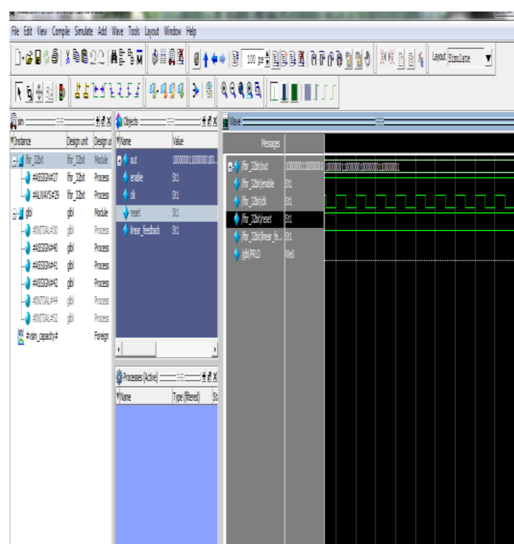

Figure 6: Simulation Output

The same output value can change the various values in the considerable memory location. This enables the changing values in the clock value and then can be producing a variation in the functional procedure BIST consider the input value and produce a variation in the LFSR pattern value.

The input value will be changed based on the microcode BIST architecture. Producing new architecture for changing test pattern

The generated value adds sum of the functional variation towards the value in consideration on the value in bits produced so that can reduces the main value system.

This can be promptly the variation in binary coordination in the binary value LFSR random model architecture through the main units.

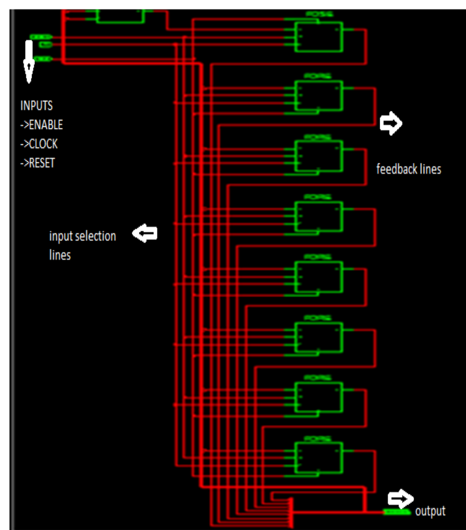

Figure 7.schematic diagram for BIST

Anaysis For Memory Bist

In the analysis stage the short signal will be send towards the memory which will increase the maximum speed of the BIST controller. This simulation is done in the XILINX platform. This will produce the change in the memory perception in the device. The input produces a change in the bit value and enhances the professional systems value by 0 and 1 value in 32 bits random manner, this can be probable produced in memory enhancement in the device as shown in figure 8.

Here we are producing the pattern generator for the LFSR and producing new microcode BIST architecture in order to produce a main functional BIST controller. Combining the two processes together we are designing the enhanced Built in self test for msp 430.

Now the enhanced BIST produces a considerable change in the variation over a main system.

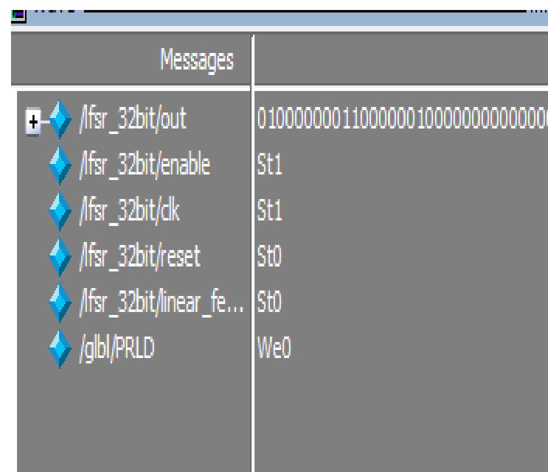

Figure 8: Analysis Parameter For Memory BIST

Conclusion

Here the BIST controller provides a wide testing procedure that enables a main functional access to the systemic checking in the memory allocation procedure It is a system performs a dynamic internal and external testing equipments that allows a variable testing in a considerable units. This system avoids the external test improves an incorporation of hardware and software systems. Error rates will be minimum so this advances a connection towards the systematic unit binary code enabling

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