International Journal of Applied Engineering Research
ISSN 0973-4562 Volume 10, Number 7 (2015) pp. 17743-17749

http://www.ripublication.com

Design of PLL And Frequency Synthesizer With SRL CMOS Using GDI Technique

[1]Venkata Subba Reddy Takkoli
Master Student, Department of ECE
SRM University, Chennai, India
subbareddytakkoli@gmail.com
[2]Mr. A V M Manikandan
Assistant Professor (Sr G), Department of ECE
SRM University, Chennai, India
manikandan.m@ktr.srmuniv.ac.in

Abstract

In this paper, Phase Locked Loop (PLL) and frequency synthesizer is designed with Self Resetting Logic Complementary Metal Oxide Semi Conductor (SRLCMOS) using GDI technique. The design enables the implementation of different logic functions with less number of gates, low leakage current and low leakage power when compared with CMOS and other existing techniques. In the proposed design, the pull down tree is implemented with Gate Diffusion Input (GDI) with level restoration which apparently eliminates the conductance overlap between nmos and pmos devices, thereby reducing the short circuit power dissipation and providing High Output Voltage V_{OH}. Simulations are done using 180nm technology.

Keywords: Phase Locked Loop, SRLCMOS, Gate Diffusion Input, CMOS.

Introduction

With continual technology scaling, the integrated system has become faster, and thus it is employed in diverse real-time applications like mobile, digital signal processing, multimedia application and scientific computation. To support high performance applications, proper choice of technology selection and topology for implementing various logic are mandatory issues in designing low-power devices. In portable battery operated devices, power consumption is critical since it determines the lifetime of the battery. It also affects the device size, cost and weight.

Static CMOS has been the design style of choice for IC designers due to its robustness against voltage scaling and transistor sizing (high noise margins). The operation are reliable at low voltages, but the problem in using this logic for

implementing logical functions it requires large number of transistors to implement a logical function. With increase in the number of transistors, the area on the chip gets increased and power dissipation also gets increased. Sub threshold leakage current is the main source of power dissipation in CMOS circuits[1], and it should be reduced to minimize the power dissipation. Circuits that contain large number of multiplexers, XOR gates are implemented using Pass Transistor Logic as PTL[2] implementations of these functions are more efficient than conventional CMOS implementations. Implementations of logic gates such as NANDs and NORs with PTL found to be slower and consume more power than CMOS implementations mainly because of the reduced output swings due to the threshold drop across a single-channel pass transistor. Leakage through PTL found to be greater than that of CMOS implementations.

To reduce the transistor count in a circuit, the logical functions are implemented using dynamic logic. But, the main problem with this is even if the transistors in the Pull Down Network(PDN) is turned off, they may be momentarily on due to the accumulation of noise at the inputs of the transistors causing the dynamic node to get discharged, thereby changing the output. To overcome this problem, a self resetting logic is proposed. A keeper transistor is used that get switched on whenever there is a discharge in the dynamic node due to noise at the inputs of PDN. This keeper transistor charges the dynamic node, thereby keeping the output same as it is used to be before the accumulation of noise at the inputs. However the drawback of this scheme is that it takes large number of nMOS transistors to implement a given logic function.

GDI [3] technique is used for reducing power and area in VLSI design circuits The GDI approach was originally proposed for fabrication in Silicon-on-Insulator (SOI) and twin-well CMOS processes. In this, complex logic functions are implemented using only two transistors. By using this method we can design standard digital circuits, with a much smaller area than Static CMOS and existing PTL techniques[4], while providing improved power characteristics. Similar to PTL implementations, the GDI circuits suffered from a reduced swing due to threshold drops. However, a significantly reduced transistor count and the logic flexibility of the basic GDI cell provided significant power reduction, despite the need for swing restoration circuits.

In this paper, logic circuits are implemented with SRLCMOS [5] using GDI technique. In which in PDN is replaced with GDI technique. Self-resetting circuitry automatically pre charge themselves after a prescribed delay by conditionally charging the dynamic nodes to evaluate the desired logic function using a local feedback timing chain instead of a global clock. Although this SRLCMOS logic inherits lot of merits, it still suffers from static power dissipation due to the nMOS logic structure. As stated earlier, during pre charge the nMOS stack is completely open and the output is fed back to the pMOS block to charge the capacitor Cy. During this period, the nMOS transistors operates in cut-off region exhibiting sub-threshold current.

Moreover, during evaluation phase when the entire nMOS transistor in the n-block and Preset transistor is ON direct impedance path exist between the vdd of Preset transistor and nMOS block leading to static power dissipation. The width of the pulses

must be controlled carefully, else there may be contention between nMOS and pMOS devices, or even worst, oscillations may occur. These demerits can be surmounted using GDI technique. The change done in the existing SRCMOS[6], instead of nMOS logic pull down tree, it is replaced as GDI logic with level restoration.

The paper is organized as follows: Section II shows the scheme of the proposed SRLGDI technique. Section III discusses about benefits of SRLGDI technique.

SRLCMOS With GDI Technique

The general structure of Self Resetting Logic with Gate Diffusion Input technique (SRLGDI) is shown in Fig 1. The structure consists of GDI block to realize any boolean function The transistor Ppreset and Preset are used to charge and discharge the dynamic node capacitor Cy during pre charge and evaluation phase. The noteworthy aspect of Preset transistor is that it acts as charge keeper to resolve the charge sharing problem which is the significant issue in dynamic circuit. The Preset transistor will pull the voltage level high even after the pre charge phase to hold the output value high in the existence of charge sharing. The output is fed back to the pre charge control input and, after a specified time delay, the pull-up is reactivated.

The inverter INV1 and the internal inverter in the GDI block completely eliminate the contention problem and provide compatibility to cascade the output from one node to another node. The output of the gate provides a pulse if the logic function becomes true. This output is buffered and it is connected to pMOS structure to pre charge. The delay line is implemented as a series of inverters. The signals that propagate through these circuits are pulses. The inverter (INV2) present at the output side provide both true and complementary output and also it acts as level restoration circuit to cascade more number of circuits without logical degradation. By using a buffered form of input, the loading (input) is kept almost low when compared to normal dynamic logic while local generation of the reset assures that it is properly timed and occurs only when required. This modification produces less power consumption and high V_{OH}, while apparently maintaining the logical functionality.

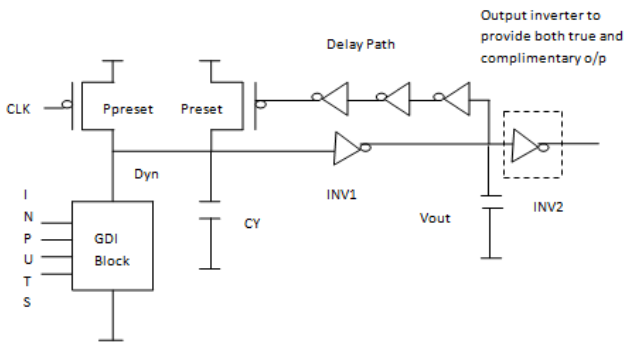

Figure 1: General Circuit Topology of Self Resetting Gate Diffusion Input

The nMOS pull down network in the conventional scheme is replaced with gate diffusion input block with level restoration and output inverter offers true and complementary output.

PLL and Frequency Synthesizer With SRLCMOS Using GDI Technique

To implement Phase/frequency detector, two D-Flipflops are used. The outputs of flipflops are given as inputs to NAND gate and output of NAND gate is given as reset signal to flipflops. D-flipflops and NAND gate in the Phase frequency detector are implemented with SRLCMOS using GDI technique.

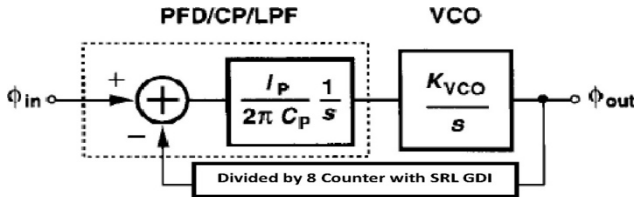

Figure 2: Block Diagram of Frequency Synthesizer [8]

As shown in the figure 2, in feedback path of PLL a divide by 8 counter is implemented with SRLCMOS using GDI technique. Frequency synthesizer [8] is implemented with SRLCMOS using GDI technique.

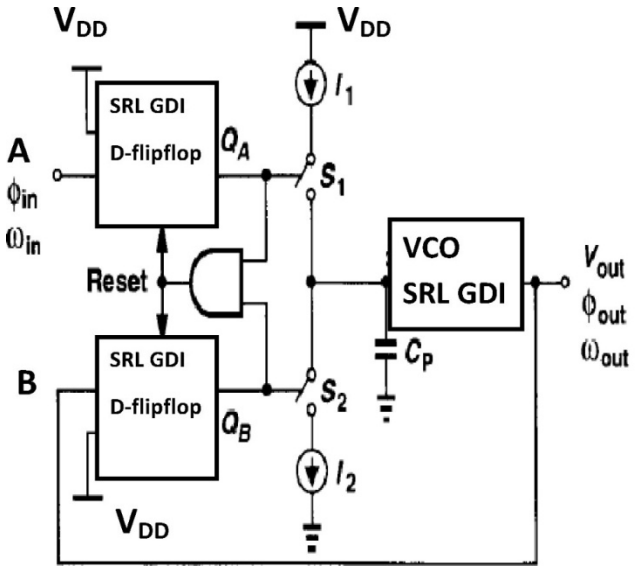

Figure 3: Block Diagram of Charge Pump PLL [7]

In the above circuit, charge pump PLL[7] and current starved voltage controlled oscillator are used. Both are implemented with SRLCMOS using GDI technique.

Simulation Results

Simulations were done using the SPECTRE based Cadence Virtuoso simulator with a standard power supply of 1.8V.

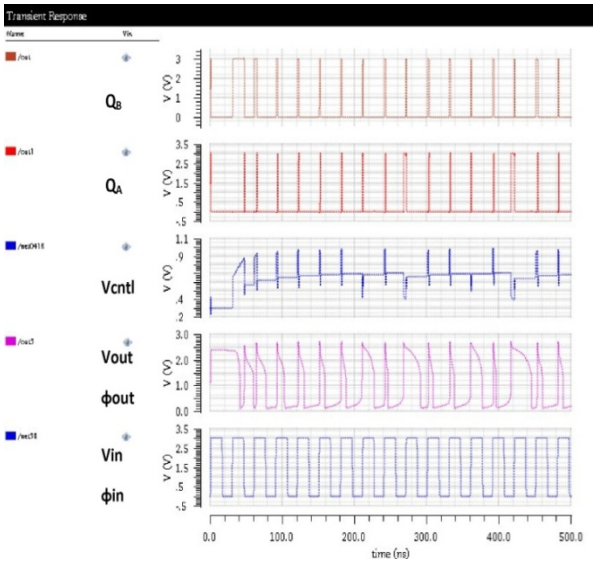

Figure 4: Output waveform of Charge Pump PLL with SRLCMOS using GDI technique

From the above figure, we can say that when both input and output are Phase/frequency locked, we get a constant Vcntl signal. To implement this PLL, Capacitor (C_P) value kept around 1000pF and Resistor value is chosen as 200 ohm.

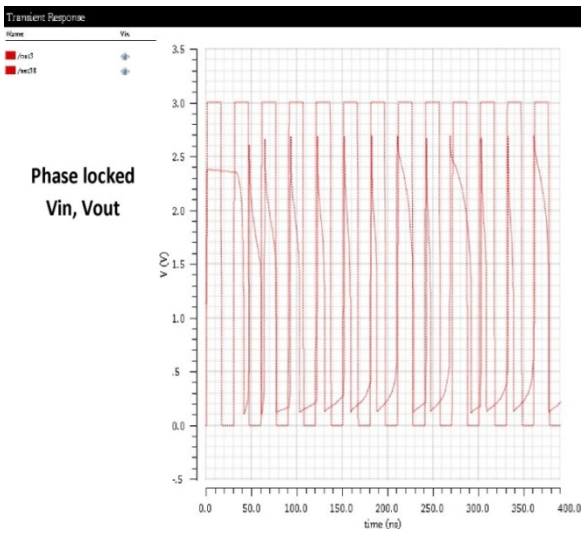

Figure 5: Output waveform showing Phase Locking of Input and Output by using SRLCMOS with GDI technique

A frequency synthesizer is developed with divide-by-8 Counter in its feedback path by SRLCMOS using GDI technique.

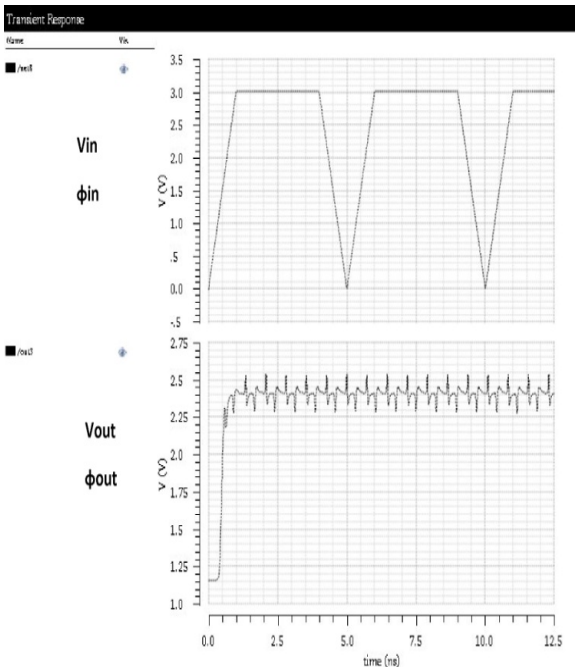

Figure 6: Output waveform of Frequency synthesizer by using SRLCMOS with GDI technique

Conclusion

In this work, an alternative methodology is proposed for the design of Phase Locked Loop and Frequency synthesizer with SRLCMOS using GDI technique. The components used to design are Phase detector, Charge Pump PLL, Low Pass filter, Divide-by-8 Counter, Current Starved Voltage Control Oscillator. The proposed circuit does not require global clock. Therefore, the SRLGDI structure will not suffer from clock distribution problem. The loading effect and the monotonicity requirement have been surrogated by the SRLGDI logic.

To fulfill the reqirement of monotonicity, charge sharing and cascading effects, multiple inverters, delay path inverters and level restoration circuit has been incorporated which slightly increases the total gate count of the circuit which is the only drawback of this logic.

References

[1] Balsara and Steiss., 1996P.T. Balsara, D. Steiss Performance of CMOS differential circuits IEEE J. Solid-State Circuits, 31 (1996), pp. 841–846

[2] Chatzigeorgiou and Nikolaidis, 2001A. Chatzigeorgiou, S. Nikolaidis Modelling the operation of pass transistor and CPL gatesInt. J. Electron., 88 (2001), pp. 977–1000

[3] Morgenshtein et al., 2002A. Morgenshtein, A. Fish, I.A. Wagner Gate-diffusion input (GDI): a power-efficient method for digital combinatorial circuits IEEE Trans. VLSI, 10:566-581.

[4] R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE J. Solid-State Circuits, vol. 32, pp. 1079–1090, June 1997.

[5] New low power adders in Self Resetting Logic with Gate Diffusion Input Technique R. Uma, Jebashini Ponnian, P. Dhavachelvan

[6] Kim, 2001Kim, W.J., Kim, Y.B., 2001. A localized self-resetting gate design methodology for low power. In: Proceedings of the 44th IEEE 2001 Midwest Symposium on Circuits and Systems, August 14–17, 2001, Dayton, OH, pp: 305–308.

[7] F. M. Gardner," Charge-Pump Phase-Locked Loops," IEEE Trans. Comm., vol, COM-28,pp.1849-1858,Nov. 1980

[8] W. F. Egan, Frequency Synthesis by Phase Lock, New york: Wiley & Sons, 1981.

[9] J. A. Crawford, Frequency Synthesizer Design Handbook, New York: Artech House, 1994.