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Design and Analysis of Multiple Test Patterns In Bist Scheme

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Abstract

This paper discuss about a new pattern generator for BIST technique. Multiple single input change vectors (MSIC) are generatedin which each vector given to the each scan chain is the single input change vector. Here two types of SIC generators are used to produce minimum vector transitions.That SIC counters are namely reconfigurable Johnson counter and SIC counter. These SIC counters are applicable for test per clock as well as the scan operations. In these methods the clock cycles are reduced which in turn increases the throughput. TheNon-linear feedback shift register (NLFSR) in Galois field configuration is used as a seed generator in the proposed method to increase the randomness of the test pattern.This method save the power consumption and also usesless area.

Keywords: Galois field, Single input change (SIC), multiple single input change vectors (MSIC), Non Linear Feedback Shift Register (NLFSR).

Introduction

In VLSI testing, the complexity can be reduced by using Automatic Test Equipment by initiating on-chip hardware testing in the circuit.Built- In Self -Test acts as the automatic test equipment.BIST is used for its speed in testing and it reduces the use of the exterior ATE.In generally BISTarchitectures,for test pattern generators and output response analysers uses linear feedback shift register (LFSR) to generate the long pseudo random patterns for scan chain inputs to achieve higher fault coverage which leads to high switching activities .Pseudo random patterns obtained from the LFSR lowers the correlation among the test sequences. It may cause the damage to the product and its yield.The maximum transition density are higher which causes high transition between the vectors and consumes high power.

Related Work

Many advanced BIST architectures have been studied and analysed. Many approaches involved in changing the functionality or the selection of the LFSR. In the first class, the seed selection in CUT's switching activity and the impact of LFSR polynomials were analysed and proposed a concept of energy reduction by seed selection [1]. The second class involves low power TPGs.A BIST technique namely dual-speed LFSR is used in the circuitsto reduce switching activities. Considering two different speed LFSRs, for half of the test patterns are applied using slow-speed LFSR that elevates transition densities [2]. Low power pattern generator is used in lowering the test power in asynchronous circuits based on the cellular automata rules [3].The method which lowers the power in test circuitis based on modifying LFSR[4]. Another approach reduces power and lower signal activities in scan chain using a technique based on low power random pattern generation [5]. On increasing correlation between successive patterns power is reduced in [6]. Same value is assigned to the most of the adjacent bits in the scan chain which reduces scan input transitions [7].

This paper proposes Multiple Single Input Change vectors usedfor the BIST circuits.The proposed design achieves the targeted fault coverage and test efficiency. Thus the proposed technique is adaptable to both tests per clock and also forscan methods.

Proposed Work:

A. Test Pattern Generation

The TPG consists of Johnson counter or SIC counter,Seed generator, XOR gates, Clock and Control circuits. There is m Primary Inputs(PI) for a full scan plan having M scan chain number with l scan cells. The m-bit NLFSR generate the vectors as s= s0 s1 s2…… sm-1 called as seed. The vectors produced by l-bit Johnson counter are expressed as j= j0 (t) j1 (t) j2 (t)…..jl-1(t). Vectors in the I clock period are defined asj = j0 j1 j2,. . j(l−1) which will bit-XOR with the seed vectorss = s0s1s2, . . . , s(m−1), and the outputobtained as xlx(l+1)x(2l+1), . . . , x(m−1)l+1 which are shifted into number of chains that is shown in figure1. During II clock period, j = j0j1 j2. . . jl−1 are shifted circularly as j = jl−1 j0 j1, . . . , jl−2 is obtained which will bit-XOR with the seed generateds= s0s1s2, . , sm−1, andthe output obtained asx2,x(l+2),x(2l+2), . . . x (m−1)l+2 which are shifted for number of chains. They are fully loaded after l clock cycles with the Johnson code words and on m primary inputs the seed are applied. So l identical Johnson code words are generated by circular Johnson counter through shifting a Johnson vector circular operation.

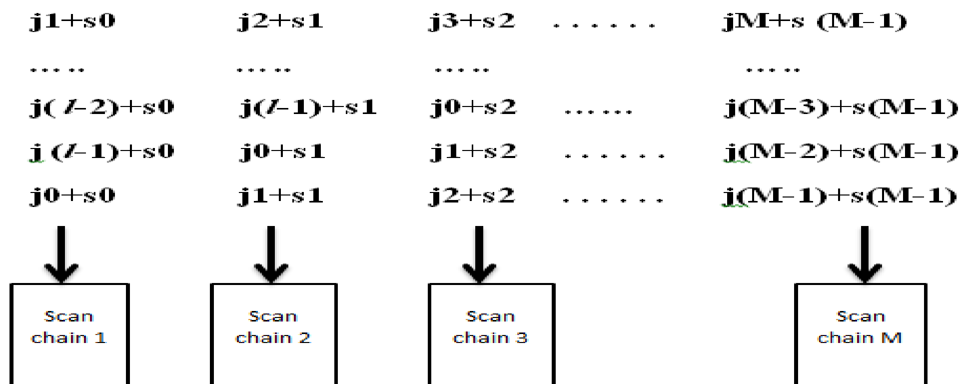

Figure 1: Msic Pattern Generation – Symbolic Representation

B. Reconfigurable Johnson Counter

Two SIC counters are designed dependingupon the scan length, i.e., scalable SIC counter andreconfigurable Johnson counter. SIC sequence is generated by using reconfigurable Johnson counter as shown in figure 2for small scan length .Three modes of operation:

a) Mode1: Initialising the counter's all states to be 0, if clockingis done more than*l*times while RJ mode is 1 and Init mode is 0.
b) Mode2:Johnson code word is generated by Johnson counter at each stage when RJ mode, the Init is 1and when clocking is done by *l* times.
c) Mode3: When RJ mode is 0then Johnson Counter will produce 2*l* distinct vectors when clocking is done about2*l* times and newly generated Johnson vector is applied to XOR gate.

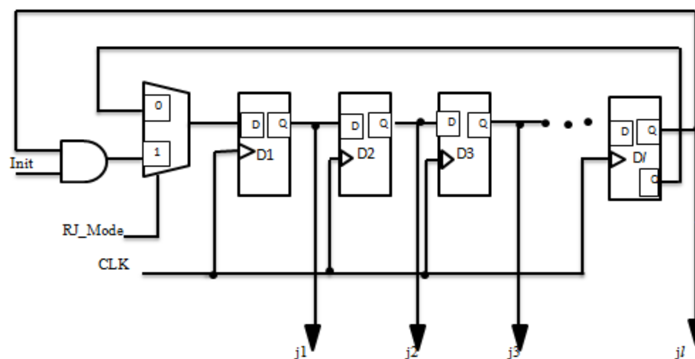

Figure 2: Reconfigurable Johnson Counter

C. Siccounter

For larger length of scan when compared to the scan chain number, we go for the scalable SIC counter as shown in figure 3. It has q-bit adder,q-bit subtractor,k multiplexers,shift registers and combinational gates.q-bit subtractor and M_shift

register is clocked by clk signal. The value assigned for q is int of log2 (*l*-M). The falling SE signals enable the q-bit adder to generate the number of 1s or 0s towards the shift register to be filled. The three operation modes are shown below:

a) If SE signals falls to 0, subtractor stores the adder count. If SE signal rises to 1, the q-bit subtractor content reduces to all zeros gradually.
b) When SE signal rises to1, the subtractor contents are decreased, but not to all zeros.
c) The needed 1s and 0s are shifted to the register by*l* times clockingand the distinctgenerated codewords are given to the scan chains.

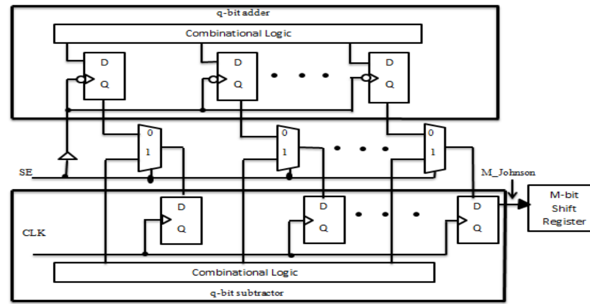

Figure 3: Scalable Sic Counter

D. Non -Linear FSR:

Non- linear fsr is a concept of the linear fsr in which the non- linearity of the last state is the current state. Non- linear fsr hasbeen proposed instead oflinear FSR for producing pseudorandom patterns .NLFSR functionality are generally in both Fibonacci and in Galois hardware configuration .The main drawback of LFSR is its linearity which is ease for cryptanalysis. In the Fibonacci configuration NLFSR, result of the update function obtained from the feedback of the last bit. In Galois configuration NLFSR(figure 4) makes parallel computation of each next state function which increases the speed of the output sequences.That sequences have good statistical properties. This wouldn't be produced by the Fibonacci NLFSRs. The time of the larger feedback function of the Fibonacci NLFSR is quiet high when compared to the propagation time of smaller function of single bits in GF configuration.

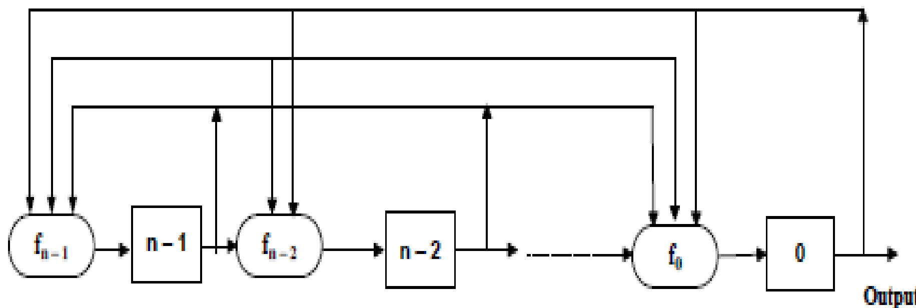

Figure 4: NLFSR In Galois Configuration

E. TPG For Test Per Clock (TPC):
The outputs of the NLFSR and the SIC counter are fed as input to the XOR gate. The input to the M scan chains areobtained from the outputs of parallel XOR tree. The test procedure for multiplepattern generations using test per clock schemes(figure 5) are:

1. Using the enable seed the CLK signal clocked and the new seed is generated by seed generator.
2. In Johnson counter mode the Johnson vector is generated by clocking one time and the RJ_Mode is reset.
3. New vector has been obtained while RJ_Mode is one and also Init isone. Then counter functions as a circular shifting register, produces distinct codewords in*l* times.
4. After generating 2l Johnson vectors, the XOR operation is performed between the outputs of the NLFSR and Johnson codeword in the output generator.
5. Outputs from the output generator are applied to M scan chain inputs and achieve the minimum transition.

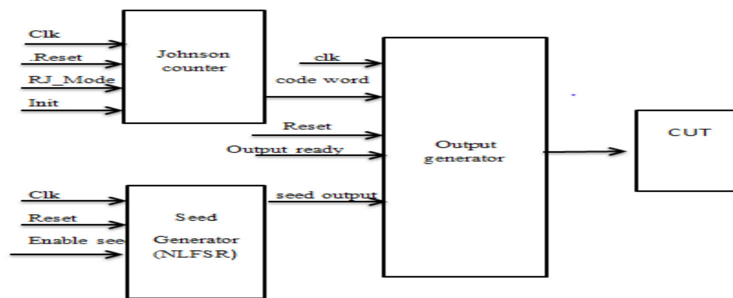

Figure 5: Structure For TPC Method

F. TPG For Test Per Scan (TPD):
The output from NLFSR andJohnson counter are fed as inputs to the XOR. The input to the M scan chains are obtained from the outputs of parallel XOR tree. The test procedure for multiple pattern generations using test per scan method(figure 6) is same as clock technique in addition capture method is present here.

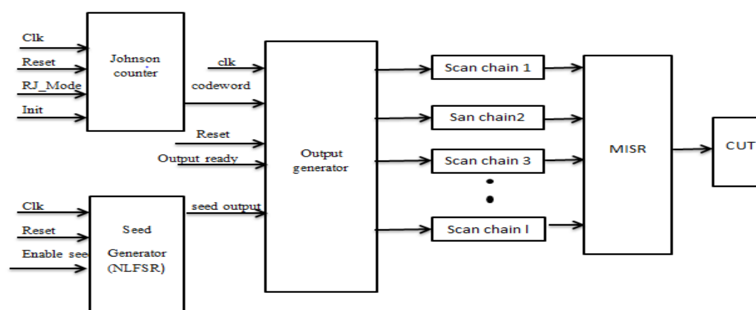

Figure 6: Structure For TPS Method

Results and Discussion

The proposed TPG based BIST are programmed on VHDL language and it can be implemented on the FPGA Spartan3E. The proposed TPG is simulated using Modelsim altera10.1b and the synthesis results are obtained using Xilinx12.4 is shown in table 1. And the verified model is given into the ISCAS 89 benchmark circuits. The simulation for s1512 and s5378 has been done for the proposed method.

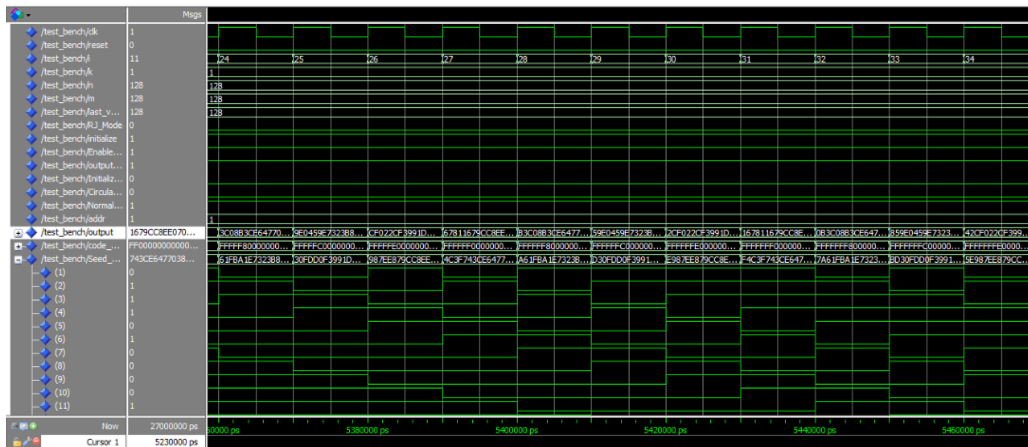

Figure 7: Simulation Result of The Test Per Clock (TPC)

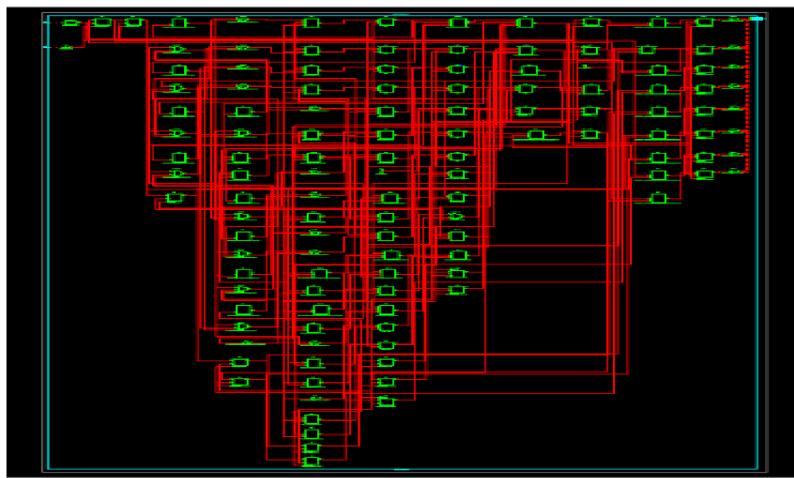

Figure 8: RTL Schematic of Test Per Clock

Figure 9: Simulation of The Test Per Scan (TPS)

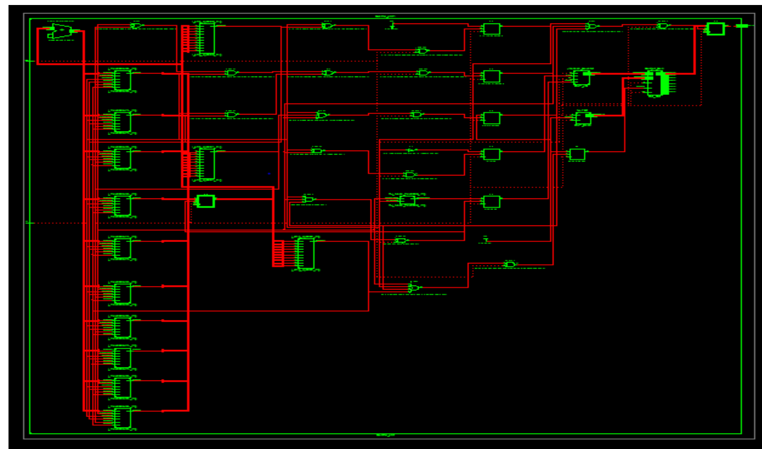

Figure 10: RTL Schematic of Test Per Scan

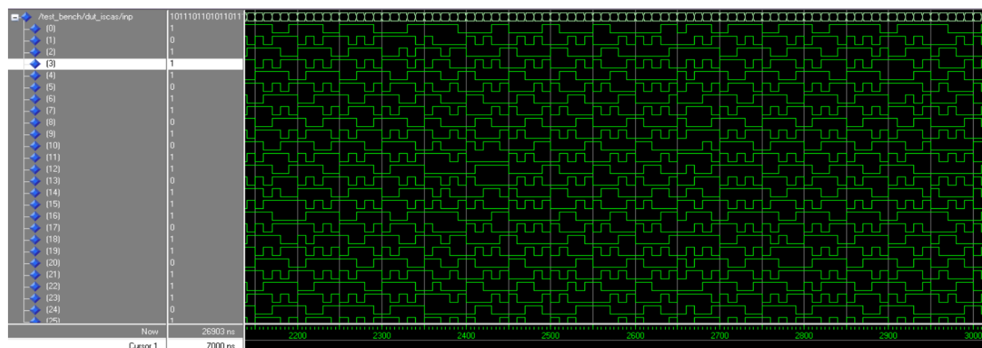

Figure 11: Waveform For S1512

Figure 12: Waveform For S5378

Table 1: Results Showing Power Reduction and Area Overhead

PARAMETERS	TEST PER CLOCK	TEST PER SCAN
NUMBER OF SLICES	41	82
CLOCK PERIOD	4.524ns	365.641ns
FREQUENCY(MHZ)	221.021MHz	2.735MHz
DYNAMIC POWER IN W	0.002	0.006

Conclusion

In this paper, a multiple pattern generation using twomethods that could easily be done in hardwareimplementation. The multiple test pattern generation is done by using the Johnson counter output xoredwith the NLFSR in GF configuration. The outputsequence generated is used to determine the power and the clock frequency. And also the area has been determined for the circuit. Thus the multiple pattern generation is done using both test per clock as well as scan methods. The proposed method is verified by using the ISCAS89 circuit in simulation and synthesis.

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