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An Efficient PFC Zeta Converter-Based PMBLDCM Drive for Air-Conditioners

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Abstract

It is extremely vital to provide some attention on the quality of the currents absorbed from the utility line by electronic goods is increasing owing to a number of reasons. A perfect Power Factor Corrector (PFC) should follow a resistor on the supply side at the same time keeping a fairly regulated output voltage. Bridge and bridgeless rectifiers have been utilized in most of the PFC converters. The power and the switching losses of the amount of semiconductors may possibly be diminished on the whole by removing the full bridge input diode rectifier and as a result abundant research works are being concentrated on design of bridgeless PFC circuits for increasing the power supply effectiveness. In this category of rectifiers, the current is permitted to flow through a smaller amount of switching devices more willingly than the traditional PFC rectifier. This assists in considerably dropping the conduction failures of the converter, consequently achieving higher efficiency at reduced cost. The performance effect and the functionality of the converter can be investigated in accordance with the dynamic load varying circumstances. Motor loads such as BLDC, PMSM, induction motor etc. possibly preferred for the purpose of dynamic varying analysis. At present, Brushless DC (BLDC) motors have been extensively utilized in the industries, transportation, agriculture and electronics, aerospace and several fields. This paper completely concentrates on the investigation several converter topologies to recognize the potential significance in PFC.

Keywords: Power factor corrector, Brushless DC, Converter, rectifier

Introduction

The wide-ranging exploitation of DC power supplies within several electrical and electronic appliances bring about a mounting requirement for power supplies that receive current with small harmonic content and furthermore have power factor near to unity. DC power supplies are broadly employed inside the majority of electrical and electronic appliances like in computers, televisions, audio sets and others. The existence of non-linear loads effects in small power factor process of the power system. The fundamental block in several power electronic converters are uncontrolled diode bridge rectifiers with capacitive filter. Because of the non-linear character of bridge rectifiers, non-sinusoidal current is obtained from the utility and harmonics are introduced into the utility lines. The bridge rectifiers supply to high THD, low PF, and low effectiveness to the power system. These harmonic currents root numerous setbacks like voltage heating, distortion, noises etc. which effects in low efficiency of the power system. As a result of this statement, there is a requirement for power supplies that obtain current with small harmonic content & also have power factor near to unity.

The AC mains utility supply preferably is expected to be free from elevated voltage spikes and current harmonics. Discontinuous input current that stays alive on the AC mains because of the non-linearity of the rectification process should be shaped to follow the sinusoidal form of the input voltage. The traditional input phase for single phase power supplies functions by rectifying the AC line voltage and filtering with huge electrolytic capacitors. This progression results in a deformed input current waveform with huge harmonic content. Accordingly, the power factor turns out to be extremely poor (approximately 0.6). The drop of input current harmonics and function at elevated power factor (near to unity) are imperative prerequisites for high-quality power supplies. Power factor correction methods are of two kinds – passive and active. At the same time, passive power factor correction methods are the preference for low power, cost sensitive applications, the active power factor correction methods are employed in most of the applications because of their better-quality performance. Converter in power electronics area is an electrical device that transforms power from of an electrical signal or power source, by transforming it from one type to another. DC-DC converters are kind of electronic devices which are employed when essential to transform DC electrical power efficiently from one voltage stage to another stage. In DC-DC converters the impedance level of input energy is transformed from one level to a different. DC/DC converter is principally employed in a system where a synchronized voltage supply is essential to the circuit. The converter manages the DC link voltage by means of capacitive energy transfer which end results in non pulsating input and output currents.

The Isolated DC-DC converters transform a DC input power supply to a DC output power at the same time preserving isolation among the input and the output, in general permitting distinctions in the input-output ground potentials in the limit of hundreds or thousands of volts. They can be an exemption to the characterization of DC-DC converters in that their output voltage is habitually (however not always) the similar as the input voltage. A present-output DC-DC converter allows a DC power

input, and generates as its output steady current, at the same time the output voltage based on the impedance of the load. The several topologies of the DC to DC converter can produce voltages higher, lower, higher and lower or negative of the input voltage explicitly:

- Buck
- Boost
- Buck boost
- Cuk
- Sepic
- Zeta

The traditional boost topology is the most extensively employed topology for power factor correction applications. It includes a front-end full-bridge diode rectifier subsequently the boost converter as illustrated in figure 1. The diode bridge rectifier is employed to correct the AC input voltage to DC, which is then provided to the boost section. This scheme is excellent for a low to medium power range applications. In case of higher power levels, the diode bridge turns out to be an significant element of the application and it is essential to handle the trouble of heat dissipation in inadequate surface area.

Literature Survey

PFC converters

(Zhiguo Pan et al., 2005) [1] formulated a low-cost scheme to Power Factor Correction (PFC) of single-phase diode rectifiers by means of a series active filter. Exploitation of series active filter is a low-cost method to PFC. This PFC has lesser prerequisites of power device ratings, which causes lesser cost, elevated efficiency, and lower electromagnetic interference compared against the traditional PFC. It also can remove the massive inductor required in the traditional PFC. On the other hand, it brings in elevated DC bus stress, elevated switching device ratings, elevated switching losses, and elevated electromagnetic interference (EMI).

(Paul Nosike Ekemezie et al., 2007) [2] formulated an attempt to devise a PFC for AC-DC converter that is geared in the direction of digital control. The PFC circuit makes use of zero voltage transition arrangement to diminish switching losses. This work primarily involves imitation of basic power electronic circuits and the investigation of the current and voltage waveforms. It begins with easy circuits with a steady boost in complexity by addition of new elements and their consequent effect on the current and voltage waveforms.

(Garcia et al., 2009) [3] made an evaluation of the most exciting solutions for single phase applications is performed. They are categorized attending to the line current waveform, number of switches, energy processing, control loops, etc. The most important merits and demerits are emphasized and the field of application is found. They launched certain postulations to direct the system in the direction of linear models. Accordingly, several approaches presumed that the output ripple was

ignored by using a vast output capacitor, which is not satisfactory in design because of its elevated cost and size.

(Villarejo et al., 2007) [4] formulated a new analytical technique for the generalized investigation of a cluster of single-stage power-factor correctors (S2PFCs). Because of this generalized scheme, new topologies have been derived, and the study of additional recognized topologies has been simplified. This technique simplifies the design of S^2 PFCs by making it possible to evaluate a huge number of several designs from the identical point of view with the aim of identifying the best topology. Still, amount of elements is augmented, efficiency is diminished and two control loops are essential.

(Kim et al., 2006) [5] formulated a soft switching unity power factor PWM rectifier, which significantly enhances circuit effectiveness by soft switching, the main switches through a commutation circuit without any auxiliary switches, and also accomplishes considerable reduction of conduction losses on account of a single-stage converter topology rather than a front-end rectifier follow by a boost converter. On the other hand, it has certain demerits since it requires a number of power circuit devices.

(Tze-Yee et al., 2011) [6] formulated an active power factor controller for a PMSM drive to enhance the elevated input current harmonics produced from the power diodes in addition to the switching of the inverter. The comprehensive design is investigated and executed by a motor drive prototype. This kind of utility interface portrays extreme peak input currents and consequently it generates an elevated level of harmonics and small input power factor. Because of low power factor, the load effectiveness is diminished. With the aim of meeting the harmonics bounds, new AC-DC converter designs are required to make use of active PFC at the input.

(Singh & Singh, 2010) [7] formulated a Cuk converter based PFC topology for a PMBLDCM drive and authenticated for a compressor load of an air-conditioner. The PFC converter has guaranteed sensible elevated power factor of the range of 0.998 in extensive range of the speed in addition to input AC voltage. Furthermore, performance constraints demonstrate an enhanced power quality with low torque ripple, even speed control of the PMBLDCM drive. The THD of AC mains current has been noticed well under 6% in the majority of the cases and entirely satisfies the international norms. The functioning of the drive has been found extremely well in the extensive range of input AC voltage with required power quality constraints. This topology has been found appropriate for the applications linking speed control at stable torque load.

Control Strategies For PFC

(Rossetto et al., 1994) [8] highlighted the information on existing commercial IC's. Expansion of these control methods to other PFC topologies is examined and CERTAIN experimental results depending on a PFC SEPIC converter with several control methods are given. On the other hand, when it comes to EMI control, it is essential to adopt specific care in the characterization of the arrangement of the power stage.

(Kripakaran et al.,2013) [9] investigated the control schemes for converters to enhance the Power Factor (PF) and diminish Total Harmonic Distortion (THD) in the input current with output voltage guideline. A novel predictive control scheme for boost PFC is given by this author. Its fundamental idea is that the entire duty cycles necessary to accomplish unity power factor in a half line period are produced by using predictive control. The duty cycle is determined in accordance with the input voltage, inductor current, reference output voltage and reference current. The formulated PFC control is derived in accordance with the Boost converter functions at continuous conduction mode and the switching frequency is much bigger than the line frequency in order that input voltage can be presumed as a stable during one switching cycle. While, harmonic distortion in an inductor of power factor and can reason for power system break downs if not understood and appropriately controlled.

(Hofmann et al., 2003) [10] portrayed the fundamental principles and experimental outcome of a digital control technique for switching power converter functioning in Continuous Conduction Mode (CCM). The process is particularly appropriate for boost converter in PFC applications. On the contrary to other familiar schemes, the new technique requires extremely low hardware and CPU resources and is therefore well convenient for low-cost 8 bit microcontroller. With that it turns out to be sensible that a microcontroller which is previously available in the majority of systems today becomes powerful enough to manage an active PFC circuit or a switched mode power supply practically in a sideline.

(Borgonovo et al., 2005) [11] formulated a scheme for controlling the input current of a single-phase boost PFC. A section of the input voltage is not essential, in view of the fact that it is obviously employed as the reference current. Moreover, the model provides little simplifications, consequently, being more absolute, taking better benefit of the natural features of the converter and obtaining comparable results, when compared to traditional control, by just using a proportional compensator. On the other hand, it experiences from the complications of high cost and a difficult control.

(Grote et al., 2011) [12] provided a digital control scheme which most favourable interleaving of multi-phase boost PFC rectifiers functioning at DCM/CCM boundary (BCM) or in DCM. In this scheme, two feedforward approaches are employed. The initial provides the turn on time to accomplish the required input current and the second works out the switching period time to accomplish BCM operation. An expansion to function in DCM is formulated to circumvent CCM under all situations. Regulated DCM is employed to recognize a new continuous stage shedding process, which is employed to reduce the switching frequency. It is further complicated to recognize interleaving features of a converter with inconsistent frequency operation.

(Karaarslan & Iskender, 2011) [13] formulated two current control methods of an AC-DC boost converter to get unity PF. Single phase elevated power factor rectification is the most commonly accomplished by means of a boost converter. This converter redesigns distorted input current waveform to estimate a sinusoidal current that is in phase with the input voltage. There are numerous current control methods for accomplishing a sinusoidal input current waveform with low distortion. The benefits of this control system are an input current with little distortion and the lack of

need of a compensation ramp; its major disadvantages are inconsistent switching frequency function and sensitivity to noise spikes.

(Kanaan et al., 2008) [14] derived the small-signal averaged scheme of a new Sheppard-Taylor-based DC-DC converter, employed in single-phase PFC applications. Compared to the traditional Sheppard-Taylor converter, this topology permits lower voltage stresses across the capacitors and maximum output voltage range for the similar operating area. In accordance with this model, a carrier-based Pulse-Width-Modulation (PWM) linear control system is developed with the aim of ensuring a unity power factor at the rectifier AC-side and a regulated voltage at the rectifier DC-side. Mutually current and voltage regulators are PI-type. The major benefits of this control scheme over earlier approaches are more sinusoidal input current waveforms, predetermined switching frequency and fewer sensitivity to noise, however it does necessitate the design of extra compensation and it has a sluggish dynamic reaction owing to low bandwidth of voltage feedback loop, like the other schemes.

(Kessal et al., 2012) [15] presented an application of several techniques to control the output voltage of AC-DC converter related with PFC, a traditional PI regulator was utilized, and another depending on fuzzy logic was constructed, the both regulators were included in the voltage loop. In order to decrease the total harmonic deformation of the input current to provide it a sinusoidal shape, hysteresis bands control were employed, the variable band hysteresis provide enhanced results compared against other bands. All these controllers have been assessed via simulation in Simulink and experimental test. The fuzzy logic inference based controller can accomplish enhanced dynamic response than its PI counterpart under large load disturbance and plant uncertainties. In view of the fact that the fuzzy control rules obtain from a heuristic information of system's behaviour neither accurate mathematical modelling nor complex calculations are required to design the fuzzy controller.

(Lu et al., 2005) [16] applied the one cycle control scheme in the bridgeless PFC. With the assistance of one cycle control together the voltage sensing and current sensing matters of the bridgeless PFC circuit can be resolved. Simultaneously, EMI results illustrate that the circuit noise is controllable. The effectiveness enhancement comes at the cost of improved complexity for input voltage and current sensing. Simultaneously, supplementary EMI problems are there. The one cycle control does not necessitate input line sensing and can function in peak current mode, on condition that a easy and high performance solution and overcoming the constraint of bridgeless topology with traditional control. The EMI issues can be also overcome with the help of a modified version of the bridgeless topology. Even though the bridgeless PFC circuit demonstrates slightly elevated EMI levels, the noise is controllable and resembling the traditional PFC circuit EMI.

(Huber et al., 2009) [17] provided a systematic indication of PLL-based closed-loop control techniques for interleaved DCM/CCM boundary boost PFC converters. It is exposed that the PLL-based closed-loop techniques constantly afford steady operation, dissimilar to the open-loop control techniques, where the only technique which results in constant operation is the slave synchronization to the turn-on instant

of the master with current-mode control. It is also revealed that the dynamic reaction of the PLL-based closed the bridgeless topology, on the other hand, undergoes substantial common-mode (CM) noise as the output rails are floating at some point in the negative mains half wave. As an effect, arrangements with either capacitors or diodes as CM return path have to be utilized which cause supplementary losses and increased circuit complexity.

PFC using Zeta Converter

(Singh & Bis, 2012) [24] formulated a novel PFC Converter by means of Zeta DC-DC converter feeding a BLDC (Brush Less DC) motor drive with a single voltage sensor for the purpose of fan applications. A single phase supply followed by an uncontrolled bridge rectifier and a Zeta DC-DC converter is employed to manage the voltage of a DC link capacitor which is lying among the Zeta converter and a VSI (Voltage Source Inverter). Voltage of a DC link capacitor of Zeta converter is controlled to realize the speed control of BLDC motor. The Zeta converter is functioning as a front end converter working in DICM (Discontinuous Inductor Current Mode) and consequently by means of a voltage follower approach. The DC link capacitor of the Zeta converter is followed by a VSI which is feeding a BLDC motor. A sensorless control of BLDC motor is employed to eradicate the condition of Hall Effect position sensors.

(Singh & Singh, 2011) [25] formulated an isolated Zeta converter as a PFC converter by means of DC link voltage control for the purpose of speed control of a permanent magnet brushless DC motor (PMBLDCM). The VSI is employed as an electronic commutator of PMBLDCM. This converter executes the PFC action and DC link voltage control in single phase by means of only one controller. The current multiplier scheme with average current control is employed for operation of the isolated Zeta converter in CCM. A rate limiter in the reference DC link voltage is intended for the purpose of controlling of current and torque in PMBLDCM.

(Argelwar et al., 2014) [26] formulated a Zeta converter fed BLDC motor drive by means of a single voltage sensor for the purpose of fan applications. A single phase supply then diode bridge rectifier and a Zeta converter is employed to manage the voltage fed to the VSI. Productivity of Zeta converter is limited to accomplish the speed control of BLDC motor. A sensorless control of BLDC motor is employed to eradicate the necessity of position sensors.

(Shijith & Sujith, 2014) [27] formulated a PFC and sensorless speed control of BLDC motor by means of zeta converter. Zeta converter is a kind of fourth-order DC-DC converter fabricated of two inductors and two capacitors and potential enough to operate in either step-up or step-down manner. The PFC is accomplished by zeta converter. Sensorless speed control of BLDC motor is accomplished and the cost and wiring of sensors are decreased.

(Bist & Singh, 2013) [28] aimed at the design of BL-Zeta (bridgeless Zeta) converter fed BLDC motor drive. A single voltage sensor is employed for the purpose of achieving PFC and DC link voltage control. Dissimilar to the traditional way of using a PWM switching of VSI, a new scheme of speed control is employed to manage the voltage at the DC link of VSI. A primary frequency switching is utilized

for electronic commutation of BLDC motor for accomplishing low switching losses in the VSI. A voltage follower scheme is exploited for DC link voltage control in BL-Zeta converter operating in DCM (Discontinuous Conduction Mode). Furthermore, the conduction losses in the DBR (Diode Bridge Rectifier) are also eradicated in a bridgeless topology of Zeta converter. A reasonable performance is realized for an extensive range of speed control of BLDC motor and changing supply voltage to investigate the behaviour in practical supply conditions.

From the literature review, it is observed that, various PFC converters have been adopted in different motor applications. The traditional techniques have their own limitations which degrade the overall performance. Some of the limitations of the traditional approaches and the corresponding modification are clearly described in Table 1.

Table 1: Research Gap Evaluation

Traditional Approaches and its Limitations	**Future Modifications Required**
Bridge Less buck and boost converter configurations are not appropriate for certain high voltage applications owing to the necessity of high voltage conversion ratio.	Bridgeless cuk converter functioned in buck mode with stable DC voltage.
Hence, a Diode Bridge Rectifier (DBR) followed by a PFC converter is exploited for enhancing the power quality at AC mains. Several topologies of the two-stage PFC converter are reported in the literature which has resulted in lower efficiency due to higher number of component count for dc link voltage control and PFC operation.	Single-stage PFC converter is proposed which has resulted in higher efficiency due to lesser number of component count for dc link voltage control and PFC operation.
In CCM, the current in the inductor or the voltage across the intermediate capacitor remains continuous, but it requires the sensing of two voltages (dc link voltage and supply voltage) and input side current for PFC operation, which is not cost-effective.	Designing the bridgeless cuk converter operated in buck mode with constant DC voltage.
But, DCM necessitates a single voltage sensor for dc link voltage control, and inherent PFC is achieved at the AC mains, but at the cost of higher stresses on the PFC converter switch.	Designing the cuk converter with lesser number of power utility devices particularly with a single switch.
The PMBLDC motor drive is fed from a single phase AC supply through a DBR followed by a capacitor at dc link. Due to	The proposed work minimizes the THD through Fuzzy logic based speed controller. Moreover, fuzzified output

an uncontrolled charging of the capacitor at dc link, draws a pulsed current. A peak higher than the amplitude of the fundamental input current at AC mains due to an uncontrolled charging of the dc link capacitor. This results in poor power quality (PQ) at AC mains in terms of poor power factor (PF) of the order of 0.728, high Total Harmonic Distortion (THD) of AC mains current at the value of 81.54% and high Crest Factor (CF) of the order of 2.28.	also provides almost unity power factor.

Traditional Cuk Converter

For a traditional uni-directional cuk converter which functions in Discontinuous-Capacitor-Voltage Mode (DCVM), that cannot be completely adopted for the battery equalization application. For coupled-inductor SEPIC and cuk power converters which functions in case of both high-voltage and high-power applications, the conception of multilevel converters is formulated which possibly will circumvent a low-frequency transformer, and diminishes the switching frequency of the devices. It is to be noted that, higher switching losses are acquired for traditional DBR.

The major features to be taken into account in this research work are Mode of Operation of Converter, Converter Topology, electronic commutation, Vector Control Strategy and controlling procedures. The present converter topologies like boost, buck-boost, buck, cuk and sepic had their individual drawbacks based on the particular applications. The familiar drawback observed in all the mentioned converter topologies is that, it possibly will not support high power applications successfully. As a result, a novel cuk converter design with smaller amount of power utility devices with efficient controlling techniques is essential for high power motor applications.

As a result, in every half line cycle, one of the MOSFET functions as an active switch and the other one function as a diode. The dissimilarity among the bridgeless PFC and traditional PFC is that in bridgeless PFC converter the inductor current flows through only two semiconductor devices, however in traditional PFC circuit the inductor current flows through three semiconductor devices. The two slow diodes of the traditional PFC converter are substituted by one MOSFET body diode in bridgeless PFC converter. In view of the fact that both the circuits functions as a boost DC/DC converter; the switching loss of the converters are identical. As a result, the efficiency enhancement in bridgeless PFC converter depends on the conduction loss difference among the two slow diodes and the body diode of the MOSFET. The bridgeless PFC converter also decreases the total elements count as compared to a traditional PFC converter.

One more drawback of this topology is the floating input line relating to the PFC stage ground, which makes it unfeasible to sense the input voltage without a low frequency transformer or an optical coupler. Furthermore, with the aim of sensing the

input current, complex circuitry is required to sense the current in the MOSFET and diode paths independently, given that the current path does not share the same ground for the period of each half-line cycle.

Power supplies with active PFC methods are becoming essential for several categories of electronic equipment to meet harmonic regulations and standards, like the IEC 61000-3-2. Most of the PFC rectifiers make use of a boost converter at their front end. On the other hand, a traditional PFC scheme has lesser efficiency owing to considerable losses in the diode bridge. The current flows through two rectifier bridge diodes and the power switch (Q) at some stage in the switch ON-time, and through two rectifier bridge diodes and the output diode (Do) at some stage in the switch OFF-time. As a result, during each switching cycle, the current flows through three power semiconductor devices. Accordingly, a considerable conduction loss, rooted by the forward volt-age drop across the bridge diode, would humiliate the converter's efficiency, in particular at a low line input voltage.

In order to overcome these disadvantages, numerous bridgeless topologies, which are appropriate for step-up/step-down applications have been recently introduced in (Roh et al 2011) [18]. On the other hand, this topology in (Roh et al 2011) [18] still suffers from having three semiconductors in the current conduction path at some point in each switching cycle. In (Ismail, 2009 [19]; Sabzali et al 2011 [20]), a bridgeless PFC rectifier depending on the single-ended primary-inductance converter (SEPIC) topology is presented. Like the boost converter, the SEPIC converter has the drawback of discontinuous output current resulting in a comparatively high output ripple. A bridgeless buck PFC rectifier was proposed in (Huber et al 2010 [22]) for the purpose of step-down applications. On the other hand, the input line current cannot go after the input voltage around the zero crossings of the input line voltage; in addition, the output to input voltage ratio is restricted to half. In addition, buck PFC converter results in an increased Total Harmonic Distortion (THD) and a reduced power factor (Jang & Jovanovi´c, 2011 [21]).

The Cuk converter provides numerous advantages in PFC applications, like uncomplicated implementation of transformer isolation, normal protection against inrush current occurring at beginning or overload current, lower input current ripple, and Electro-Magnetic Interference (EMI) related with the DCM topology (Huber et al 2010 [22]) the SEPIC converter, the Cuk converter has both continuous input and output currents with a low current ripple. Consequently, for applications, which necessitate a small current ripple at the input and output ports of the converter, the Cuk converter seems to be a probable candidate in the essential converter topologies.

Bridgeless Cuk Rectifiers for PFC Applications

In accordance with the potential efficiency of the Cuk Converter, Abbas A. Fardoun et al (2012) [23] formulated new bridgeless single-phase AC–DC PFC rectifiers based on Cuk topology. The lack of an input diode bridge and the occurrence of only two semiconductor switches in the current flowing pathway at some stage in each interval of the switching cycle result in fewer conduction losses and an enhanced thermal management compared to the traditional Cuk PFC rectifier. The formulated topologies are intended to work in DCM to accomplish approximately a unity power

factor and low total harmonic distortion of the input current. The DCM operation provides extra benefits like zero-current turn-ON in the power switches, zero-current turn-OFF in the output diode, and uncomplicated control circuitry. The three proposed bridgeless Cuk PFC rectifier type 3 are shown in Figure 1.

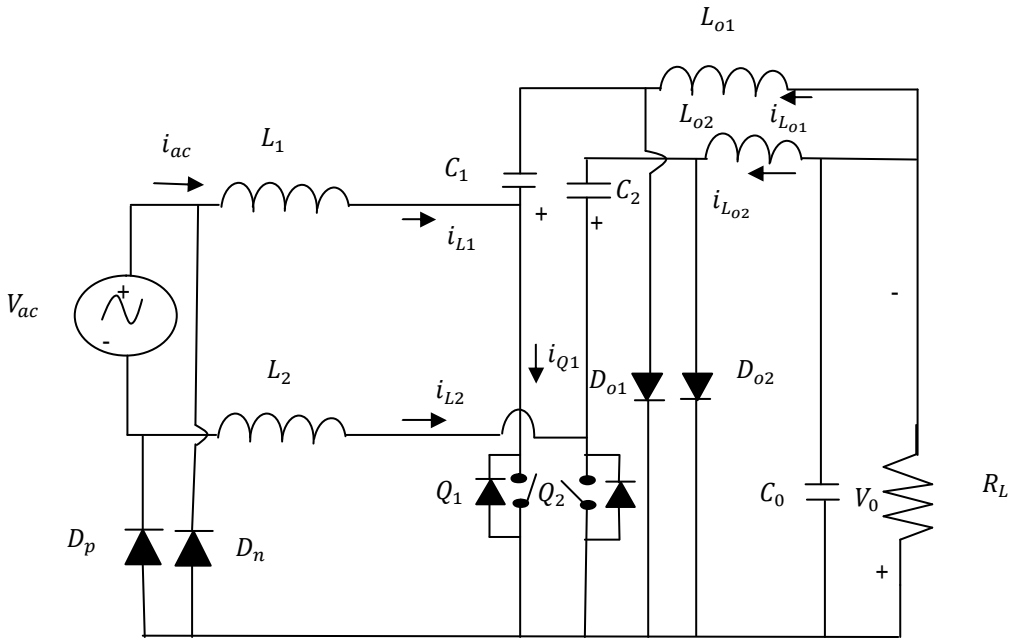

Figure 1: Type 3 Traditional Bridgeless Cuk PFC rectifiers

It is to be noted that by referring Figure 1, the one rail of the output voltage bus is constantly linked to the input AC line through the slow-recovery diodes D_p and D_n or openly as in the case of the topology. Consequently, the proposed topologies do not undergo the high common-mode EMI noise emission setback and have common-mode EMI performance resembling the traditional PFC topologies. As a result, the proposed topologies appear to be promising candidates for commercial PFC products.

The traditional bridgeless rectifiers of Figure 1 make use of two power switches (Q_1andQ_2). On the other hand, the two power switches can be driven by the similar control signal, which considerably simplifies the control circuitry. Compared against the traditional Cuk topology, the construction of the proposed topologies makes use of one additional inductor, which is regularly described as a drawback in terms of size and cost. On the other hand, an enhanced thermal performance can be accomplished with the two inductors compared to a single inductor. It should be pointed out here that the three inductors in the proposed topologies can be united on the same magnetic core permitting significant size and cost reduction. In addition, the "near zero-ripple-current" condition at the input or output port of the rectifier can be accomplished without compromising performance.

Traditional Bridgeless Cuk PFC for type-3 rectifier

Power supplies with active PFC methods are becoming essential for several categories of electronic equipment to satisfy harmonic regulations and standards, like the IEC 61000-3-2. The majority of the PFC rectifiers make use of a boost converter at their front end. On the other hand, a traditional PFC scheme has lesser effectiveness because of considerable losses in the diode bridge.

The Cuk converter presents numerous benefits in PFC applications, like simple execution of transformer isolation, normal protection against inrush current happening at beginning or overload current, lesser input current ripple, and less EMI related with the DCM topology. The traditional topologies are generated by connecting two DC–DC Cuk converters, one for each half-line period (T/2) of the input voltage. The traditional bridgeless type-3 Cuk rectifier of at some point in positive half-line period and at some point in negative half-line period of the input voltage is shown in Figure 1 will be considered in this investigation. The traditional topologies do not undergo high common-mode EMI noise emission setback and have common-mode EMI performance resembling the traditional PFC topologies. Thus, the proposed topologies seem to be promising candidates for commercial PFC products.

Evaluation Study of The Traditional Converter Circuit

As a result of the lesser conduction and switching losses, the above discussed converter topologies can additionally enhance the conversion efficiency when compared with the traditional Cuk PFC rectifier. Furthermore, with the aim of maintaining the same efficiency, the traditional circuits can function with a higher switching frequency. It must be observed that type 2 has the least number of semiconductor devices in the current conduction path. On the other hand, it has two drawbacks such as floating switch and a step-up voltage gain above 2 as given in Abbas A. Fardoun (2012) [23].

The floating switch needs a more complex driver circuitry and characteristically causes higher electromagnetic emissions. The gain range is restricted by the blocking voltage of *Do* 2 at some stage in the positive half cycle of the input line signal resembling the topology discussed in Ismail (2009). This drawback can be reduced by executing input/output galvanic isolation; on the other hand, components with higher blocking voltage capability are required. Type 1 also has the benefit of a lower component count, however a higher current peak. But, type 3 has an elevated component count, however lower stresses. Although, the major limitation of the type 3 circuit is the higher number of semiconductor devices which results in switching losses. In accordance with the motivation of the above mentioned Cuk converter circuit, the present research work formulated a novel cuk converter design which overcomes the limitation of the above mentioned circuits.

Evaluation Study

Table 2 shows the device utility comparison of the traditional and the proposed model. It is clearly observed from the table that the proposed converter design utilizes lesser number of power utility devices. Especially, the number of switches used in the

proposed converter design is just one, where as in the traditional converters, the switches used are more than one. This would result in lesser switching losses which in turn increases the efficiency and decreases the THD%.

Table 2: Device Utility Comparison of the Traditional and the Proposed Model

Configuration	**No. of Devices**					**½ Period Cond.**	**Suitability**
	S_w	**D**	**L**	**C**	**Total**		
BL-Buck (Jang & Jovanovi, 2011)	2	4	2	2	10	5	No
BL-Boost (Huber et al 2008)	2	2	1	1	6	4	No
BL-Boost (Fardoun et al 2012)	2	2	1	2	7	7	No
BL-Buck-Boost (Wei et al 2008)	3	4	1	3	11	8	Yes
BL-Cuk T-1 (Fardoun et al 2012; Fardoun et al 2010)	2	3	3	3	11	7	Yes
BL-Cuk T-2 (Fardoun et al 2012; Fardoun et al 2010)	2	2	3	4	11	11	Yes
BL-Cuk T-3 (Fardoun et al 2012; Fardoun et al 2010)	2	4	4	3	13	7	Yes
BL-Cuk (Mahdavi & Farzaneh-Fard, 2012)	2	3	3	2	10	8	Yes
BL-SEPIC (Sabzali et al., 2011)	2	3	1*	3	9	7	Yes
BL-SEPIC (Mahdavi & Farzanehfard, 2011)	2	3	2	2	9	7	Yes
Vashist Bist & Bhim Singh (2014)	2	4	2	1	9	5	Yes
Proposed Design	1	2	3	4	10	5	Yes

It should be noted that type 2 has the lowest number of semiconductor devices in the current conduction path. However, it has two disadvantages: floating switch and a step-up voltage gain greater than 2. The floating switch requires a more complex driver circuitry and typically causes higher electromagnetic emissions. The gain range is limited by the blocking voltage of D_{o2} during the positive half cycle of the input line signal similar to the topology discussed in Ismail (2009). This disadvantage can be minimized by implementing input/output galvanic isolation; however, components with higher blocking voltage capability are needed. Type 1 also has the advantage of a lower component count, but a higher current peak. Whereas, type 3 has a higher component count, but lower stresses. In conclusion, the converter of choice is an application dependent.

Figure 2 shows the efficiency comparison of the proposed converter design with the traditional converter circuits. The efficiency has been simulated for different various Output power ratings. The efficiency attained by the proposed converter design is observed to be higher when compared with the traditional converter circuits. This is mainly due to the unique conduction mode and the lesser power utility devices in the proposed circuit.

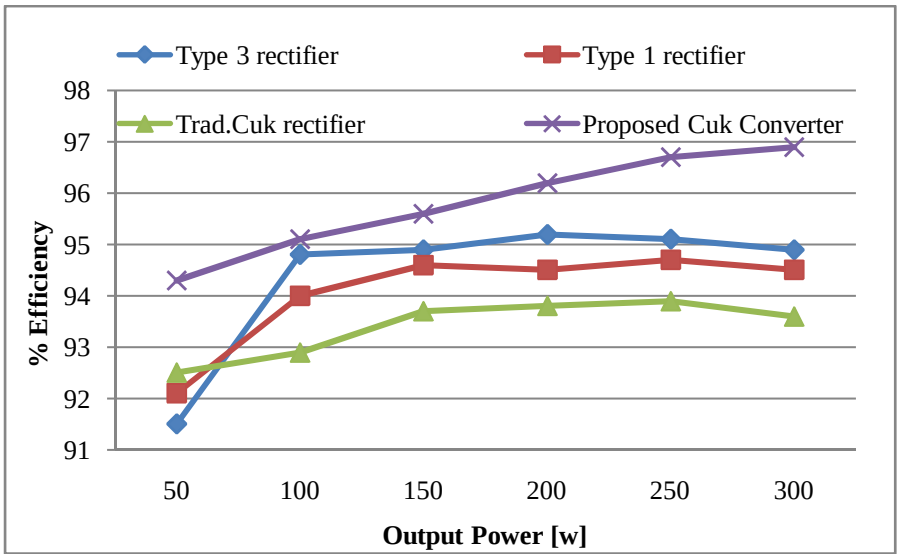

Figure 2: Simulated efficiency of Traditional PFC Cuk, type-1 rectifier, type-3 rectifier and Proposed Converter operating in DCM

Figure 3 shows input current THD as a function of output power. It is evident from Figure 3 that both the proposed and the traditional Cuk rectifier exhibit extremely low THD (<1% for Pout > 100 W) when they are designed to operate in DCM. It is clearly observed that the THD of the proposed converter design is lesser when compared with the traditional converter designs.

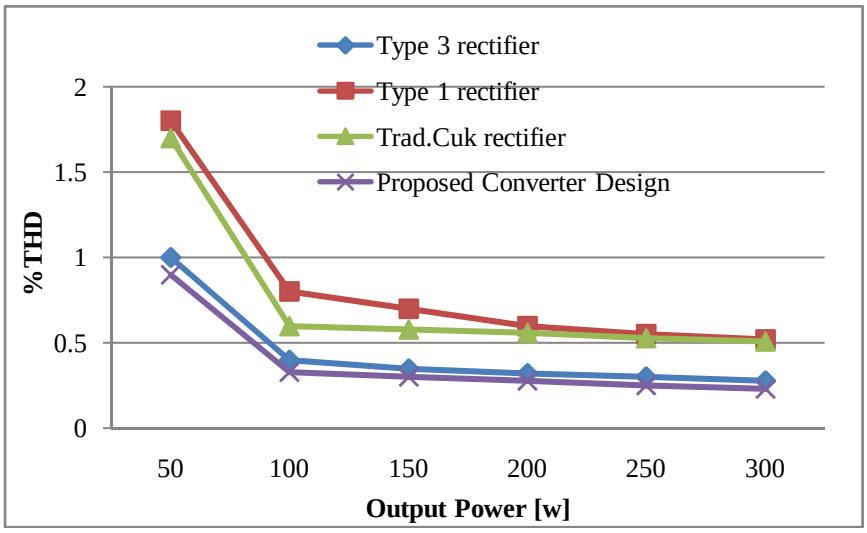

Figure 3: Simulated THD of Traditional PFC Cuk, type-1 rectifier, type-3 rectifier and proposed converter operating in DCM

Summary

This research work discusses regarding the traditional converter topologies and its categories. A comparative analysis among bridged and bridgeless converter rectifiers is made and the significance of bridge less converter and their performance is investigated. Voltage control and power factor correction of a PFC Zeta converter fed BLDC motor drive is discussed. These categories of PFC converters have drawbacks like high voltage stress, particularly in the light load and heavier loss comparing against a typical DC-DC converter. These features critically limit their practical applications. Consequently, a novel PFC cuk converter design is thoroughly investigated further in this paper. In this converter model, four different modes of operations with two modes in positive cycle (switch ON and OFF condition) and two modes in negative cycles with (switch ON and OFF condition) were analyzed. The validity and performance of the converter topologies are verified by simulation results. Because of the lower conduction and switching losses, the converter topologies can additionally enhance the conversion efficiency when compared against the traditional Cuk PFC rectifier.

This research work is inspired by this cuk converter model to guarantee well-organized PFC with interconnected BLDC. However, the main drawback of this converter is that, it employs moderately large number of power utility devices with two switches, four diodes and inductors, three capacitors and two internal diodes across the switch/ Snubber. This possibly will results in higher switching losses. Consequently, the present research work intends to design a bridgeless cuk converter model with lesser power utility components.

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