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Ultra Low Power Sub-Threshold Ring Oscillator

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Abstract

In order to achieve ultra low power nano watt range a circuit must operate in subthreshold regime. A small current flows termed as leakage current while Vdd<Vth, device operate satisfactorily at this low voltage leads to low power consumption without degrading the performance. In this paper body biasing approach has been applied to operate CMOS inverter in subthreshold region. Forward and reverse body bias have effect that threshold voltages can be shifted lower or higher to speed up or slow down devices dynamically. Swapped body bias and dynamic threshold technique introduce for performance improvement of ring oscillator. The proposed oscillator minimum supply is 0.3v required for oscillation consumes power 3nw.

Keywords: Ring oscillator, sub threshold, body biasing, cadence

Introduction

MOSFET is preferred in integrated circuits (ICs) because of their scaling feature. All device dimensions reduce by same factor. Scaling enables to increase speed of circuit, area occupied and decrease total power consumption. According to ITRS road map power consumption serve as central tenet of performance determination. [1] Low power ICs are the demand of current era. Reducing the power consumption is the most challenging tasks. Voltage scaling is an efficient way to achieve low power consumption it results in a quadratic reduction in the dynamic power consumption. Reducing the supply voltage scales down the threshold voltage of MOSFET too, continual reduction of supply voltage suffers from fundamental limitation like leakage current, static power etc. Total power of a CMOS integrated circuit is given by

$$P_{total} = P_{static} + P_{Dynamic}$$

$$= I_{leakage} * Vdd + C_L * V_{DD}{}^2 * \mathrm{f}_{clk}$$

Power in modern digital CMOS integrated circuits has been dominated by dynamic power. In order to reduce power consumption reducing the supply voltage is best choice. For conduction of MOS gate voltage must be greater than Vth.

$V_{GS} < V_{th}$ *NMOS OFF*

$V_{GS} > V_{th}$ *NMOS ON*

$V_{GS} < V_{th}$ a thin channel forms in active area result in small about significant current known as sub threshold current. In subthreshold circuits the supply voltage is reduces below the threshold voltage of a transistor. Due to the quadratic reduction in power with respect to the supply voltage subthreshold circuits are classified as ultra low-power circuits. Sub threshold CMOS circuit functionality are similar to conventional circuit. It is attract attention to low power cmos designer. A sub threshold approach sacrifices speed for power, utilizing leakage currents to drive logic gates.

Threshold Volateg Engineering

Threshold voltage is one of the most important parameter of MOSFET, minimum voltage required to create channel inversion. If the gate bias voltage is not sufficient to invert the surface $V_{GS} < V_{T0}$ the channel current that flows under these conditions is called the sub threshold current. Supply voltage of sub threshold circuit maintained lowers than threshold voltage. In this research work supply voltage is in the range of 0.1 to 0.5V. it is required to have much lower Vth. Threshold voltage can be adjusted by selective dopant ion implantation into the channel region. The body influences the threshold voltage when it is not tied to the source it can be consider as a back-gate. Threshold of NMOS increases by adding extra p-type impurities through bulk terminal. A positive body voltage increases the threshold of NMOS while negative body voltage results in reduction of threshold. Threshold of a MOS is given by well known bosy bias equation [6]

$$V_{th} = V_{t0} + \gamma\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}$$

V_{t0} is threshold voltage for the zero-substrate threshold, γ is substrate bias effect. Positive body voltage of tend to increase the threshold voltage of PMOS at the same time it decrease the threshold voltage of NMOS. Similarly negative body voltage tends to decrease the threshold voltage of PMOS and increase the threshold voltage of NMOS. Forward biasing of body reduces threshold voltage while reverse bias increase threshold voltage [4].

Body bias is technique is a best choice of sub threshold design. It ensures ensure fast switching coupled with effectively turning off the devices when idle in sub threshold regime. There are 3 method insights to introduce body voltage to an inverter namely conventional CMOS, dynamic threshold CMOS and swapped body bias CMOS shown in figure1 [3]

In the standard configuration has the bulk of the NMOS and PMOS tied to the ground terminal and supply voltage (VDD) for CMOS inverter respectively. It reverse biases the bulk terminal.

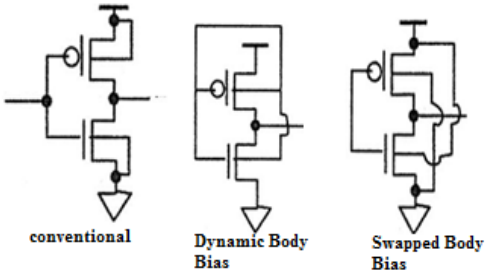

Figure 1: Body biasing scheme of inverter [3]

In DTMOS the bulk of the PMOS and NMOS are connected to the input signals of the circuit. When input switches high to low PMOS turn on since bulk is forward bias threshold voltage reduces, NMOS turns off since bulk is reverse bias threshold decrease. Similarly when input switches low to high NMOS turns on bulk forward bias threshold decrease, PMOS turns off bulk is reverse bias threshold increases. DTMOS lowers the threshold voltage when the transistor is turned on and increases the threshold voltage when the transistor is off. This method can reduce leakage current when the transistor is off.

In the case of the SBB technique the bulk of the NMOS devices are tied to the power supply voltage VDD while those of the PMOS devices are tied to ground. Since bulk of both MOS is forward bias results in lower down the threshold while MOS is operating. Swapping the bulk terminals exponentially increases the sub threshold currents.

In SBB body terminal are permanently shorted to supply or ground. In this research work an addition circuit have been employed to shift dynamically conventional design to SBB based subthreshold circuit. An external body voltage generator is required which supply high or low voltage to body terminal depending on control input.

Cmos Ring Oscillator

Ring oscillator is most important block of frequency generating circuits. CMOS ring oscillator based VCO is the most competitive and promising candidate for high frequency and wide bandwidth. It attract attention because of useful feature (i) easily designed with CMOS technology (ii) consume low input voltage (iii) low power dissipation (iv)large tuning range (v) multiphase output and (vi) adjustable duty cycle.

Ring oscillator contains odd number of delay cell with output of last stage is feedback to the input of first stage [5]. To achieve sustained oscillation an oscillator must provide phase shift of 2π and unity voltage gain this phase shift equally divided between each delay cell.

In this research work a 5 stage ring oscillator shown in figure2 has been designed using conventional, swapped body bias and dynamic threshold based inverter delay cell with cmos 45nm technology. Oscillation frequency of a ring oscillator is depends on number of delay stage N and propagation delay τ_{pd} of each stage [4]

$$F_{osc} = \frac{1}{N 2\tau_{pd}}$$

The propagation delay of a cell is defined as time taken for a change in input node to propagate to the output node (time taken to Vdd/2 crossing point). Delay times τ_{plh} and τ_{phl} is estimated as the average current during charge down and charge up through load capacitor respectively.

$$\tau_{plh} = \frac{C_{load}\,\Delta V_{HL}}{I_{avg}}$$

$$\tau_{plh} = \frac{C_{load}\,\Delta V_{LH}}{I_{avg}}$$

$$\tau_{phd} = (\tau_{phl} + \tau_{plh}) / 2 = (C_{load} * V) / I_{avg}$$

The oscillation frequency of the ring oscillator for N of stages is given by

$$f_{OSC} = \frac{I_{avg}}{V * N * C_{load}}$$

Oscillation frequency increases with current and decreases with higher value of N which leads to large device area. In order to have high frequency current should high which required high supply voltage leads to to high power consumption.

A conventional CMOS 45nm based ring oscillator require minimum supply voltage 0.5V must be greater than threshold voltage. Table I shows the simulation results that GHz rage of frequency can achieve at the cost of power consumption in the range of micro watt.

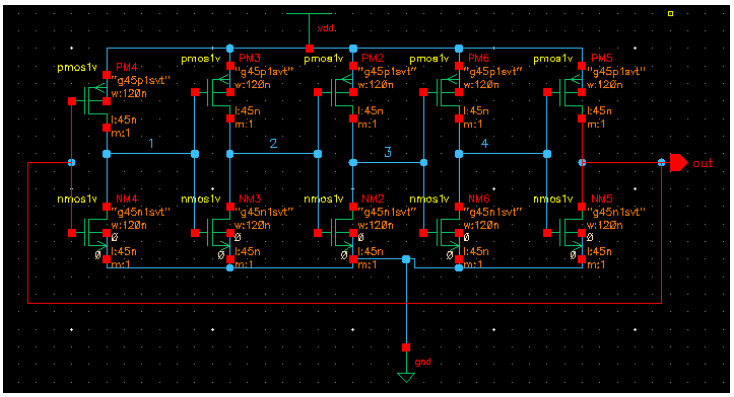

Figure 2.5: Stage Conventional Ring Oscillator

Table 1: Frequency and Power of 5 Stages Conventional Ring Oscillator

Supply Voltage(v)	Oscillation frequency (GHz)	Power Consumption (uw)
0.66	1.997	1.635
0.77	4.536	5.23
0.88	7.48	11.54
1	10.25	20.54

Subthreshold Cmos Ring Oscillator

Sub threshold current which is the leakage current which keeps flowing through a MOS transistor when it is supposed to be blocked. Sub-threshold current as a function of sub-threshold voltage can be ranges from 1µA to 10pA. The sub-threshold voltage characteristics of MOSFET devices allow this voltage to be harnessed and used in the nano power region opening up a wide array of possibilities for useful low power circuits. Oscillation frequency is directly proportional with current. In sub threshold region current is reduced in nano amperes result in significant reduction of power consumption. In the sub-threshold region, the drain current Ids is exponentially related to the gate voltage Vgs as shown in Eqn

$$I_{DS} = I_0 \exp(\frac{V_{GS} - V_{th}}{V_{tm}})[1 - \exp(\frac{V_{ds}}{V_{tm}})]$$

Where $I_0 = {}^{W}\!/_{L}.\mu.C_{ox}.V_{tm}{}^{2}$. V_{tm} is the thermal voltage 26mv at 25°C.

5 stage ring oscillator based on SBB and DT inverter delay cell fig4 &6 has been has been designed using cadence virtuoso 45nm cmos technology and simulation has been performed on cadence spectre simulator. Figure 5 and 6 shows the simulation result of SBB and DT ring oscillator. It is observed that both the circuit starts oscillation from 0.3V onwards.

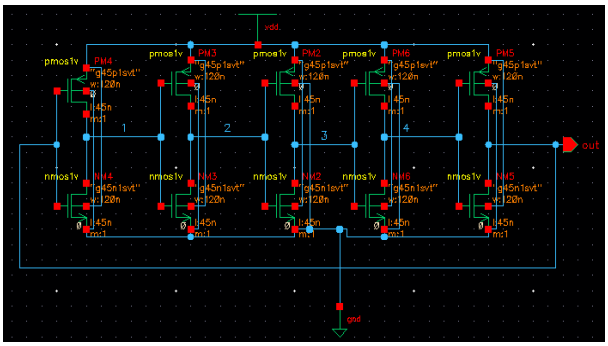

Figure 3: 5 Stage SBB Ring Oscillator

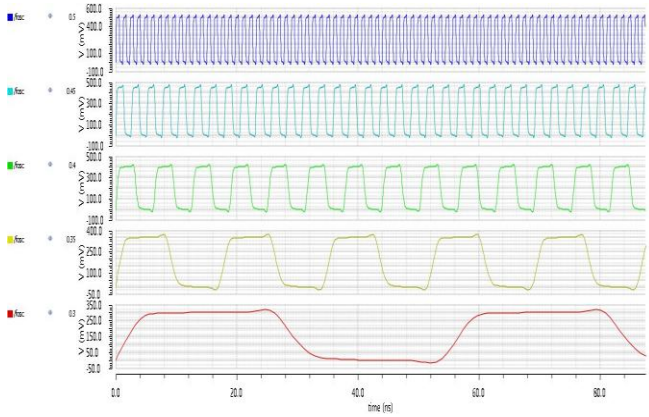

Figure 4: 5 Stage SBB Ring Oscillator Output Waveform

It is observed that SBB ring oscillator starts oscillation at 0.3v. Since power supply lowers down power consumption lowers but frequency reduces as shown in table2.

A DT ring oscillator fig4 starts oscillation at 0.3v. simulation result shows that DT ring oscillator have low power consumption that SBB ring oscillator also have low frequency range due to threshold voltage can be adjusted run time.

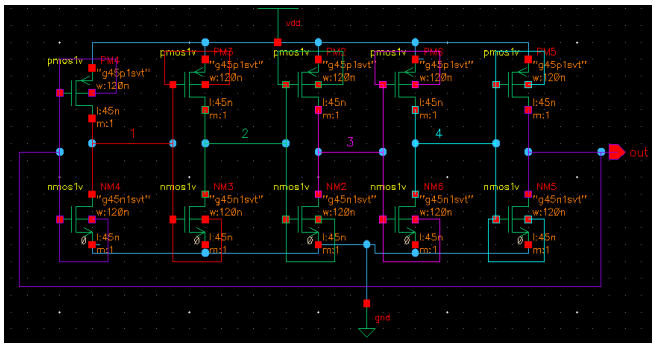

Figure 5.5: Stage DT Ring Oscillator

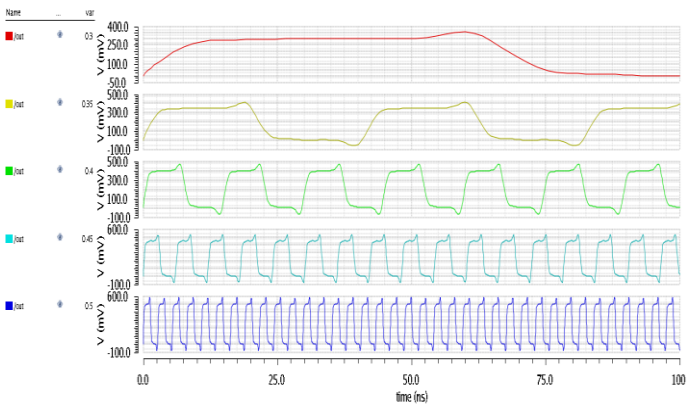

Figure 6.5: Stage Dt Ring Oscillator Output Waveform

Table II shows the frequency and power consumption at different supply voltage.

Table 2: Frequency and Power of 5 Stages SBB & DT Ring Oscillator

Supply Voltage(v)	Oscillation frequency (MHz)	Power Consumption (nw)	Oscillation frequency (MHz)	Power Consumption (nw)
	SBB		DT	
0.3	18.28	3.154	15.38	2.995
0.35	57.93	13.67	24.3	13.2
0.4	159.1	49.81	67.27	48.15
0.45	390.2	158.3	323.8	152.2
0.5	863.2	445.9	369.4	425.4

Conclusion

In this paper implementation of ring oscillator in sub threshold regime have been proposed. Conventional inverter delay based ring oscillator leads to high power consumption; SBB and DT technique have employed to reduce power consumption. It can be observed that the DT technique have low power consumption than SBB technique. Table III shows the performance improvement of dynamic threshold ring oscillator over static threshold. DT has 50.7% power saving compare to SBB

Table 3: Power Vs Supply voltage of SBB & DT Ring oscillator

voltage(mv)	Power(nw)		% Reduction
	SBB	DT	
300	3.154	2.995	5
350	57.93	13.2	77.2
400	159.1	48.15	69.7
450	390.2	152.2	60.99
500	863.2	425.4	50.7

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