International Journal of Applied Engineering Research
ISSN 0973-4562 Volume 10, Number 6 (2015) pp. 14877-14890

http://www.ripublication.com

Analysis of Quantum Devices with Conventional Devices

M.UshaRani[1], Dr.A.SenthilKumar[2]R.Shankari[3], P.Kalaivani[4]

Assistant professor, Dept. of ECE, VELAMMAL Engineering College, Chennai, Tamilnadu, India[1]
Professor, Dept. of EEE, VELAMMAL Engineering College, Chennai, Tamilnadu, India [2]
Assistant Professor, Dept. of ECE, Arunai Engineering College, Thirvannamalai, Tamilnadu, India [3]
Assistant Professor, Dept of ECE, Rajalakshmi Institute of Technology, Chennai, Tamilnadu, India[4]

ABSTRACT:

Multiplier system design is always efficient and fast in the field of electronics especially image processing and signal processing. Multiplier is essential element which contributes to the total system power consumption. Application specific integrated circuits ASIC and VLSI frequently uses various bit width multipliers. Many logical designs were compared and recently reported that quantum logic exhibits only less leakage current and power dissipation than conventional logic. New comparative analysis is performed between CMOS circuits and its logic cells it clearly demonstrates CMOS is efficient than CPL by considering various parameters such as area, speed, power dissipation and power delay. This paper involves the comparative analysis between 2 and 4 bit multiplier system design using conventional and quantum devices.

KEYWORDS*:* FinFET, Quantum Dot Gate FET, TunnelFET, Intermediate Gate Mode.

I. INTRODUCTION

CMOS technology is widely used for integrated circuit construction. Integrated circuits include microcontrollers, microprocessors, digital circuits and static RAM. MOS is also applicable for analog circuitry such as data convertors, imaging sensors and transceivers for highly integrated communication. CMOS is also referred as ComplementarySymmetry Metal Oxide SemiconductorCOS-MOS. Complementary-

Symmetry refers to the digital design logic associated with CMOS which uses symmetrical and complementary pairs of n and p type semiconductors to perform logical operations. Important CMOS device characteristics are low static consumption of power and highly immune to noise. Always one pair of the transistor is turned off; the combination of series transistor draws equal power only during switching operation between off and on states. CMOS devices does not emit much heat when used in other logical functions, example NMOS logic or TTL logic, usually they exhibit some amount of current even in ideal state. CMOS devices in multiplier system also have logic functions of high density on a chip. This was the main reason for using CMOS technology in VLSI chip designing.

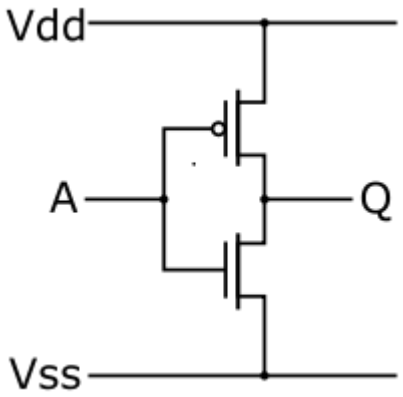

Fig. 1 Static CMOS

CMOS - COMPLEMENTARY METAL OXIDE SEMICONDUCTOR

Metal Oxide Semiconductor refers to the field effect transistor structure; its operation depends upon the current flow controlled by electric field. MOS generally have a metal electrode which acts as gate and is placed on the top of insulator. Semiconductor material used prior is aluminium and now its polysilicon. This paper deals with two mechanisms in runtime for leakage current reduction in CMOS circuits. Assumptions were done in both the cases, and a sleep signal is introduced which is helpful for indicating standby mode circuit. This can be done in both environment and system. First method deals with shifting of internal signals and set of external inputs and the main goal is to set all the logic level values to reduce current leakage. CMOS gate current leakage depends upon applied input combinations. Second step involves addition of both p and n mos gate transistors, which in turn increases the input signal controllability and decreases leakage of current using stack effect.

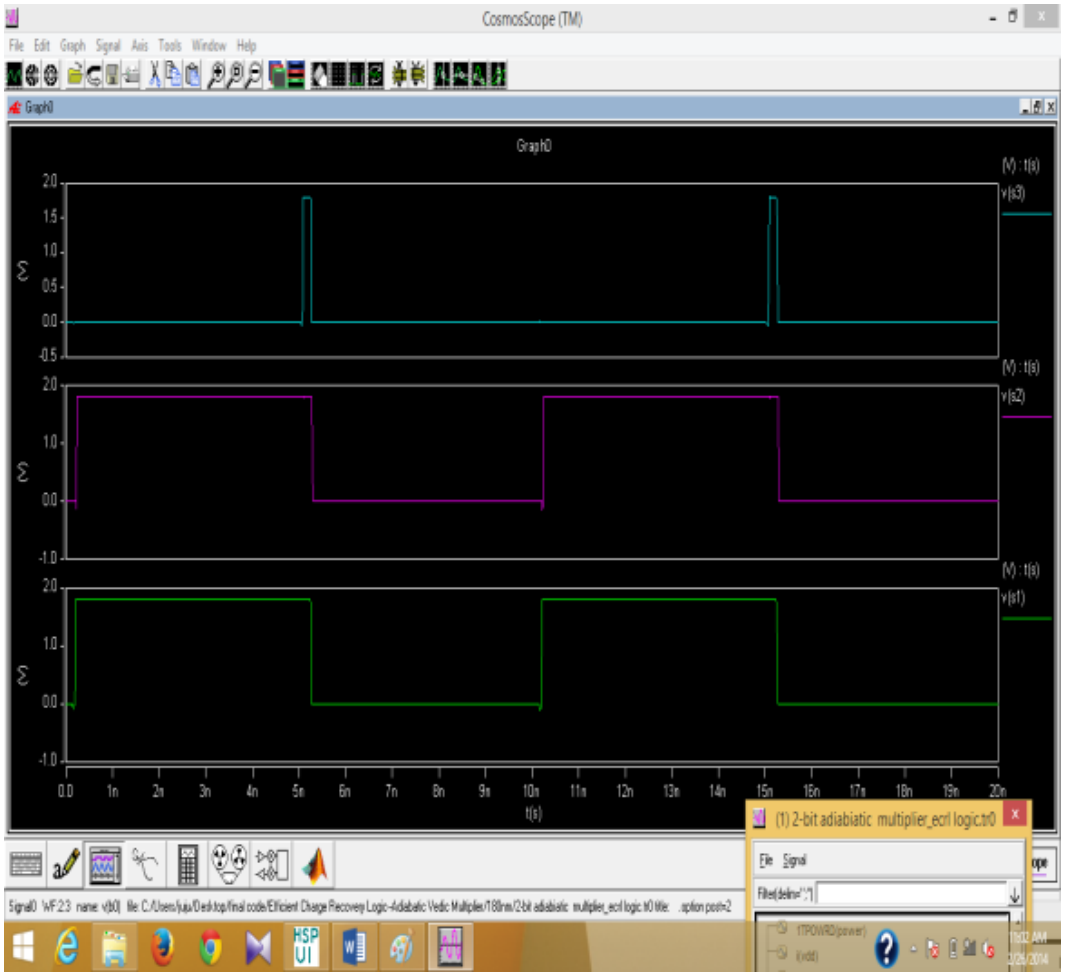

Fig. 24-Bit Adiabatic Multiplier System using CMOS

More amount of current leakage in CMOS contributes to high power dissipation and it increases length of channel, threshold voltage, and oxide thickness of gate. Modeling and leakage component identification is essential for reduction and estimation of power leakage, especially in low power applications. This paper also reviews various intrinsic leakage mechanisms of transistor, which includes drain induced barrier lowering, weak inversion, gate oxide tunneling and gate induced drain leakage. All these components will produce short channel effects, to perform proper scaling in CMOS devices and to manage effects certain channel techniques were followed. It includes halo doping and retrograde well and halo doping circuit techniques for leakage reduction. Standby control technique for leakage, which exhibits the leakage reduction with the help of stacked transistors. Transistors must have minimum area overhead, process technology and power.

EXTRACTED NUMERICAL VALUES FOR CMOS

ivdd= -1.4091u from= 0 to 50.0000n
tplh= -5.0857n targ= 5.0643n trig= 10.1500n
tphl= 5.1080n targ= 10.1580n trig= 5.0500n
peakpwr= 548.9276u at= 40.1721n from= 1.0000n to= 50.0000n
inputpp_a0= 1.8000 from= 1.0000n to= 50.0000n
outputpp_s1= 1.8479 from= 1.0000n to= 50.0000n
iddrms= 12.9816u from= 0 to= 50.0000n
avg_power= -2.5151u from= 1.0000n to= 50.0000n
power= 2.4385u from= 1.0000n to= 50.0000n
average_delay= 11.1855p
power_delay_product= -28.1329a
maxcur_vdd= 9.4734u at= 111.1438p from= 100.0000p to= 1.0000n
maxcur_s1= 142.0320u at= 103.1250p from= 100.0000p to= 1.0000n

CMOS multiplier system exploits more amount of power dissipation and it can considerably reduce the supply voltage. Threshold voltage of transistor can also be reduced to maintain noise margin levels and to have better standby performance. This in turn increases the subthreshold leakage of n and p mos transistors, and set to power saving mode for supply power reduction. Future technologies will get worse and to overcome this leakage current effect a techniques is proposed in logic circuit designs. Devices will operate under standby mode in ideal state without any transmission for low power applications. The proposed multiplier system design consists of minimal area overhead circuit which makes the circuit with low leakage.

II. TFET - GATE ALL AROUND TUNNELFET:

Tunnel field effect transistors are semiconductor switches, used to achieve better standby power performance it is necessary to deal with conventional MOSFETs. Conventional devices can be compared with the help of Denard's scaling rules. Tunnel FETs, also known as Surface Tunnel Transistors (STTs) or TFETs. They are promising devices in low power applications to replace or complement conventional MOSFETs. It offers small subthreshold swing and low off current. TFETs have quantum tunneling effect so it consumes less power. Two conditions exist and during on state, barrier tunneling takes place for current flow from source to drain. When the device gets turned off, barrier will make off current lower than the case of conventional devices.

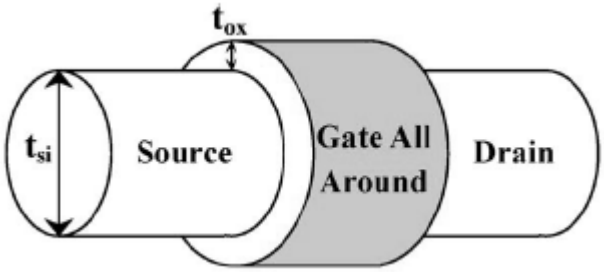

Fig. 3Gate All-Around Tunnel FET

TFETs are p-i-n gated diodes, commonly referred to as gated p-n diodes. Switching takes place between the diodes, during on state certain supply voltage is applied and diode gets reverse biased. Conventional device technology is very much consistent, so the supply voltage is same as in the case of quantum devices. Device terminals were selected in such a way it suits for the TFET operation. Diodes get reverse biased near the pin structure, and tunneling effect can be achieved. NMOS operates only during positive voltage from drain to the gate, and drain is referred to n-region in TFET. P+ region acts as its source for an n-type device. When TFET is OFF, diode leakage current flows between the sources and drain p-i-n structure. In off state energy bands are formed horizontally across the body of a gate all around FET, with applied reverse bias across the p-i-n junction, but no gate voltage exists.

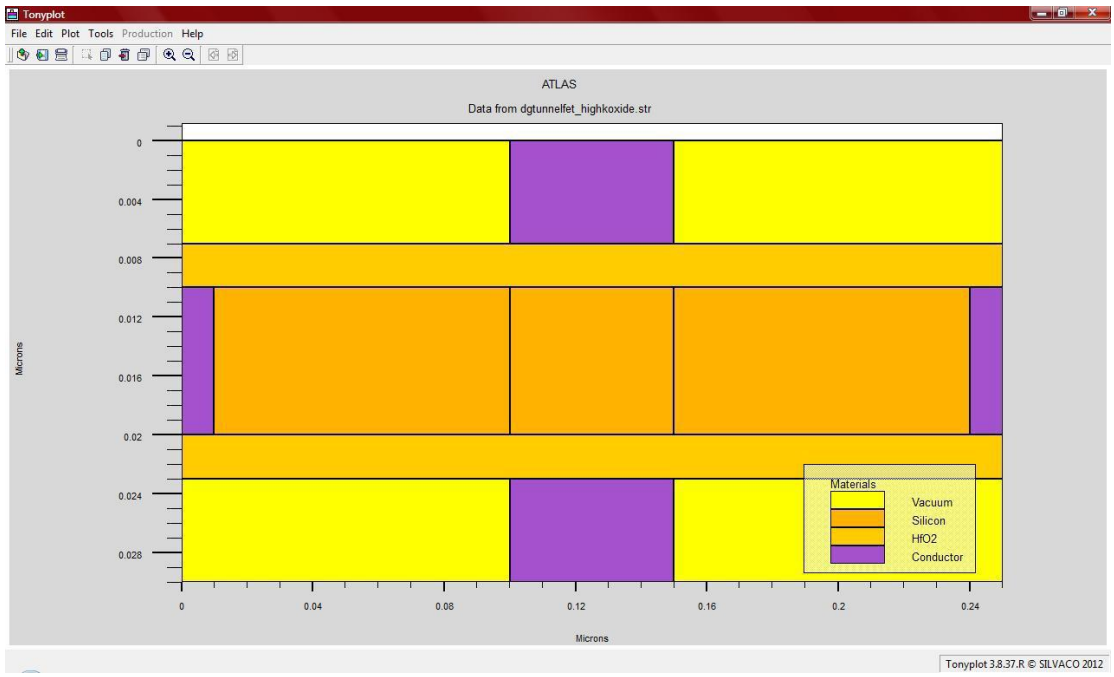

Fig. 4Double Gate Tunnel FET device structure

Gate all around TFET is symmetric between the p and n sides with similar gate alignment and doping levels. It also exhibit ambipolar behavior, when negative supply voltage is applied pFET and positive to nFET it resembles the same transfer characteristics. Energy bands under the gate are lifted in the intrinsic region, and the band-to-band tunneling have very small energy barrier between the conduction and valence band of the intrinsic n+ region.

The n-type TFET on current depends upon the energy barrier width between the p+ regions and n+ intrinsic regions, and the barrier width decreases with increase in current. Metal-oxide-semiconductor field effect transistors were scaled to reduce short channel effects for better packing density and performance. Transistor have figure of merit and it is the subthreshold slope S, which measures the gate change voltage necessary to change the current. Order of magnitude changes when switching the transistor from then on to off state. Gate-All-Around Tunnel FET is a candidate for low power design which offers extremely high speed, low off-state current and potential for achieving steep slopes it provides proper scaling of and gate oxide and body thickness is applied. Band-to-band tunneling is done with electrical measurements in the transfer characteristics. Further, increase in on-state current and a decrease in the subthreshold slope upon reducing the gate oxide thickness.

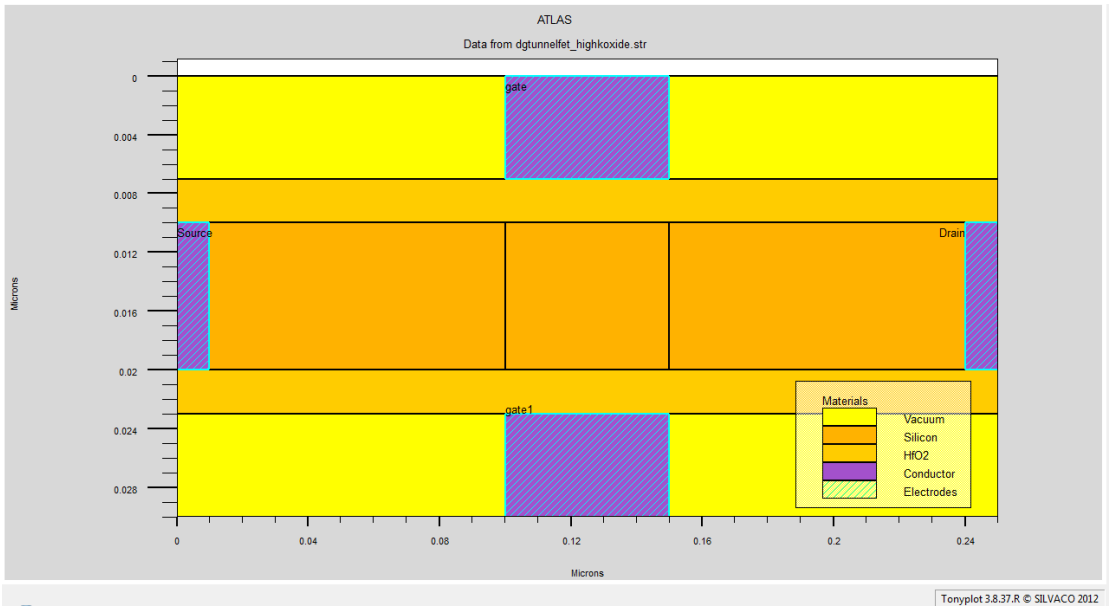

Fig. 5Double Gate Tunnel FET device structure showing electrodes

EXTRACTED NUMERICAL VALUES FOR DG-TFET

1. THRESHOLD VOLTAGE - 0.76429 V
2. SUBTHRESHOLD VOLTAGE - 33.793 mV/decade
3. LEAKAGE CURRENT - 3.136 X 10-5 A/μm

EXTRACTED NUMERICAL VALUES FOR GAA-TFET

1. THRESHOLD VOLTAGE - 0.540666 V
2. SUBTHRESHOLD VOLTAGE - 6.78814 mV/decade
3. LEAKAGE CURRENT - 1.03952 X 10-19 A/μm
4. MAXIMUM ON-CURRENT - 9.25844 X 10-8 A/μm
5. CUT-OFF FREQUENCY - 22 GHz
6. MAXIMUM OSCILLATION FREQUENCY - 248 GHz
7. DEVICE IS UNCONDITIONALLY STABLE FROM 1 GHz ONWARDS

III. QUANTUM DOT GATE FET

Quantum size effect is suggested in many nanostructure semiconductors for the usage of quantum dots in electronic logic combinational design circuits. Solution is inexpensive in processed quantum dot structure, which has high binding energy and sizable band gap. They were successfully demonstrated in the case of LED- Light emitting diodes and in multiplier applications. The multiplier which is used in QDGFET is Wallace tree multiplier. Quantum dot films in QDGFET have well formed near the silicon layer and active channel exists near the organic field effect transistors. These transistors have poor mobility in carrier channel with antiparticles material. QDGFET also have long ligands of organic chain formed near the gate around it. This paper also deals with quantum mechanics and device physics for development of multiplier system. This would improve the quantum dot gate channel standby performance. QDGFET synthesis can be done in many techniques with the help of organic solvents near the quantum well and aqueous layers, it acts as surface interface between the organic phases and micro emulsions. Inorganic nanoparticles use several kinds of generic ligands to stabilize the quantum well. Basic hot injection method is outlined to get fine quality particles. In most cases the reaction flask has precursor made up of metal, which is held initially at a given temperature and the anion gets injected. Often the nucleation temperature is greater than the growth temperature in quantum dots.

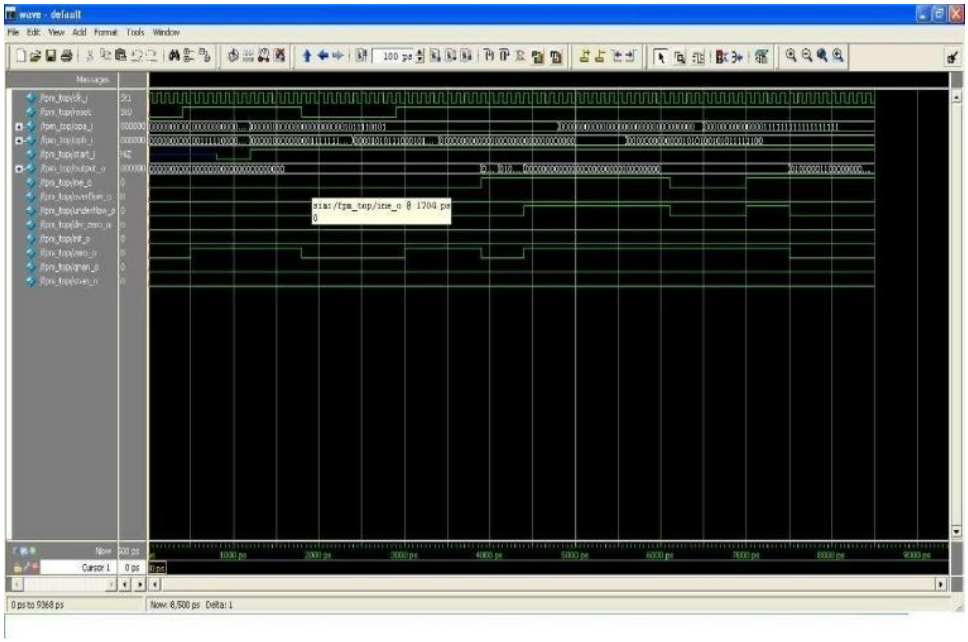

Fig. 64-Bit Multiplier System usingQDGFET

EXTRACTED NUMERICAL VALUES FOR QDGFET

ivdd= -3.6771u from= 0. to= 50.0000n
tplh= -5.0869n targ= 5.0631n trig= 10.1500n
tphl= 5.0972n targ= 10.1472n trig= 5.0500n
Peakpower= 577.4328u at 40.1614n from 1.0000n to 50.0000n
Inputppa0= 1.0000 from 1.0000n to 50.0000n
Outputpps1= 1.0123 from 1.0000n to 50.0000n
iddrms= 26.5053u from to 50.0000n
avg_power= -3.6420u from= 1.0000n to= 50.0000n
power= 3.5760u from= 1.0000n to= 50.0000n
average_delay= 5.1966p
power_delay_product= -18.9259a
maxcur_vdd= 4.4566u at= 116.9721p from 100.0000p to 1.0000n
maxcur_s1= 125.1720u at= 112.5000p from 100.0000p to 1.0000n

This paper deals with the fundamental logic combinational designs using quantum dot gate FETs with three state characteristics. This three state QDGFET manifests with a stable intermediate state transistor, where a wide range of gate input voltages is applied with constant drain current. Threshold voltage varies over this range in QDGFET. A simplified multiplier circuit model was developed for this intermediate state. This model is also applicable for logic circuits which use multivalued logic. Wallace tree multiplier system was designed based on cellular automata of quantum dot is presented, where encoding of digital data is carried out in the positions of two electrons. The combinational logic circuit design consists of a

cell, composed of a ring connected by tunnel junctions with four dots, and two single dot electrometer. The device is operated by applying inputs to the gates of the cell. Logical operations are calculated using the electrometer outputs. Simulations were carried out with the help of H-SPICE and its characteristic parameters were also obtained.

IV. FinFET

FINFETs are semiconductor switches; it is compared with conventional MOSFETs. The CMOS downscaling has led to an improved power consumption, in which leakage current is too high. In order to improve the electronic circuit efficiency, switches are promising candidates to replace or complement the MOSFETs used today. FINFETs, which are gated p-n diodes whose on-current arise from tunneling effects, are attractive new devices for low power consuming applications due to their low off-current and their potential for a small subthreshold swing. The numerical simulations presented here have been carried out using a band to band tunneling model in Tanner tool. In this paper, we discuss logic circuit designs using the circuit model of FINFET. The performance and power characteristics of FinFET logic gates using transistors in various connected configurations are explored. Fin field effect transistor with improved drain and source regions are provided. In some FinFET, the spacers present adjacent to the fins remain while the drain and source regions are removed. Implanting the drain and source regions were carried out with the help of angular implant near gate electrode, thereby it allows more uniformly doped drain. The fin gets reformed by either metallization process or epitaxial growth. In another FinFET device, the spacers were placed adjacent to the sides of fin were silicided and drain source regions were removed. In another embodiment, fins are then reformed by an epitaxial growth process. Embodiment's combination can also be used.

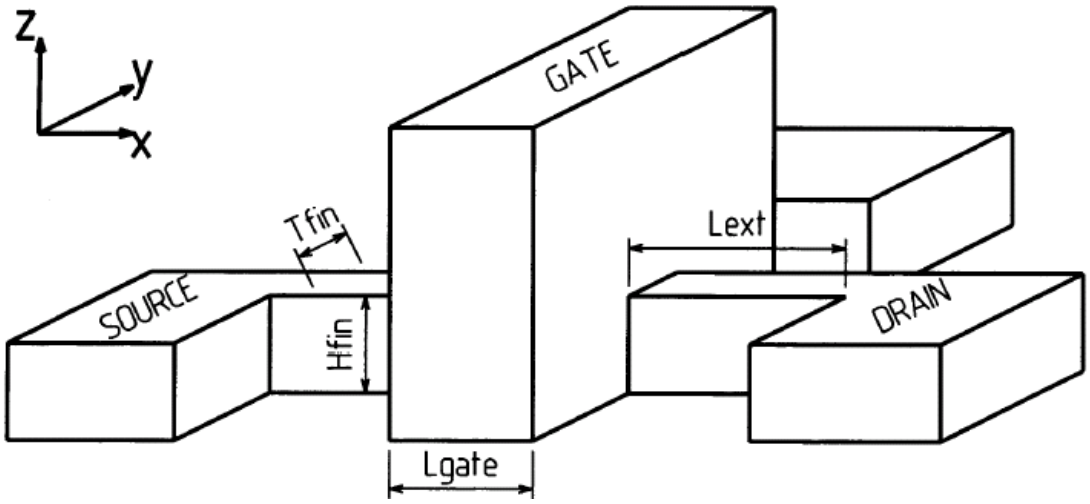

Fig. 7FinFET device structure

In general, three modes of FINFET logic gates are logically obvious: (1) SG- single gate mode, in which FINFET gates are tied together; (2) LP- low power mode, in which the back-gate bias is tied to a reverse-bias voltage to reduce sub threshold leakage and (3) IG- independent gate mode, in which independent signals drive the two device gates. In this paper, we discuss the comparative analysis of various multiplier system designs using CMOS, TFET, QDGFET and FINFET for leakage current reduction.

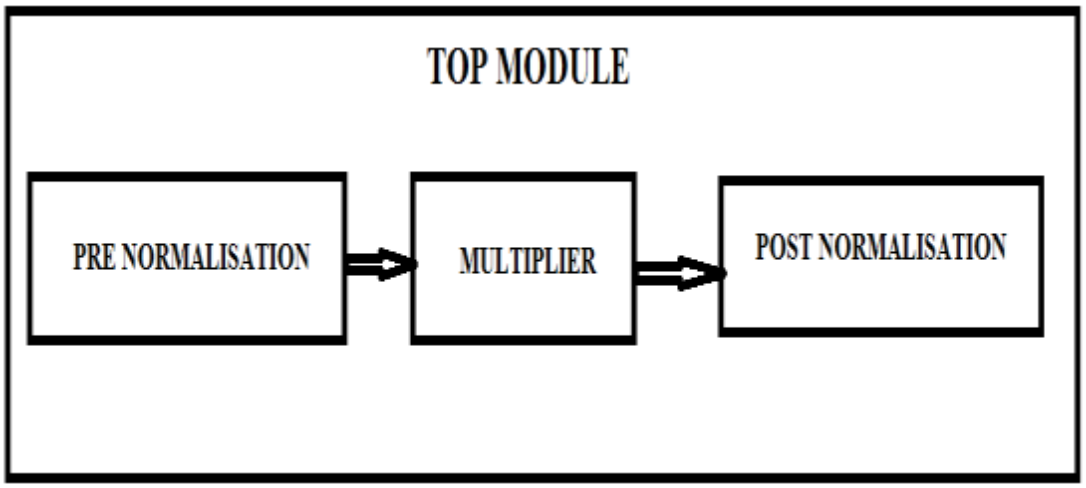

Fig. 8Multiplier flowchart

The proposed FinFET system is to derive the performance and power characteristics analysis of combinational multiplier system design. It uses back of the envelope logic design with the help of pre and post normalization process. FinFET is a multi-gate or trigate architecture which delivers superior scalability level. Above the planar substrate 3D structures arises as FinFETs, which provides increased volume of planar gate within the same area. Drastic control change is applied conducting channel by the gate, which encloses. It allows only less amount of leakage current through the device body even in its off state. Lower threshold voltages were used; it yields more power in optimal switching speeds.

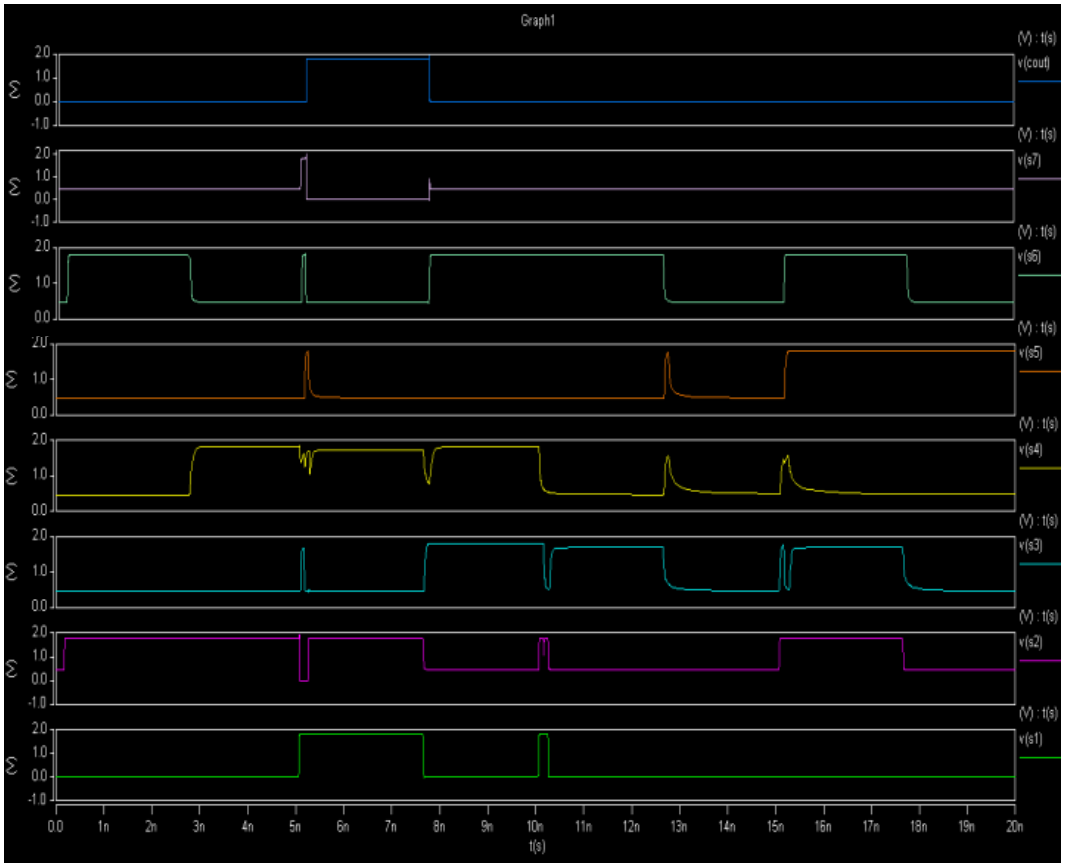

Fig. 94-Bit Multiplier System usingFinFET

EXTRACTED NUMERICAL VALUES FOR FinFET
ivdd=-916.1695n from 0 to 50.0000n
tplh= -5.0888n targ= 5.0612n trig= 10.1500n
tphl= 5.1079ntarg= 10.1579n trig= 5.0500n

Peakpwr= 207.5768u at 40.1627n from 1.0000n to 50.0000n

Inputppa0= 850.0000m from= 1.0000n to 50.0000n
Outputpps1= 861.4596m from= 1.0000n to 50.0000n
iddrms= 7.9165u from 0 to 50.0000n

average_power=-770.5331n from 1.0000n to 50.0000n

power= 756.2551n from 1.0000n to 50.0000n

average_delay= 9.5496p

power_delay_product= -7.3583a

maxcur_vdd= 3.4249u at 116.9721p from 100.0000p to 1.0000n

V. CONCLUSION

Fin field effect transistors and quantum devices are supposed to be the next generation device in the continuous application of Moore's law. FinFET is advantageous, in the case of constant and performance field scaling. FinFET based design has an extremely important task in the accurate modeling of parasitic FinFET. Channel length is reduced by increasing barrier lowering level even at zero applied drain bias, because the source and drain have associated built-in depletion layers. It makes significant patterns in charge balance at short channel effects, with no applied reverse bias to increase depletion width. Device parameters like threshold voltage, subthreshold voltage and leakage current were calculated and comparatively reduced using the multiplier system for various conventional and quantum devices. This was performed in the top module along with the pre and post normalization process. Fast resonant tunneling mechanism of the charge carriers from the inversion channel in the FinFET. The design, stability and RF performance of QDGFET were studied using H-SPICE simulation. The intrinsic and extrinsic parameters were obtained through ac analysis. The cutoff frequency and the maximum oscillation frequency obtained estimate the high frequency performance of CMOS, TFET, QDGFET and FinFET. Comparative analysis study is finally done by comparing the conventional devices along with the extracted quantum device values.

Table 1: Comparative Analysis

PARAMETERS	**CMOS**	**GATE ALL-AROUND TUNNEL FET**	**QUANTUM DOT GATE FET**	**FinFET**
THRESHOLD VOLTAGE	**-1.4091V from= 0 to 50.0000n**	**- 0.76429 V**	**-3.6771V from= 0 to 50.0000n**	**-916.1695V from= 0to 50.0000n**
SUBTHRESHOLD VOLTAGE	**142.0320uV/decade at103.1250p from 100.0000p to 1.0000n**	**- 33.793 mV/decade**	**125.1720uV/decade at 112.5000p from 100.0000p to 1.0000n**	**3.4249uV/decade at 116.9721p from= 100.0000p to1.0000n**
LEAKAGE CURRENT	**-5.0857n targ= 5.0643n trig= 10.1500n**	**- 1.03952 10-19 A/µm**	**-5.0869n targ= 5.0631n trig= 10.1500n**	**-5.0888n targ= 5.0612n trig= 10.1500n**
MAXIMUM OSCILLATION FREQUENCY	**1.8000 from= 1.0000n to 50.0000n**	**- 9.25844 X 10-8 A/µm**	**1.0000 from= 1.0000n to= 50.0000n**	**850.0000m from= 1.0000n to 50.0000n**

PEAK POWER	**548.9276u at 40.1721n from= 1.0000n to 50.0000n**	**- 0.76429 u**	**577.4328u at 40.1614n from= 1.0000n to 50.0000n**	**207.5768u at 40.1627n from= 1.0000n to 50.0000n**
RMS VALUE	**12.9816u from= 0 to 50.0000n**	**18.9056u from= 0to 50.0000n**	**26.5053u from= 0 to 50.0000n**	**7.9165u from= 0 to 50.0000n**
AVERAGE POWER	**-2.5151u from= 1.0000n to 50.0000n**	**-3.8720u from= 1.0000n to 50.0000n**	**-3.6420u from= 1.0000n to 50.0000n**	**-770.5331n from= 1.0000n to 50.0000n**
AVERAGE DELAY	**11.1855p**	**9.1125p**	**5.1966p**	**9.5496p**
POWER DELAY PRODUCT	**-28.1329a**	**-22.879a**	**-18.9259a**	**-7.3583a**

REFERENCES:

[1] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini and T. Elewa Double-gate silicon-on-insulator transistor with volume inversion: a new device with greatly enhanced performance IEEE Elec. Dev. Lett., vol. 8, no. 9, 1987.

[2]. Y. Yang, X. Tong, L.-T. Yang, P.-F.Guo, L. Fan, and Y.-C. Yeo Tunneling field-effect transistor: Capacitance components and modeling IEEE Electron Device Lett., vol. 31, no. 7, pp. 752–754, Jul. 2010.

[3]. David Lovelace, JulioCosto and NatalinoCamilleri Extracting Small-Signal Model Parameters of Silicon MOSFET Transistors WE3C-6, 1994, pp. 865-868.

[4] S. Cho, K. R. Kim, B.-G.Park, and I. M. Kang RF performance and small-signal parameter extraction of junction less silicon nanowire MOSFETs IEEE Trans. Electron Devices, vol. 58, no. 5, pp. 1388–1396, May 2011.

[5] R.Wang, J. Zhuge, R. Huang, Y. Tian, H. Xiao, L. Zhang, C. Li, X.Zhang, and Y.Wang Analog/RF performance of Si nanowire MOSFETs and the impact of process variation IEEE Trans. Electron Devices, vol. 54, no. 6, pp. 1288–1294, Jun. 2007.

[6] G. Gonzalez Microwave Transistor Amplifiers Analysis and Design Englewood Cliffs, NJ: Prentice-Hall, 1997.

[7] A. A. Ketterson, J.-W.Seo, M. H. Tong, K. L. Nummila, J. J. Morikuni, K.-Y.Cheng, S.-M. Kang, and I. Adesida, "A MODFET-based optoelectronic integrated circuit receiver for optical interconnects, " IEEE Trans.Electron Devices, vol. 40, no. 8, pp. 1406–1416, Aug. 1993.

[8] S. M. S. Imtiaz and S. M. El-Ghazaly, "Performance of MODFET and MESFET: A comparative study including equivalent circuits using combined electromagnetic and solid-state simulator, "IEEE Trans. Microw. Theory Tech., vol. 46, no. 7, pp. 923–931, Jul. 1998.

[9] H. Rohdin, A. Nagy, V. Robbins, C.-Y. Su, A. S. Wakita, J. Seeger, T. Hwang, P. Chye, P. E. Gregory, S. R. Bahl, F. G. Kellert, L. G.Studebaker, D. C. D'Avanzo, and S. Johnsen, "0.1-μm gate-length AlInAs/GaInAs/GaAs MODFET MMIC process for applications in high-speed wireless communications, " Hewlett-Packard J., no. 4, pp.1–26, Feb. 1998.

[10] K. Kuhn, "Moor's law past 32 nm: Future challenges in device scaling, "inProc. 13th Int. Workshop Comput. Electron., 2009, pp. 1–6.