International Journal of Applied Engineering Research
ISSN 0973-4562 Volume 10, Number 6 (2015) pp. 16121-16128

http://www.ripublication.com

Analysis of 16-Bit Counter Using GDI Technique and CMOS Logic

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Abstract:

This paper presents the simulation of a 16-Bit Counter using CMOS logic and GDI technique. Gate diffusion input logic is a technique to design low power digital circuits that is used to reduce transistor count and power delay product of the digital circuits. The 16-bit counter is designed by using master-slave flip-flop based on GDI technique. In this approach conventional CMOS counter and GDI based counter has been analyzed in terms of delay, power consumption and power delay product. All these parametric analysis had been carried out using Tanner CAD tool with varying supply voltage from 0.8V to 1.8V. The analysis showed that GDI based counter is more suitable for low power application as a counter

Keywords – Master slave D Flip-flop, GDI Technique, CMOS Logic, Low Power VLSI

INTRODUCTION

Counting is the most commonly used operation in real time DSP applications. The counter is designed with the help of flip flop circuits. The energy consumption of flip flops plays an important role in sequential design. The important factors for designing sequential circuits are energy consumption and delay. The energy consumption of counter is improved by using GDI technique. In this chapter the design of low power counter using GDI technique is focused.GDI based counter circuits are analyzed and compared to select the suitable sequential circuits for low power applications.

The GDI technique is based on the use of a simple cell as shown in figure 1. The GDI cell contains three inputs- G (gate input is common for both PMOS and

NMOS, P (Input to the source/drain of PMOS), and N (Input to the source/drain of NMOS). Bulks of both NMOS and PMOS are connected to N or P, so it can be arbitrarily biased in contrast to CMOS inverter [7].

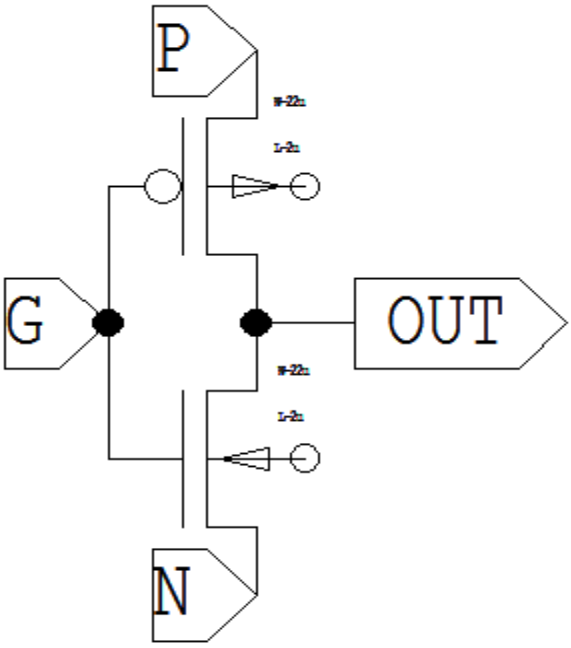

Fig. 1. Basic Gate Diffusion Input Cell

Figure 1 shows the basic structure of gate diffusion input cell. The GDI cell can achieve different Boolean expression with respect to different combinations of inputs G, P and N. The most of the basic logic functions that can be realized with the help of GDI technique involves fewer transistors. The table 1 shows that different configuration modification in the inputs of G, P, and N of the basic logic cell can direct to very different Boolean expressions at the output node [10]. The multiple input gates can be implemented by combining several GDI cells and that can be applied to sequential and combinational circuits for low power signal processing applications [11].

Table 1 Functions of the basic GDI Cell

Input			Out	Function
P	G	N		
B	A	0	A’. B	F1
1	A	B	A’+B	F2
B	A	1	A+B	OR
0	A	B	A.B	AND
B	A	C	A’.B+A.C	MUX
1	A	0	A’	NOT

POWER CONSUMPTION IN SEQUENTIAL CIRCUITS

Sequential circuit is the circuit whose output depends not only on the present state and also depends on the previous state of the circuit [1]. This circuit contains a memory element or storage unit to store the past history of input units. In sequential circuits, the memory elements are implemented using flip flops. Wide utilization of memory storage systems and sequential logic in modern electronics triggers a demand for high performance and low area implementations of basic memory components. One of the most important storage element in sequential circuit is the D flip flop.

Counters are normally used in real time digital signal processing applications. The dynamic power dissipation is described by the following formula $P=CV^2F$.The well known Moore's law states that the transistor density of integrated circuits doubles every 2 years. The integration of device is very important concern of any digital circuits or any processors [6]. In mobile applications, the number of users is increasing day by day. So the energy efficiency plays a crucial role for any device. It is necessary to reduce power consumption of the digital circuits. The product of power dissipation and delay is called as power delay product. Power delay product is high in CMOS logic style compared to GDI technique based logic design. The Counter is used to count the number of clock pulses and it is made by group of flip-flops. The essential one bit storage element called D flip-flop is discussed in [4].Due to increase of delay and area overhead, flip-flops are not widely used in high speed applications[3].The proposed low power technique helps to reduce the leakage power and increase the speed. Counter is generally used as frequency divider in display devices. The reason is, in asynchronous deign the output of one flip-flop is applied as the clock input to the next flip-flop. The formal methods for deriving pass-transistor logic have been presented for n-MOS. They are based on the model, where a set of control signals are applied to the gates of NMOS transistors. Another set of pass signals are applied to the sources of the transistors [9].

Due to the reduction of threshold voltage drop, cascading of pass transistor is very difficult. The major problem that exists in PTL technique is swing degradation. The swing degradation avoided by the use of buffer stage inserted between two GDI cells were analyzed by [2]. The merits of Pass transistor logic over CMOS logic are high speed, less transistor count and lower interconnection effect due to less wiring [8]. A Transmission gate circuit is a parallel combination of both PMOS and NMOS controlled by signals. Any one of the transistor is on at a given instant. It produces logic "1" or logic "0" at the output. At the output end it produces full swing voltage but it requires large area [2].In many of integrated circuits the power dissipation of the clocking system, including the clocking buffers and flip-flops, often consumes the total chip power. Flip-flops and latches are fundamental building blocks of any sequential system [4]. Latency analysis means to analyze the delay between input and output [5].

Design of D Flip-flop Using Conventional Static CMOS Technique

The schematic diagram for D Flip-flop using static CMOS technique is shown in figure 2.The static D Flip-flop consists of Master and Slave latches. When CLK signal

is low internal signals are passed to the outputs. When the CLK signal is high it acts as hold phase. The demerit of conventional static CMOS based D Flip-flop is power delay product.

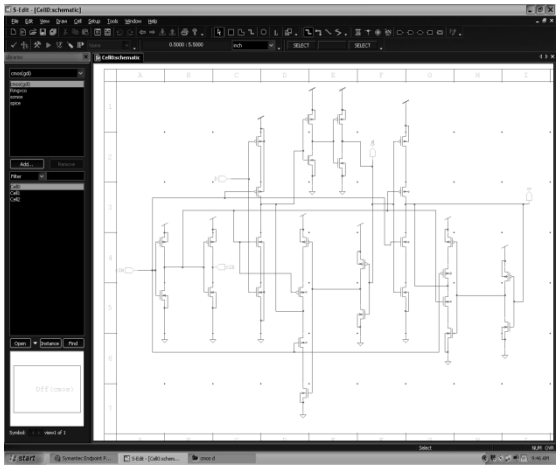

Fig.2. Design of D Flip-flop Using Static CMOS Technique

Design of D Flip-flop Using GDI Technique

A new implementation of GDI technique is presented. This new D FF design allows reducing power-delay product and area of the circuit, while maintaining low complexity of logic design. It is based on the Master-Slave connection of two GDI D-Latches. The components of the circuit are body gates and inverters. The body gates are controlled by the CLK signal and create two different paths between the inputs to the output of the latch. When the CLK signal is low, the signals propagate through PMOS transistors. When the CLK signal is high, internal values are maintained due to the conduction of NMOS transistors.

It is based on the Master Slave connection of two GDI D Latches [7]. Each latch cell consists of four basic GDI cells. The transmission of the signal is performed through the diffusion nodes of the GDI cells. It might cause a threshold voltage drop in the output signals. The limitation of GDI cell is overcome by adding inverter at the output level. This inverter acts as a buffer and is used to maintain the proper voltage at the outputs. The schematic of D Flip-flop with buffer using GDI technique is shown in figure 3.

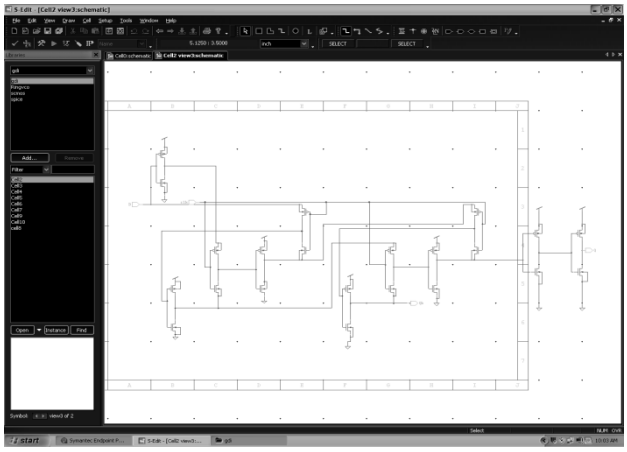

Fig.3. Design of D Flip-flop with buffer using GDI technique

Design of Counter Using GDI Technique

In general, counters are realized by using Flip-flops in the sequential circuits.

The count range is from 0 to 2^n-1 for up counter and from 2^n-1 to 0 for down counter, where **n** indicates the number of Flip-flops used in sequential circuits. The counters realized by using GDI based D Flip-flops produce better results than conventional static CMOS based D Flip-flop.

Simulation Results & Discussion

Figure 4 shows the T-spice output containing the input signals (D, CLK) and output signals (Qm, Q) of D Flip-flop using conventional static CMOS technique.

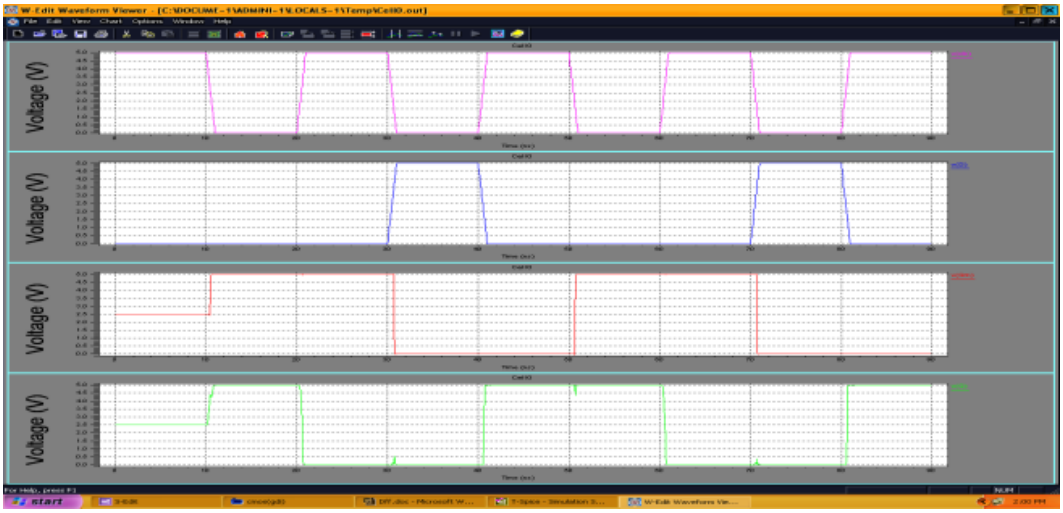

Fig.4. output waveform of D Flip-flop using Conventional Static CMOS technique

The low output voltage swing of the GDI based D Flip-flop without buffer is improved by using properly sized inverter. Inverters act as buffer to maintain proper voltage swing of signals. Figure 5 shows the output waveform containing the input signals (D, CLK) and output signals (Q, Qb) of D Flip-flop using GDI technique with buffer.

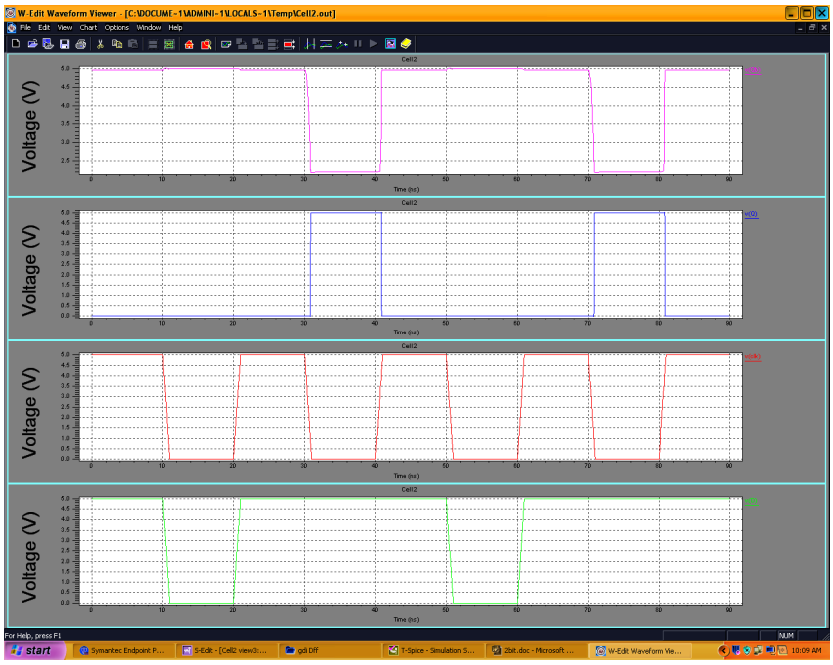

Fig.5. Output waveform of D Flip-flop using buffer in GDI technique

16-Bit Static CMOS counter:

The implementation of static CMOS counter can be designed by using master slave D Flip Flop. The total transistor count in 16-bit static CMOS counter is 448.The existing 16-bit counter is shown in figure 6.

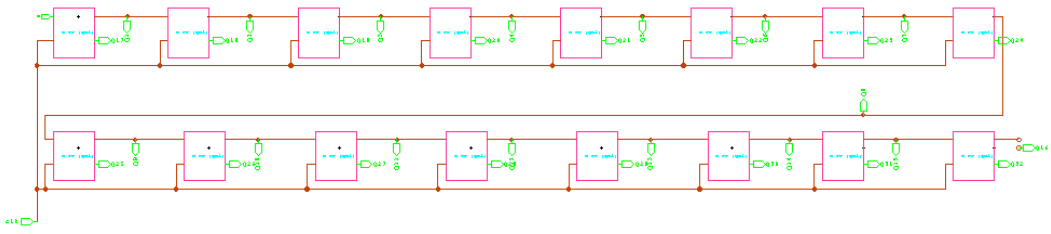

Fig.6. Existing 16 Bit Static CMOS Counter

16 Bit GDI counter:

The implementation of GDI counter can be designed by using master slave GDI based

D flip-flop. The proposed 16-bit counter using GDI technique is shown in figure 7.

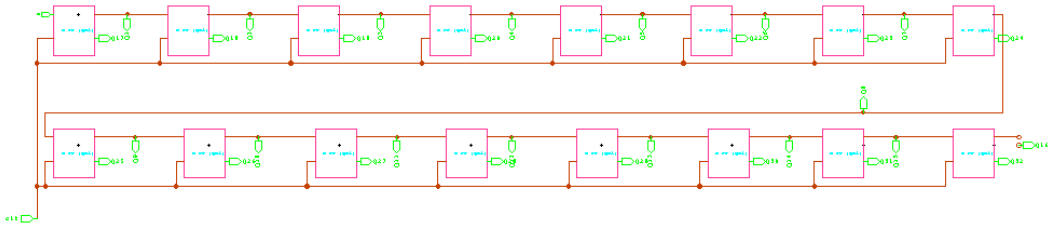

Fig.7. Proposed 16 Bit GDI Counter.

Table 2: Analysis of Power, Delay, and Power Delay product by using various voltage levels

Operating Voltage in Volts	16-bit counter using GDI technique			16-bit counter using CMOS technique		
	Power (µw)	Delay (ns)	PDP (10^{-18}) J	Power (µw)	Delay (ns)	PDP (10^{-18}) J
0.8	0.006320	0.00793	0.05011	0.005565	0.01070	0.059545
1.0	0.009876	0.0124	0.1224	0.008696	0.01672	0.1453
1.2	0.01422	0.01785	0.2538	0.012522	0.02407	0.3014
1.4	0.01935	0.0243	0.4702	0.01704	0.03277	0.5584
1.6	0.02528	0.03174	0.8023	0.02226	0.04280	0.9527
1.8	0.03199	0.04513	1.4437	0.02817	0.05417	1.5259

The table 2 gives the analysis of 16 bit counter using GDI technique and CMOS logic. The results are analysed with the help of tanner software with temperature of 27^0 C.

The proposed GDI based 16 bit counter is analysed by varying the supply voltages from 0.8 V to 1.8 V. All the simulations are carried out by using 180nm technology node.

CONCLUSION

The main focus of this paper is to design low power counters circuits. This paper proposes the Gate Diffusion Input (GDI) technique to design the counters for achieving high speed operation in DSP applications. This is a better style when compared with the existing CMOS design in terms of area and power delay product. The total transistor count is reduced to 30% in comparison with CMOS style and also the power delay product has been reduced in the amount of around 20%. Thus this logic style has created a better platform for the design of the sequential circuits. The implementation of 16-bit counter thus has been presented using GDI technique and can be extended to higher configurations in the future.

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