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FPGA Based Digital Pulse Width Modulator Technique For Digitally Controlled DC-DC Converters

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Abstract

Portable electronic devices and other battery powered devices need a device to reduce the battery voltage to lower voltage. A simple way to reduce the battery voltage is to use low dropout (LDO) voltage regulators, unfortunately power not delivered to load is lost as heat making LDO unsuitable for battery powered applications. An alternative way is to use a switching converter to reduce battery voltage to lower DC voltage. Switching converters uses transistor as switch to control the power delivered to the load. The regulation of output voltage with the switch is achieved by varying the duty cycle of the switch with pulse width modulation control technique. In this paper Digital Pulse Width Modulator (DPWM) architecture is proposed which uses gray counter and one hot encoder to derive a PWM pulse to control the duty cycle of switch. This approach consumes low power as compared to traditional DPWM techniques.The proposed DPWM architecture is implemented in low cost SPARTAN 3A FPGA utilizing Digital Clock Manager (DCM) available in FPGA.

Keywords: Digital Clock Manager (DCM), FPGA, Gray counter, Digital Pulse Width Modulators, Switching converters, FPGA

Introduction

Increased use of handheld and portable battery powered electronic devices seeks the need for power management system. Power management techniques improve the battery life time and also efficiency of the devices. Power management system refers to the generation and control of voltages to operate the electronic devices. Linear and switching regulators are typical elements in power management technique. Linear

regulators have low noise but inefficient in terms of power loss. Switching regulators are efficient in terms power as compared to linear regulators. As portable devices need a low power consuming and high efficiency DC –DC converter, switching regulators can be used to provide appropriate supply voltage to these type of devices [2]. In switching regulators output voltage is sensed and regulated by the switch control circuit. FET switches used in these type of converters are controlled by pulse width modulation technique to regulate the output voltage. With pulse width modulation technique the regulation of output voltage is obtained by varying the duty cycle of the switch. Duty cycle refers to the period of switch is kept ON to the cycle period. Pulse width modulation can be achieved with both analog and digital techniques. Analog techniques are suffers from temperature changes and noise so an alternate digital control technique can be used as pulse width controller or switching controller to these types of switching regulators. Digital controllers can be realized with DSP's and ASIC. But in the switching regulator switching frequency is in the range of MHZ leads to power losses. With advancement in Very Large Scale Integration Technology (VLSI) and development of design tools it is possible to develop a digital switching controller which has high speed and lower power realized with Field Programmable Gate Array (FPGA). As FPGA's are interconnection of logic blocks the DPWM architecture can be easily implemented in it and the architecture can changed by changing the connection between logic blocks depending on the application. DPWM implemented in FPGA can be used as switching controller to control switching regulators used in batter powered applications [10].Traditional DPWM techniques are counter and comparator based and these techniques uses binary counter [3]. For each change in switching level multiple bits changes at a time in a binary counter and these counter and comparator are power consuming devices. The PWM signals generated by these methods is not constant, they are duty cycle dependant. The output PWM signal value is given by

$$\text{Output} = \text{Duty cycle (D)} * \text{input} \quad \text{----------} \quad (1)$$

$$\text{Duty cycle } D = T_{ON}/(T_{OFF}+T_{ON}) \quad \text{----------} \quad (2)$$

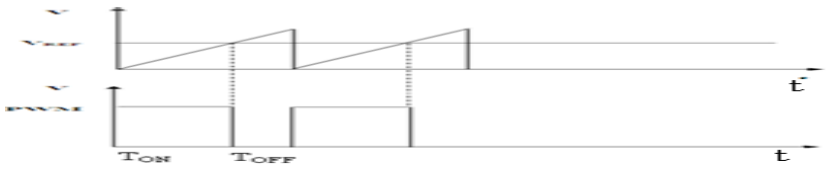

Figure 1: PWM with Duty Cycle

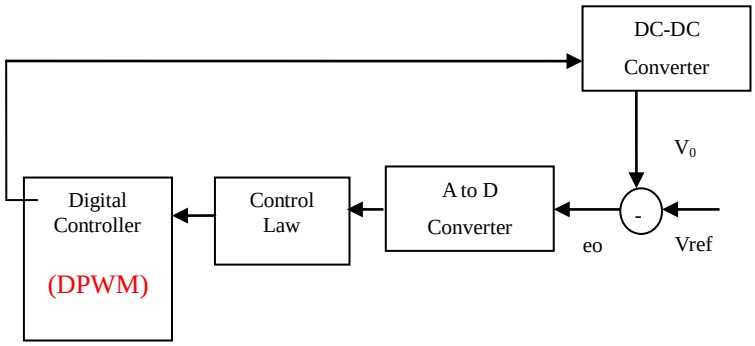

Figure 2: Block of Digital Control Scheme for DC-DC Converters

This paper presents two DPWM architectures the first architecture uses the binary counter and comparator with Delay Locked Loop clocking capability available in almost all FPGA's [3] to generate the variable duty cycle PWM pulse. The second architecture uses the gray counter and one hot encoder with Delay Locked Loop clocking capability and generates variable duty cycle PWM pulse.

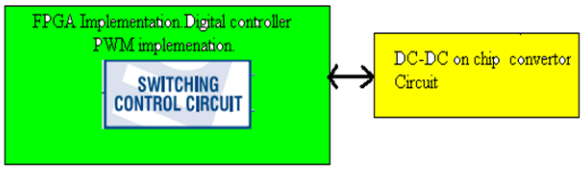

Figure 3: Digital Controller Realised with FPGA

The output voltage of a DC-DC convertor depends on the pulse generated by the switching control circuit (FPGA Digital controller-PWM).

Literature Review

There are different architectures available for DPWM to generate PWM pulses [3], each of them differs on the type of counter realization and also the based on the methodology used for generation of PWM pulse.

Counter Comparator Based DPWM Architecture

This DPWM architecture uses binary counter, comparator along with RS latch to generate the PWM pulse of variable duty cycle [3].With higher switching frequency and high resolution the clock frequency is high so it increases the power consumption.

PWM architecture with variable duty cycle from 0% to 100% is achieved with usage of DCM block in FPGA [1]. Comparator compares the counter data, with up-down counter data generated with push buttons and generates variable PWM pulse. This architecture uses DCM to decrease the clock frequency which minimizes the skew of clock signal.

Delay Line Based DPWM Architecture

This method eliminates the need for higher clock frequency by using a delay line in which a pulse from a reference clock starts the cycle, when the time delay matches with delay experienced through the multiplexer it sets the PWM pulse to high, when reference clock travels through the delay line and reaches the output selected by the multiplexer it set the PWM output to low [6]. In this method the area increases with increase in resolution bits of multiplexer and causes gate delays

Hybrid DPWM Architecture

A hybrid architecture combining the delay line and counter [7] approach. This new architecture provides a compromise between area and power consumption .It uses 32 cell ring oscillator and 32:1 multiplexer. This architecture is developed for low power and lower voltage levels but the control circuit consumes much power which affects the overall power conversion efficiency.

DLL Based DPWM Architecture

A new FPGA based Digital pulse width architecture [4] that utilizes the DLL block present in FPGA. This architecture combines a synchronous block with an asynchronous block for increased resolution without increasing the clock frequency. Synchronous block used is counter based with the input clock frequency multiplied by four with help of advanced feature of DLL. Asynchronous part is complex in nature uses the lower clock frequency and phase shifting capability of DLL for decreased power consumption. This clock phase shifting capability improves the resolution of counter based solution with available number of clock pulses. However this approach has different delay for each data paths which minimizes linearity of proposed DPWM.

Proposed Gray Counter Based DPWM Architecture

Gray counter based DPWM architecture was propsed. The simulation results were obtained and power analysis report is obtained for different frequencies.

The block diagram of the proposed architecture is shown in Fig.3.

DCM Block

The key module in the proposed DPWM architecture is DCM block of SPARTAN 3 FPGA. Proposed architecture utilizes the advantage of Delay Locked Loop (DLL) capability of DCM block. Input signals to DLL block is CLKIN and CLKFB and provides CLK0, CLK2X, CLK180, CLK90, CLK2X180, CLK270, CLKDV clock signals. This advanced clocking capability of DCM minimizes the clock skew[11] by eliminating the clocking delay on routing network caused by loading differences.

Proposed architecture uses the clock multiplying capability (CLK2X) of the DCM block. The external clock frequency is multiplied internally which eliminates the need of using the higher external clock frequency. When higher external clock frequency is used it increases the size of parasitic components in the circuit. Further power consumption is also increased with higher external clock frequency. The external frequency to the proposed architecture is 12.5 MHZ which is multiplied internally by

factor of two (CLKL2X) to yield 25 MHZ clock frequency.

Counters

Traditional DPWM architectures use binary counter, comparator to generate variable duty cycle PWM pulse. Binary counter used is a simpler one but in binary counter multiple bits changes at a time when switching from one state to other state.It causes multiple flipflops to change its state at a time and it consumes more power and also introduces glitches so the binary counters are not efficient in terms of power. In DPWM architectures these binary counters increments its value by one for each clock pulse, when the final value is reached it sets the PWM pulse. Comparator is used to compare the binary counter value with predefined value. When the predefined value is reached in binary counter PWM pulse is generated. As power consumption is a major issue in design of switching controllers used in mobile and portable electronic applications it is necessary replace the binary counters with an alternate design which reduces the power consumption.

Gray counter is used in the proposed architecture where only one bit changes at a time for each state transition. In other words only one flipflop changes at a time so gray counter can be of low power. Gray code counter consumes half of power as binary counter and has less noise. Designing of gray counter is complex task against designing of binary counter as the deciding of next state in gray counter needs an extensive logic

In the proposed method a four bit gray counter is designed which on receiving clock pulse starts counting from 0000 to 1000.When final count 1000 is reached it sends a enable signal to one hot encoder.

One Hot Encoder

One hot encoder is a digital circuit in which only one bit of state variable is one at a time and remaining bits are zero. Each bit in a state variable needs a flipflop, so one-hot encoding is better suited for use with the fan-in limited and flip-flop-rich architecture field-programmable gate arrays (FPGAs) offered by Xilinx. The next state in one hot encoder is easily derived from state diagrams so they are simple, ease to use, faster and speed doesn't depend on number of states. One hot encoder uses less number of gates reduces the area, consumes less power. However if the number of states is small the speed is limited due to delays from inefficient use of configuration logic blocks(CLB's).

Pulse Width Control Circuit

Pulse Width circuit is a group of multiplexer connected together. It receives the input signal D_0-D_{15} from one hot encoder, when the D_{15} bit of one hot encoder set to high state pulse width control circuit issues set signal to SR flip flop connected to it. When one hot encoder reaches a particular state based on the control signal for modulating the duty cycle of PWM pulse, pulse width Control Circuit resets the SR flipflop. The PWM pulse width depends on set and reset condition of SR flipflop.

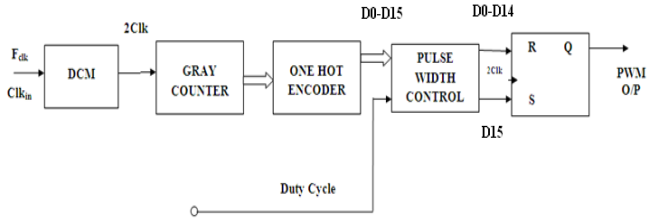

Figure 4: Block Diagram of Proposed Gray Counter Based DPWM Architecture

Results and Discussion

Binary Counter Based DPWM Architecture

Binary counter based DPWM architecture with 8 bit counter, an 8 bit register with overflow detector and SR flip flop [3] was designed with VHDL. Behavioral simulations results were obtained for functional verification and synthesized with XILINX ISE 13.3.The target FPGA was low cost SPARTAN 3A.

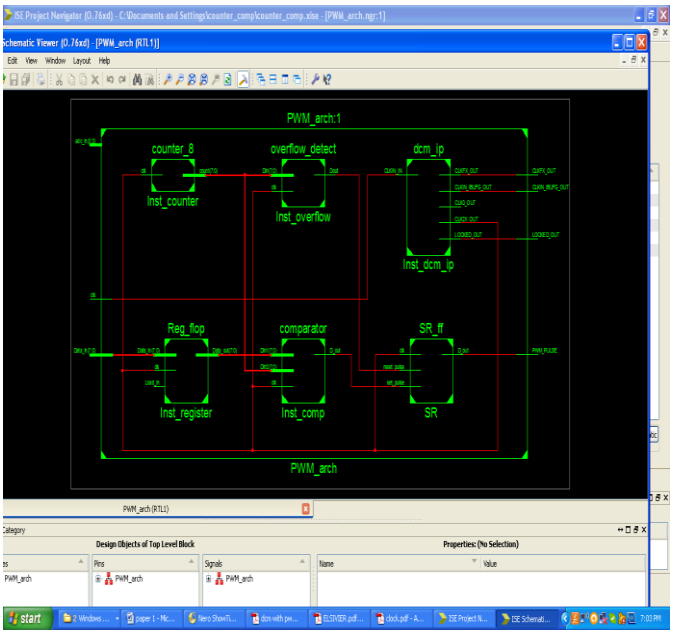

Figure 5: RTL Schematic of Binary Counter Based DPWM Architecture

Binary counter based DPWM architecture[3] is designed with eight bit binary counter and eight bit register which stores the duty cycle value. Binary counter based DPWM architecture utilizes the DLL clocking capability of FPGA. Input clock frequency 12.5 is multiplied by two (Clk2X) to yield the clock frequency of 25MHZ.When the clock input is given to the binary counter, it starts counting and comparator checks the value of counter with the data in the register when the counter

value matches the register value, it sets the SR flipflop to high state, overflow detector detects the overflow signal from counter and it resets the flip flop. The output of SR flipflop gives the PWM pulse.

For instance if the register value is 10000100, the counter starts counting from 00000000 and when it reaches the value 10000100 the comparator output will be 1 which sets the SR flipflop and when counter value overflows the overflow detector will reset the flipflop. This gives the PWM pulse with duty cycle of 48%. The duty cycle value of PWM pulse can be changed by changing the data present in the register.

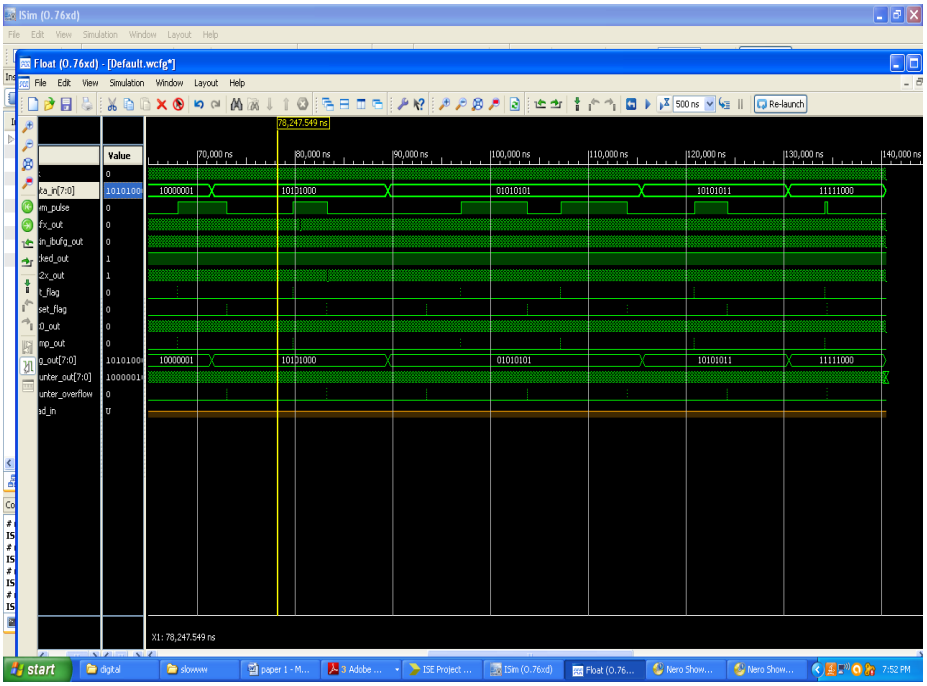

Figure 6: Simulation Waveforms for Binary counter based DPWM architecture with Variable Duty Cycle PWM pulses.

Gray Counter Based DPWM Architecture

Proposed gray counter based DPWM architecture is designed with VHDL. Behavioral simulations are obtained and Synthesized with Xilinx 13.3.Proposed Method is implemented in low cost SPARTAN 3A.The experimental results are obtained for external clock frequency of 12.5 MHZ.

When the clock pulse is given the gray counter starts counting from 0000 to 1000 at first (D_0) LSB bit is made high in one hot encoder and it continues till MSB bit (D_{15}) is made high. When the D_{15} bit set to high it sets the SR flip flop and in next clock pulse all the bits of one hot encoder resets to zero. In next clock pulse counter starts counting from 0000 to 1000 and it again sets the D_0 LSB bit in one hot encoder to high state and it continues till the particular bit (D_0-D_{14}) in one hot encoder set high. When particular bit set to high it resets the flipflop. This set and reset condition of flipflop gives the desired PWM signal.

For instance when the control signal (adc) is 1000 the gray counter starts counting from 0000 to 1000 then the bits of one hot encoder (D_0 –D_{15}) one by one goes to high state. When D_{15} bit (1000000000000000) of one hot encoder set to high state it sets the SR flipflop. Again when gray counter starts counting from 0000 to 1000 and when one hot encoder D8 bit is high (0000000010000000) it resets the flipflop. This gives the PWM pulse of 55.1%

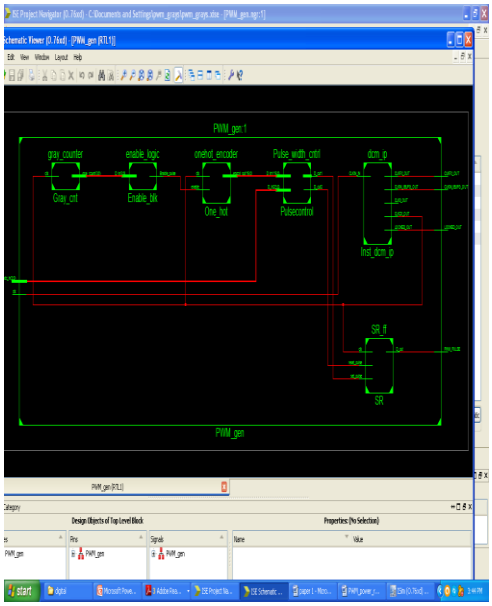

Figure 7: RTL Schematic of Proposed Gray Counter Based DPWM Architecture

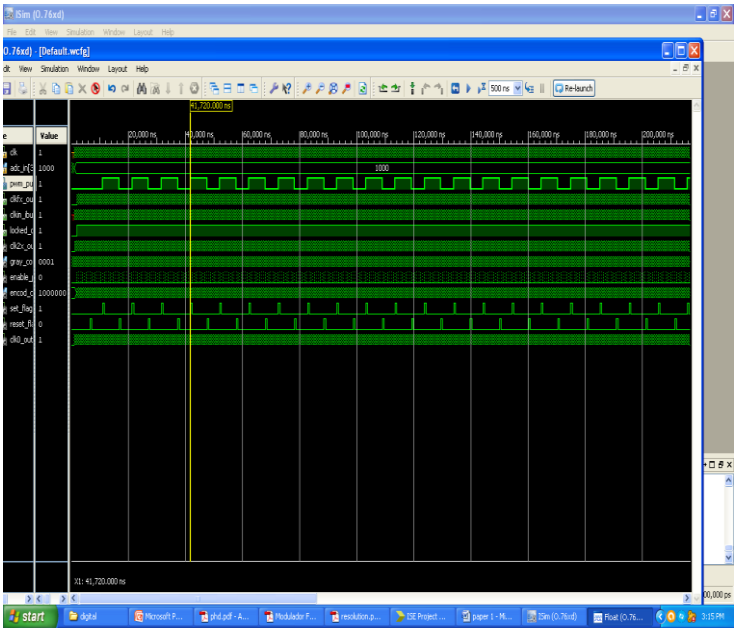

Figure 8: Simulation Waveform for duty cycle = 55.1% with adc:1000

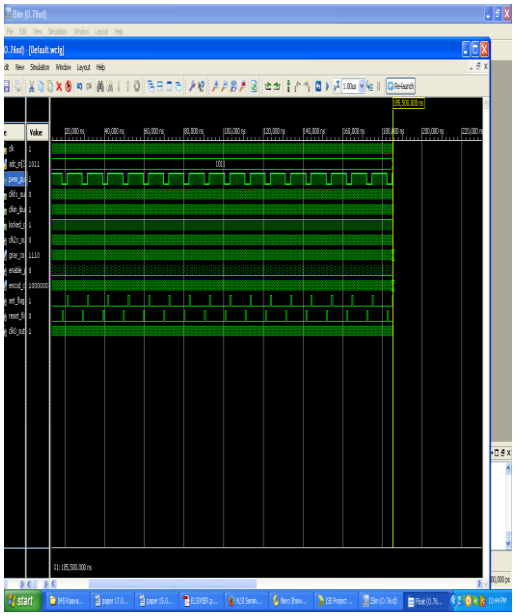

Figure 9: Simulation Waveform for duty cycle = 74.8.% with adc:1011

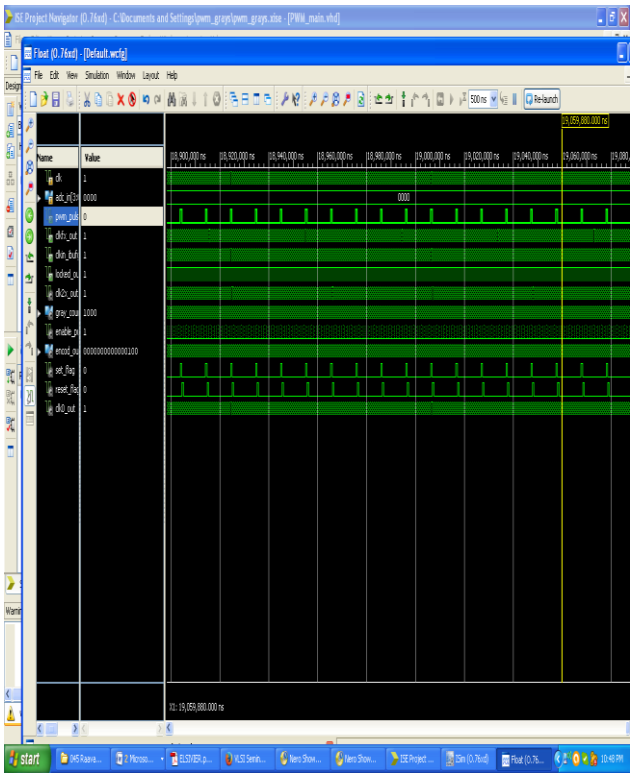

Figure 10: Simulation Waveform for duty cycle = 6.3% with adc:0000

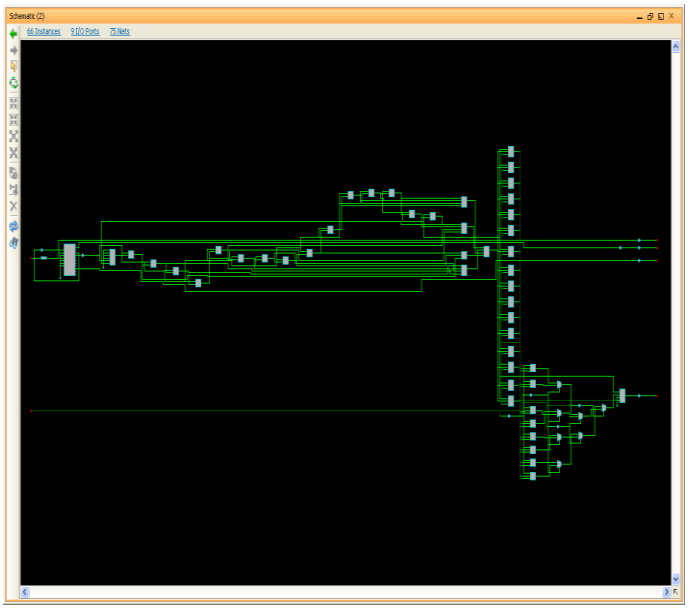

Figure 11: Netlist for the proposed Gray Counter Based PWM Architecture

Experimental Results

After Place and Route simulation the VHDL code is down loaded into low cost SPARTAN 3A. The input was given with 4 switches in the board and results are viewed in Digital storage Oscilloscope. The input clock frequency given is 12.5 MHZ and multiplied by two with DCM and power analysis is obtained for different input frequency to target FPGA and power analysis is done.

Table 1: Device Utilization Summary for Proposed Gray Counter Based DPWM Architecture

Logic Blocks	Used	Utilization	Utilization Percentage
Number of Slice Flip Flops	32	1,408	2%
Number of 4 Input LUT's	15	1,408	1%
Number of occupied Slices	26	704	3%
Number of Bonded IOB'S	9	144	6%

Power analysis report is obtained for both architectures with low cost SPARTAN 3A low speed (XC3S50A-4tq144), high speed (XC3S50A-5tq144) devices, and SPARTAN 3E low speed (XC3S100e-4tq144), high speed (XC3S100e-5tq144) devices.

Table 2: Power Analysis Report

Device	Frequency (MHZ)	Power Consumption(mW)	
		Proposed Gray Counter Based DPWM	Binary Counter Based DPWM
SPARTAN 3A (XC3S50A-4tq144)	6	14.79	14.86
	12.5	15.44	15.49
	15	15.69	15.86
	25	16.68	16.96
	50	19.16	19.72
	100	24.11	25.24
	150	29.07	30.76
	200	34.02	36.29
	250	38.98	41.81
	300	43.94	47.33
SPARTAN 3A (XC3S50A-5tq144)	6	14.80	14.88
	12.5	15.44	15.61
	15	15.69	15.61
	25	15.69	17.02
	50	19.16	19.84
	100	24.12	25.47
	150	29.08	31.11
	200	34.05	36.74
	250	39.01	42.38
	300	43.97	48.01
SPARTAN 3E (XC3S100e-4tq144)	6	14.79	14.82
	12.5	15.44	15.49
	15	15.67	15.75
	25	16.66	16.78
	50	19.11	19.36
	100	24.03	24.52
	150	28.94	29.68
	200	33.86	34.84
	250	38.77	40.00
	300	43.69	45.16
SPARTAN 3E (XC3S100e-5tq144)	6	14.79	14.81
	12.5	15.43	15.48
	15	15.67	15.74
	25	16.66	16.76
	50	19.11	19.32
	100	24.03	24.44
	150	28.94	29.57
	200	33.85	34.69
	250	38.77	39.82
	300	43.68	44.94

Proposed gray counter based DPWM architecture consumes less power as compared to binary counter based DPWM architecture. In proposed method as the

gray counter is used has negligible power consumption as compared to binary counter used in proposed DPWM architecture. The comparator used in binary counter based DPWM also contributes to significant amount power consumption.

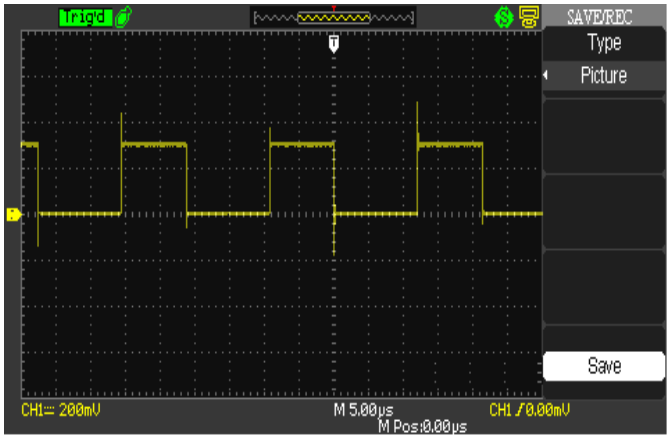

Figure 12: Digital storage Oscilloscope waveform for Duty cycle = 46.2%

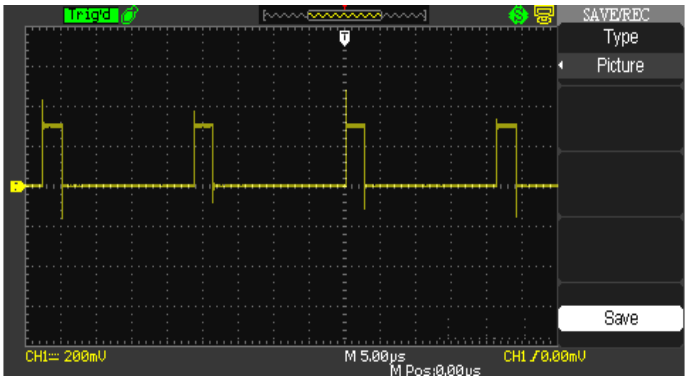

Figure 13: Digital storage Oscilloscope waveform for Duty cycle = 16 .1%

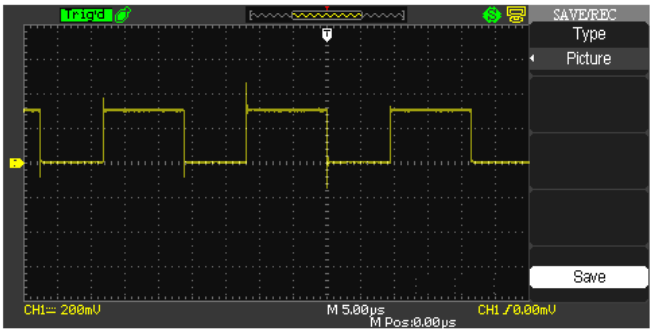

Figure 14: Digital storage Oscilloscope waveform for Duty cycle = 60.2%

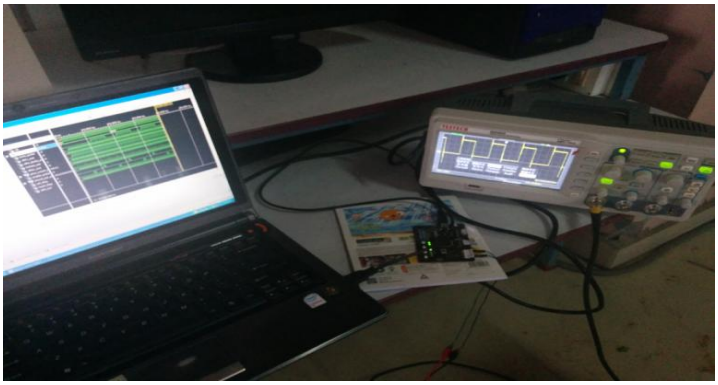

Figure 15: Experimental Setup for the Proposed Gray Counter Based Method

Conclusion

In this paper binary counter based DPWM architecture and gray counter based DPWM architecture is presented . The architectures are developed with VHDL language and PWM signals are generated . Time resolution of proposed work is 7.8125 ps. The proposed architecture is implemented in SPARTAN 3A FPGA which uses the DCM resource available in FPGA. The external clock frequency is multiplied with DCM and given to the system. This DPWM architecture can be used as digital controllers for high frequency switching converters. Power Analysis report is obtained for the both architectures with different target FPGA with different input clock frequency and tabulated. In this proposed method gray counter and one hot encoder circuit are used which reduces the power consumption as compared to binary counter based DPWM which uses binary counter and comparator to generate PWM pulse.

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