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Bridgeless Converter Based Switched Mode Power Supply With Power Quality Improvement

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Abstract

In this paper the power factor corrected (PFC) Switched Mode Power Supply (SMPS) based on bridgeless Buck-Boost converter topology with fuzzy logic control is proposed and is compared with the conventional SMPS. The multiple outputs of the SMPS are +12V,-12V,+5V,-5V for PC applications. To obtain nearly unity power factor and reduction in total harmonic distortion (THD) of input current, the SMPS with buck-boost converter based topology is designed to operate in discontinuous conduction mode (DCM). DCM operation gives added advantages of improved power factor and reduced switching losses and reduces the complexity of circuit operation. The presence of only two switches in the current conduction path during each switching cycle and the absence of diode bridge rectifier results in reduced conduction losses and an improved power factor, as compared to the conventional SMPS. Performance comparisons between the bridgeless buck-boost topology based PFC SMPS are performed based on MATLAB/Simulink simulations.

Keywords: Power factor correction; Total harmonic disortion; Discontinuous conduction mode; unity power factor.

Introduction

Input power supplies for electronic devices with power factor correction (PFC) techniques are important for all electronic equipments to match the harmonic current levels and standards, such as IEC 61000-3-2[1]. Almost all PFC techniques implies various boost converter topologies at their front end for power factor achievement. However, conventional SMPShas lower efficiency due to losses in diode bridge rectifier[2]. In conventional SMPS, current flows through diode bridgerectifier and the power switch during the switch on-time, and through bridge rectifier and the output diode during the switch off-time. During each switching cycle the current flows through four diodes and a power semiconductor switch. This results in generation of harmonic content in the system and degrades the efficiency and performance of the converter[3].

In diode bridge converter, the presence of power semi-conductor devices in the current flowing path produces the discontinuous current which results in high output ripple contents[4].The input current does not follow the source voltage, which will increase the total harmonic distortion (THD) and the reduction in power factor. Hence this will affect the quality of the power transferred.

In order to improve the efficiency of the power supplies, considerable research has been made over the development of improved bridgeless PFC circuit topology[5]. One of the popular research proved the efficiency of the bridgeless converter based SMPS is better than the diode bridge rectifier based SMPS, by eliminating the front end diode bridge rectifier circuit.

Proposed Bridgeless Buck-Boost Converters

This paper compares two types of PFC topologies with low conduction losses. The bridgeless converter provides several advantages such as protection against inrush current naturally, easy implementation of transformer isolation, less electromagnetic interference (EMI) and less ripples in input current with the DCM topology [6].

Fig. 1 shows the schematic diagram of bridgeless buck-boost converter based SMPS. Input supply is fed to the dual buck-boost converter through the LC filter circuit to remove the ripple content. The upper buck-boost converter, conducts for positive half cycle of the input ac supply through one high frequency switch S_p, inductor L_p and two diodes D_{p1} and D_{p2} Similarly, the lower buck-boost converter conducts for the negative half-cycle through one high frequency switch S_n, inductor L_n and two diodes D_{n1} and D_{n2}. Both inductors L_p and L_n of buck-boost converters are designed to operate in DCM to obtain inherent PFC at the input ac mains. The capacitors present in the input side of the half bridge VSI will act as the filter for the half bridge VSI circuit. The switch rating and the heat sink designs are estimated from the voltage and current stresses of the switches present in the buck-boost converter. The switches of the buck-boost converter are controlled by means of the closed loop control of its dc output voltage.

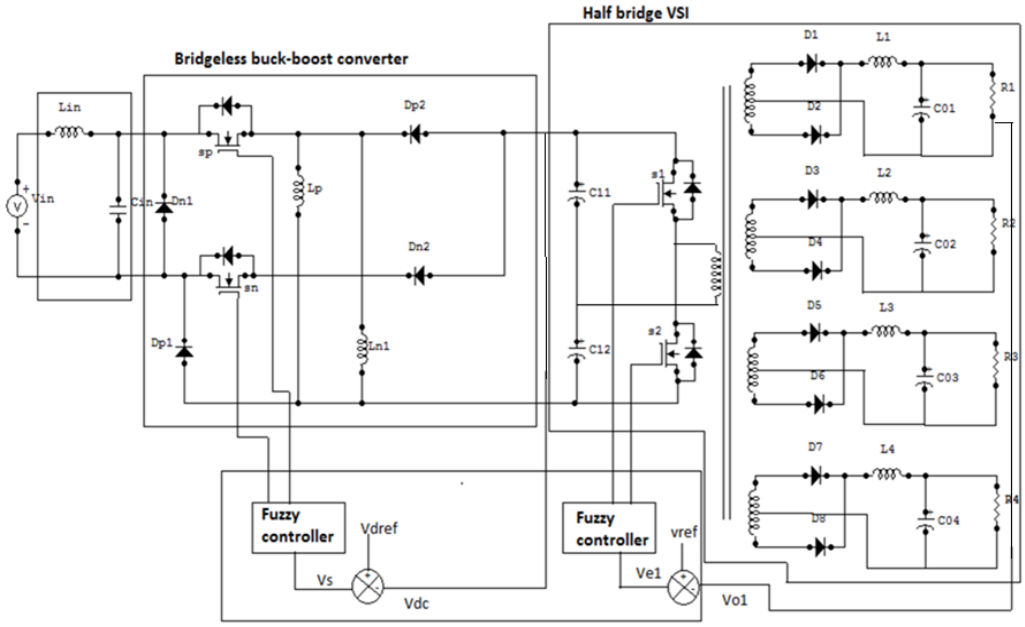

Figure 1: Bridgeless Buck-boost converter based SMPS

The regulated dc output voltage of buck-boost converter is fed to the half-bridge VSI for obtaining multiple dc voltages. The half-bridge VSI consists of two input capacitors C_{11} and C_{12}, two high frequency switches S_1 and S_2, one multiple output High Frequency Transformer (HFT). Centre tapped configuration of the HFT is having one primary winding and four secondary windings for reducing losses[7]. At the secondary side of the HFT, filter inductors L_1, L_2, L_3, L_4 and capacitors $C_{01}, C_{02}, C_{03}, C_{04}$ are connected to each winding to reduce the current and voltage ripples respectively. The dc output voltages are controlled by means of the closed loop control scheme. The highest rated dc output voltage is sensed and fedback for this purpose. Other three outputs are controlled by duty ratio control of half bridge VSI because a common core is connected for all the secondary windings of HFT with proper winding arrangements. A study has been made to reveal the effect of varying input voltages and loads[8].

Operating Principle of Bridgeless Converter Based Multiple Output SMPS

The multiple output SMPS based on back to back connected dual bridgeless buck-boost converter at the front end is fed by the single phase ac supply. This system consist of the buck-boost converter with a half-bridge VSI and multiple output HFT at the load end.

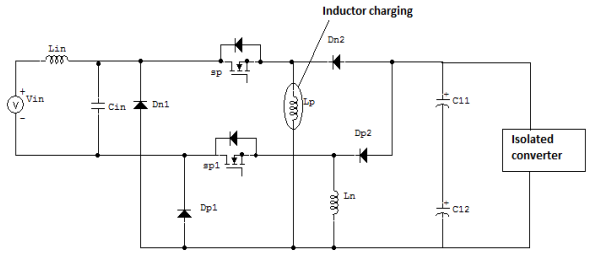

Figure 2a: Inductor charging when switch S_1 is on

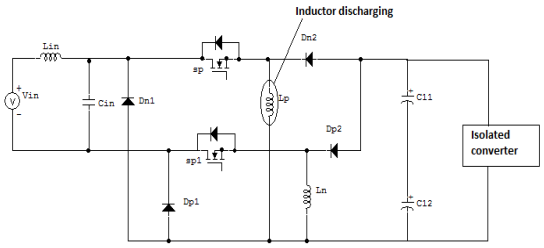

Figure 2b: Inductor discharging when switch S_1 is off

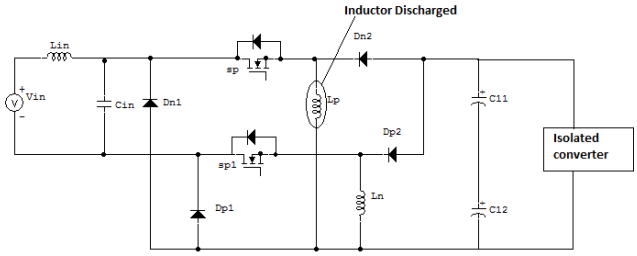

Figure 2c: Discontinuous Conduction Mode when switch S_1 is off

In order to get the high power factor and low input current THD, the buck-boost converters should be controlled correspondingly. To obtain the multiple output voltages and high frequency isolation, a half bridge VSI is connected at the output side.

A. Operation of Buck-Boost Converter

The upper half buck-boost converter is operated in positive half cycle of ac supply and the lower buck-boost converter is operated in negative half cycle of the ac supply. Operational diagram of the upper buck-boost converter is shown in the figure2.a, 2.b, 2.c, similarly for the negative half-cycle operation of the lower buck-boost converter. DCM operation has three states in its switching cycle. In the first state, the upper

switch S_p is on, inductor L_p storing energy from the input supply and the current across the inductor increases to the maximum value as shown in Fig. 2a. The current flow path in the input side is completed by the diode D_{p1}. In the second state, switch S_p is turned off and the energy stored in inductor L_p is transferred to the half bridge VSI, thus the maximum value of current stored in the inductor reaches to zero as shown in Fig. 2b. In the third state of one switching cycle, neither the switch nor the diode conducts and the inductor current is at zero ensuring DCM operation as shown in Fig. 2c. The same sequence of operation repeats in the next switching cycle. Similarly for negative half cycle of the input ac supply voltage, the lower buck-boost converter operates with the same sequence of operation.

B. Operation of Half Bridge VSI

The output of dual buck-boost converter is fed to half-bridge VSI for high frequency isolation, and for obtaining multiple output dc voltages. The operation of the half-bridge VSI in one switching cycle consists of four states. The second and fourth states are same and occur two times in each switching cycle. In the first state, the switch S1 is turned on, the input current flows through the primary winding of HFT by the capacitor C_{12}. Diodes D_2, D_4, D_6, D_8 start conducting and inductors connected with the windings start storing energy. Therefore, inductors currents $i_{L1}, i_{L2}, i_{L3}, i_{L4}$ increase and output filter capacitors $C_{01}, C_{02}, C_{03}, C_{04}$ discharge through the loads. In the second state, both the switches are turned off, and all secondary diodes $D_1 to D_8$ freewheel the stored energy until the voltage across the HFT becomes zero. Therefore, inductor currents $i_{L1}, i_{L2}, i_{L3}, i_{L4}$ start decreasing. In third state of the switching cycle, the second switch S_2 is turned on and the input current flows through capacitor C_{11} and the primary winding. Diodes D_1, D_3, D_5, D_7 in the secondary windings conduct and inductors L_1, L_2, L_3, L_4 start storing energy. When the energy stored in the inductors reach their maximum values, the switch is turned off. In the last state, all the secondary diodes start conducting which is similar to the second state.

Design of Proposed Bridgeless Converter Based Multiple Output SMPS

The component values are important to simulate the multiple output SMPS. The switching frequency is considered to be very high than the supply frequency (50Hz) for deriving the necessary equations by considering the switches and the diodes are ideal in nature[9].

A. Design of Buck-Boost Converter

The design of buck-boost converter is very important for ensuring the DCM operation. Hence the components are designed exactly to match the exact operation. The inductor for storing the energy and to be operated for DCM is expressed as

$$L_p = \frac{DTV_{avg}}{\Delta i_{LPon}} \tag{1}$$

D = duty cycle

i.e., $t = \frac{t_{on}}{T}$ where t_{on} is the 'on' time of the switch

T is the total period in one switching cycle,

Vavg is the average of single-phase ac input voltage across the input of the buck-boost converter.

In DCM operation, the inductor current ripple is considered as maximum and it must be equal to two times the input current[10].

$$\Delta i_{Lon} = 2 * I_{in} \tag{2}$$

By Substituting the value of inductor current ripple and can yield Lpmin as

$$L_{p\min} = \frac{DTV_{avg}}{2i_{in}} = \frac{0.2 * 50\mu S * 198V}{2 * 1.63A} = 607\mu H \tag{3}$$

For a deep DCM condition

$$L_p < \frac{L_{p\min}}{10}$$

B. Input Filter Design

L-C filter is essential to filter the higher order harmonics and is designed as follows. The maximum capacitance value is expressed as,

$$C_{in\max} = \frac{I_m \tan\theta}{\omega V m} = \frac{2.30A * 0.0174}{3114 * 311V} = 409nF \tag{4}$$

Where *Im*and *Vm*are the peak input ac current and ac voltage respectively.

The inductor for obtaining low harmonic distortion at the input side of ac mains is calculated as,

$$L_{in} = \frac{1}{4 * \pi^2 * f_c^2 * C_{in}} = \frac{1}{4 * (3.14)^2 * 5000KHz^2 * 330nF} = 3.07mH \tag{5}$$

Where *fc*is the cutoff frequency.

C. Design of Half-Bridge VSI

The input capacitors of the half-bridge VSI act as a low pass filter to eliminate the harmonics which is reflected due to the single phase ac mains[11].

Design of Input Capacitor:

The input capacitor is designed to eliminate the harmonics introduced due to the single phase ac mains. So, it is governed by the amount of the 100*Hz* (lowest harmonic) current flowing in the capacitor. For maintaining PFC operation, the input current and voltage should be in phase. Therefore, the input power Pin [2] is,

$$P_{in} = \sqrt{2} V_{in} \sin\omega t * \sqrt{2} I_{in} \sin\omega t = V_{in} I_{in} (1 - \cos 2\omega t) \tag{6}$$

where the latter term corresponds to the 100*Hz* ripple which is reflected on the input capacitors of the half bridge VSI. It is expressed as,

$$i_c(t) = -\frac{V_{in} I_{in}}{V_{dc}} \cos 2\omega t \tag{7}$$

where, ic(t) is the total current flowing in the capacitors C11 and C12.The output voltage ripple corresponding to these capacitors' current is given by [2],

$$\Delta V_{dc} = \frac{1}{C}\int i_c(t)dt = -\frac{I_{dc}}{2\omega C} \sin 2\omega t \tag{8}$$

Sin(ωt) is taken as 1 for the maximum value of voltage ripple at the capacitor. Hence,

$$C = \frac{I_{dc}}{2\omega \Delta V_{dc}} \tag{9}$$

Therefore, the capacitors C11 and C12 are estimated as,

$$\frac{C_{11}}{2} = \frac{C_{12}}{2} = \frac{I_{dc}}{2\omega \Delta V_{dc}} = \frac{1.2A}{2*314*6V} = 0.63mF \tag{10}$$

Two equal valued input capacitors C11 and C12 are calculated as 0.63mF for a ω of 314 rad/sec, ΔVo being 6V (2% of Vo) and output current of the buck-boost converter being 1.2A.

Permissible current ripple is assumed to be 2%.

Design of Turns Ratio:

In steady state condition, the change in output inductor current iL1 during switch on and off conditions is equal to zero[12] and it is expressed as,

$$\frac{T_h(0.5nV_{dc} - V_{01})D_h}{L_1} + \frac{T_h V_{01}(0.5 - D_h)}{L_1} = 0 \tag{11}$$

where Vo1 is the sensed dc output voltage, Dh is the duty cycle of half-bridge VSI and Th is one switching time.

Solving (8) for calculating turns ratio,

$$n = \frac{V_{01}}{D_d V_{dc}} = \frac{12V}{0.4*300V} = 0.1 \tag{12}$$

Turns ratio from (13) is calculated as 0.1 for an output dc voltage of +12V and for a duty cycle Dh of 0.4.These component values are used in the modeling of the proposed multiple output computer SMPS. These values and the ones used in the experimental prototype are tabulated in Table I[8].

Table 1: Parameters of Bridgeless converter basedmultiple output SMPS

COMPONENT CONNECTED	SELECTED VALUE
input inductors L_p and L_n	60 μ H
filter capacitor C_{in}	330nF
filter inductor L_{in}	2.5 mH
capacitor C_{11} and C_{12}	660 μ F

Control of Proposed Bridgeless Converter Based Multiple Output SMPS

The control of the bridgeless converter based SMPS is entirely depends on the FUZZY logic controller. Here, the bridgeless buck-boost converter utilizes voltage follower approach and the half bridge VSI utilizes average current control scheme. In fuzzy logic controller, 7 membership functions are used and the corresponding rules(7*7) are created accordingly. The desired output voltage based on their output ranges in membership functions will be fedback to the system.

A. Control of front end converter:

Generated PWM is given to the bridgeless converter switches based on polarity of the supply accordingly. In this technique the voltage error is determined[13] i.e., the difference between the reference voltage (V_{dcref}) and the sensed dc output voltage (V_{dc}) is fedback to a fuzzy logic controller. The error in voltage signal will be

$$V_e(n) = V_{dcref}(n) - V_{dc}(n)$$

Thus the error signal will be given to the switches of the controller in bridgeless converter and the output will be maintained constant.

B. Control of Half Bridge VSI:

The output voltage of the half bridge VSI can be controlled by means of average current control scheme. Here the highest rated winding output voltage is sensed (V_{01}) and examined with the constant reference value (V_{01ref}). The voltage error signal (V_{01}) is fedback to the fuzzy logic controller-2 and the output signal is compared with the saw tooth signal as a reference signal to generate PWM switching signals to control the switches for maintaining the output voltage constant.

Fuzzy Logic Controller

Fuzzification:

In Fuzzification, the input variable (crisp variables) error signal and change in error signal are converted into fuzzy variables. This controller uses the linguistics labels as

NB,NM,NS,ZE,PS,PM,PB. All the inputs and outputs must contain the membership function with all these labels[14].

Knowledge base and inference stage:
Knowledge base includes the process of explaining the rules which is represented in the form of IF-THEN rules statements representing the relation between input and output variables in membership functions.

Defuzzification:
In this stage various methods can be used to generate the fuzzy sets value for the outputs of fuzzy variable.

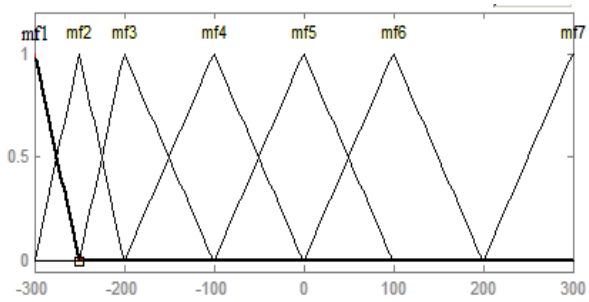

Figure 3a: Membership function for input fuzzy variable of fuzzy controller-1

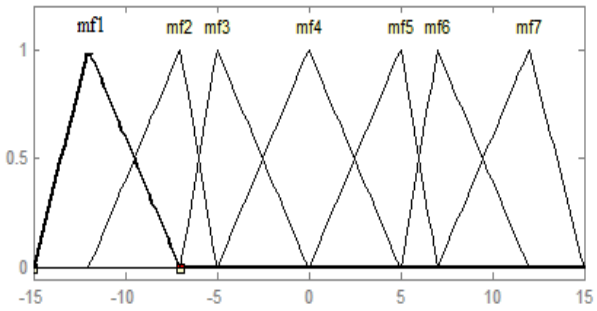

Figure 3b: Membership function for input fuzzy variable of fuzzy controller-2

Table 2: Fuzzy Controller Rule Base

e(pu) / ce(pu)	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	Z
NM	NB	NB	NB	NM	NS	Z	PS
NS	NB	NB	NM	NS	Z	PS	PM
ZE	NB	NM	NS	Z	PS	PM	PB
PS	NM	NS	Z	PS	PM	PB	PB
PM	NS	Z	PS	PM	PB	PB	PB
PB	Z	PS	PM	PB	PB	PB	PB

Simulation and Experimental Results

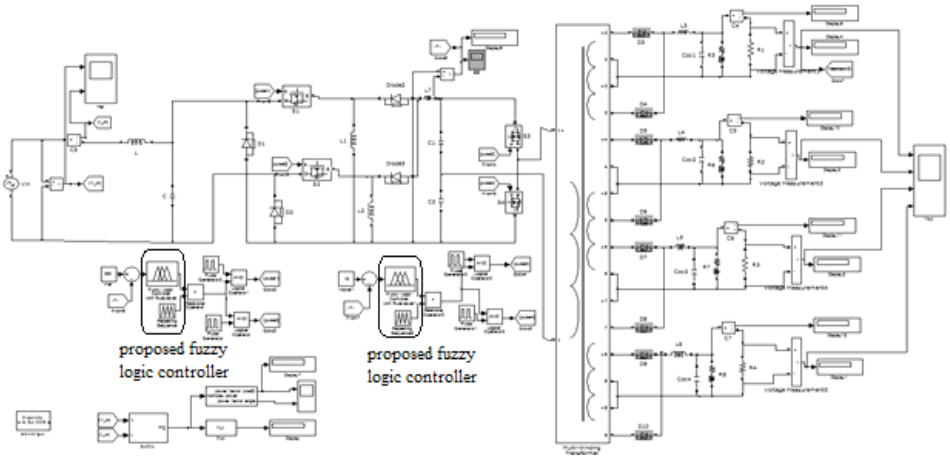

Figure 4a: Simulation diagram of bridgeless buck-boostfuzzy logicbased smps

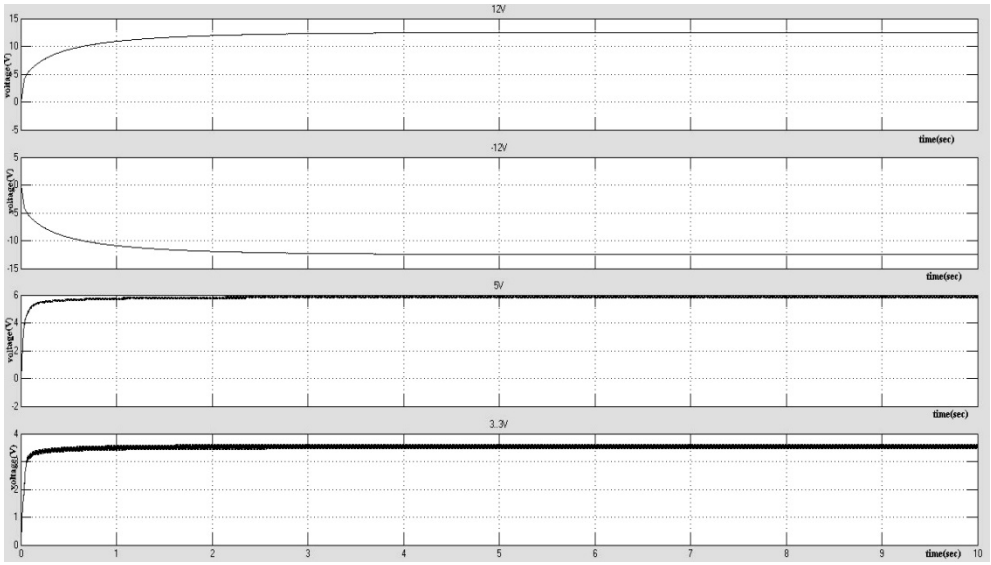

Figure 4b: Waveform of bridgeless buck-boost fuzzy logicbased smps

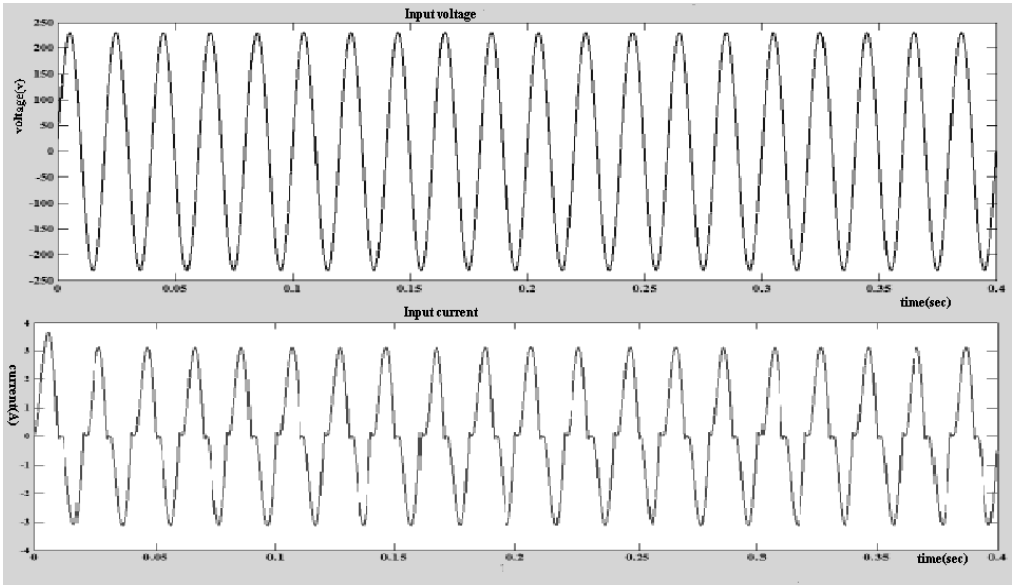

Figure 4c: Input voltage and Input current waveform of proposed bridgeless buck-boost fuzzy logic based smps

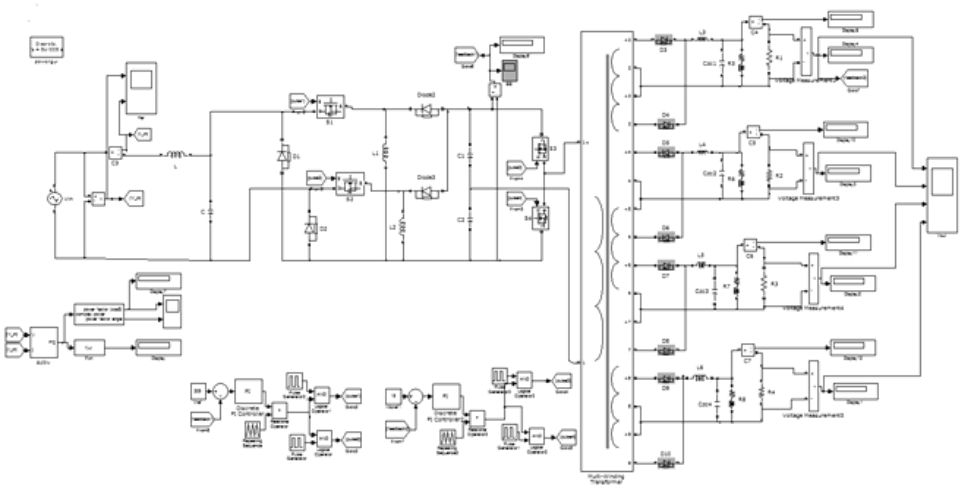

Figure 5a: Simulation diagram of conventional converter based SMPS

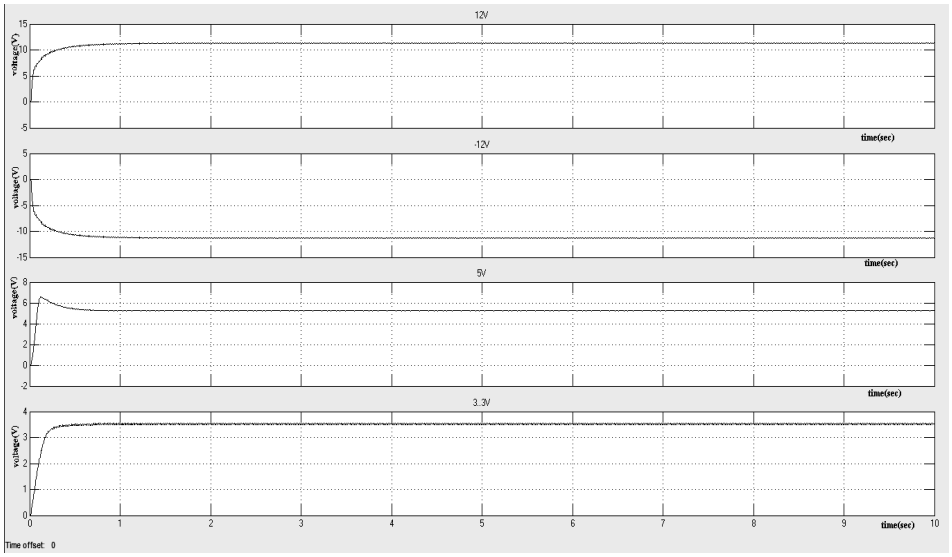

Figure 5b: Output waveform of conventional converter based SMPS

Figure 5c: Input voltage and Input current of conventional converter based SMPS

Table 3: Power quality indices of bridgeless converter based multiple output SMPS

INPUT VOLTAGE(RMS)	DPF	DF	PF	i_{in}(A)	i_{inTHD}(%)
180V	1	0.9991	0.9991	7.616	4.65
230V	1	0.9986	0.9986	4.596	5.11
260V	1	0.9980	0.9980	4.623	6.29

Comparison of Conventional And Proposed Bridgeless Converter Based SMPS

The performance of proposed bridgeless SMPS is compared with the existing conventional SMPS. Here the comparison is based on i) total number of components present in the circuit i.e., high frequency switches, diodes, inductors and capacitors. ii) During a half cycle, the total number of components is to be conducted. Table IV shows the comparison results among various bridgeless converter based SMPS.

Total harmonic distortion analysis of input current for conventional controller based SMPS and proposed bridgeless buck-boost converter based on fuzzy logic control based SMPS are shown below.

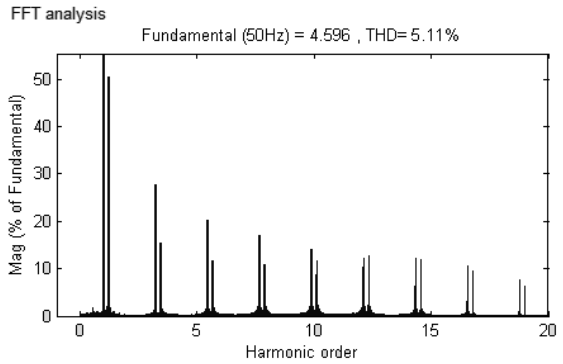

Figure 6a: THD analysis of proposed SMPS

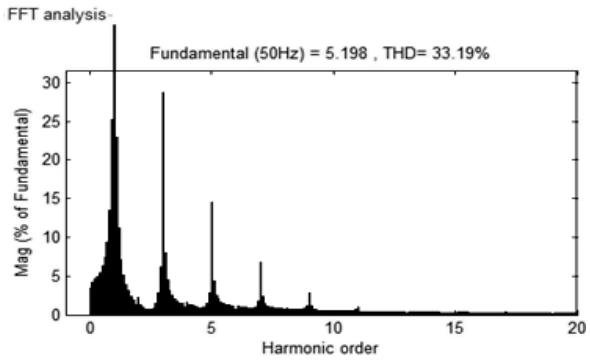

Figure 6b: THD analysis of conventional SMPS

Table 4: Comparison of Proposed PFC Converter With Other PFC Converters

Configuration	Components in conduction				Half cycle conduction
	Diode	Capacitor	Inductor	Switch	
Bridgeless SEPIC [7]	2	4	3	2	10
Conventional Bridgeless Buck-boost converter [8]	4	3	1	3	8
Bridgeless Cuk converter [12]	2	3	3	2	7
Proposed Bridgeless-Buck boost converter based SMPS	4	2	2	2	6

Conclusion

The multiple output SMPS based on bridgeless buck-boost converter has been simulated and the multiple outputs +12V, -12V, +5V, +3.3V are obtained. The output voltage of the buck-boost converter has been maintained constant to achieve the inherent power factor and improvement in the power quality. The performance of the multiple output SMPS is satisfactory when the input voltage is varied and at the

different loads are applied and the changes are within the acceptable limits of IEC 6l000-3-2. It is evident from the above comparison that the performance of proposed converter is better and the power factor gets improved when the hardware prototype is implemented.

Appendix

Nominal input ac mains voltage 220V,50Hz.

Half bridge VSI input voltage 300V.

Multiple dc output voltages and current 12V/0.102A, 5V/1.6A, 3.3V/1.1A, -12V/0.23A

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