

A Low Power Hybrid Clock Gating Technique For High Frequency Applications

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Abstract

Proliferation of high speed applications is leading towards increase in the dynamic power consumption per chip. Clock gating is found to be the most effective technique by which overall power consumptions can be reduced without sacrificing the performance and functionality of the chip. Look Ahead Clock Gating (LACG) is one of the new approaches in this area which overcomes the drawback of small time window of other conventional techniques. In LACG, the main idea is to calculate the clock enable signal one cycle ahead of time, based on present cycle data of other flip-flops on which it depends. However there may be cases when this technique will block the output of logic block when they should be propagated to the output. Also another drawback of this technique is that it consumes more power. So in the proposed hybrid clock gating technique the sequential and combinational blocks have been separated for overcoming the problem. Also lesser overhead of the gating circuitry has been used which leads to power reduction. An average power saving of 36% can be achieved using the hybrid clock gating technique. The proposed design has been validated & implemented using Cadence Virtuoso 90 nm CMOS technology.

Keywords: clock gating, low power, hybrid clock gating, high speed.

Introduction

The new generation of semiconductor processing technology is stepping towards the scaling of effective channel length of integrated circuits and at the same time the device density, speed and complexity on a semiconductor chip is increasing. The need

of portable consumer electronics is craving path for smaller, lighter and more durable electronic products which indirectly translates to low power requirements. Due to high frequency and load, clock is one of the major sources of power dissipation in digital circuits. Hence there is an immense need to reduce the unnecessary power consumption. As it is found that in high speed applications the clock switches at a very faster rate as compared to the incoming data. It has been observed that clock distribution can take up to 40% of the total power dissipation of high performance systems. Thus to reduce this power dissipation various gating techniques have been introduced.

When a clock signal of a functional module is not required for an extended period we can use a gating function to turn off the clock feeding the module. Thus masking the undesired switching of clock signals we can save an appreciable amount of power dissipation in a system. The basic idea of clock gating is to reduce the dynamic power consumption [1] of Flip-Flops (FFs) by gating the switching of unnecessary clock signals without violating the functional correctness as the FFs are the major source of power dissipation in a digital system. Clock Gating [2] thus leads to a considerable amount of power reduction of overall system by generating proper control signals. One of the major concern in designing a clock gating logic circuit design [3] is that the power dissipation due to the extra circuitry should not outweigh the power saving. Different methods have been described for gating at circuit level. It can be done using gates such as AND and OR gates, Latches and FFs.

XOR and AND gates are the two most widely used logic element for getting the clock enable signal. A XOR gate can be used to compare present and previous data and if both are same we can disable the clock from making transition in the next clock cycle by ANDing the output of XOR gate and the clock and feeding its output as input clock of a FF [4]. This is known as adaptive clock gating technique. Thus just using a XOR gate and an AND gate we can find out the clock gating signal. As signals take some time to settle, so this circuit may however violate the functionality sometimes. So Auto Gated Clock Gating (AGCG) technique came into picture which uses master-slave FF and uses the XOR gate in the output of FF's internal master rather than D, as it gives guarantee to be stable when the slave is transparent. AGCG technique is shown in fig.1. It consists of a master slave FF where the XOR gate is inserted between the output of master and output of slave.

The output of XOR gate is then fed at the input of AND gate which is then ANDed with the incoming clock signal. The output of AND gate is the clock enable signal which triggers the slave at the rising edge of the clock as here we have taken the positive edge triggered M-S FF. This gating technique is very simple to implement but one of its drawback is that it doesn't lead to much power saving.

Another variant in the clock gating technique is the synthesis-based clock gating technique [5]. It is the most popular method employed by Electronic Design Automation (EDA) tools. It is based on the various heuristics and algorithms for clock gating, but its drawbacks is that most of the clock switching activity has been left redundant [6] ,

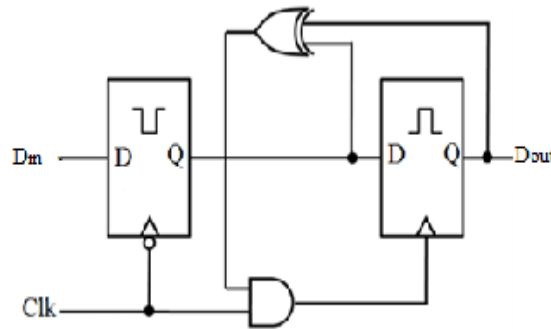


Figure 1: Logic diagram of auto gated FF

which leads to undesirable power dissipation. Data-Driven clock gating technique solved this problem. In the data-driven clock gating technique the clock enable signals are derived from logic synthesis along-with manual definitions [2]. One of the common drawbacks of data-driven clock gating and AGFF was that, it has a very small time-window for proper functioning of the gating circuitry [7]. Thus there was a need to increase the time-window.

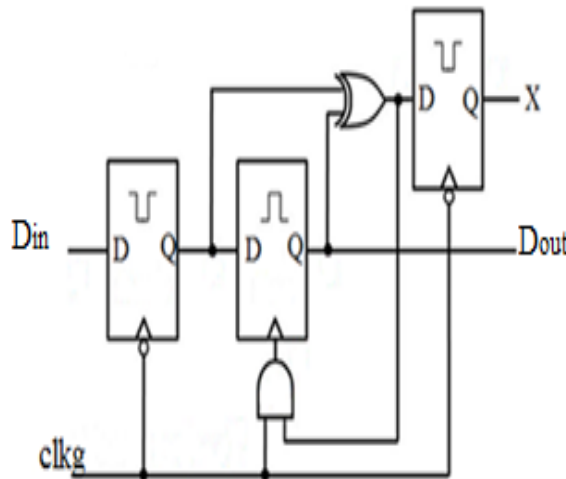


Figure 2: Logic diagram of enhanced Auto-Gated FF

The LACG technique [8] overcomes this drawback by calculating the clock gating signal one cycle ahead of time based on the present cycle data. The figure of LACG is shown in fig. 3. It consist of an enhanced auto gated FF as shown in fig.2. FFs with D as input and Q and X as the output is the symbol for enhanced auto gated FF which has been used to design the LACG circuit, shown below in Fig.3. The drawback of this technique is that, this technique has not

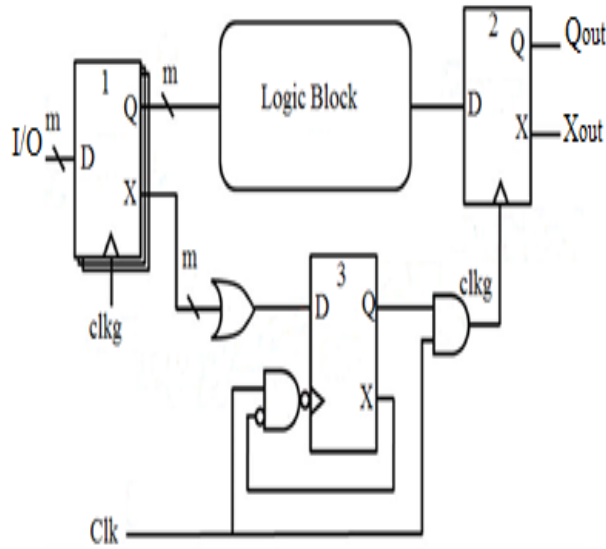


Figure 3: Implementation of Look Ahead Clock Gating technique

considered the case when the output of logic block has to be propagated to the output but since the target FF has been gated in that clock cycle depending on the present data. Since, in case of sequential circuits in which the circuit may take more than one clock cycle to get the output. In those cases if the target FF has been gated based on the present cycles of data then it may gate the output of the sequential logic block output by gating the target FFs. Hence, it will alter the functionality of the system. Also in LACG the overhead is more due to the involved gating circuitry. Here only the target FFs are grouped to reduce this overhead. In the proposed design to achieve power saving further, along-with the target FFs source FFs are also grouped. The rest of the paper discusses the design methodology of hybrid clock gating technique, its implementation using three different circuits with variation in the number of FFs and the power analysis.

Proposed Hybrid Clock Gating Methodology

In the proposed design the logic block has been taken two separate blocks one for sequential logic block in which the clock gating signals can be calculated based on the input and output of the logic block and the other, for the combinational logic block in which clock gating signals can be calculated based on the present cycle of data as shown in Fig.4(a) and 4(b) respectively.

In Fig. 4(a) positive edge triggered master-slave D-FFs have been used for sequential logic block. A master changes its state when clock is low and slave changes its state when clock is high. The purpose of master slave FF is to protect a FF's output from inadvertent changes caused by glitches at the input [9]. The input and output of m D-FFs is fed to the input of XOR gate. The ' m ' number of output of XOR gates are then fed to the input of the OR gate. As the output of OR gate reduces

to zero after clock to output contamination delay [10] hence is then latched using a D-latch. The output of the latch is then given to the input of an AND gate which is then, ANDed with the incoming clock signal to provide the clock to the master slave D-FFs. Thus this design is capable of gating the clock signals of source as well as target FFs without disturbing the functionality of the circuits at all.

In the Fig. 4(b) the combinational logic block can be implemented using the LACG technique [8] as it provides greater time window. In LACG technique the clock enabling signals of the other FFs in the system has been calculated based on the XOR output. The output of the XOR gate is used to get the clock enable signal of this gated FF in-order to reduce the extra overhead due to this FF. The output of this FF is then used to produce the clock enabling signal. Thus in this technique the clock enable signals has been calculated based on the present cycle of data. However, LACG provides greater time window but for the cases where power saving is of more concern and the time window is sufficient to get the clock gating we can use the combinational block also with clock gating technique of Fig. 4 (a). As the gating circuitry consists of FF, XOR gate, OR gate, AND gates and latch so the overhead will increase with the increase in the number of logic blocks. Thus to reduce this overhead, clustering [11] of the input as well as the output FFs can be done. Hence by doing so with one overhead of gater several signals can be gated and power reduction can be achieved.

In order to show the variation in power consumption and percentage power saving in logic circuits with different number of FFs, three distinct logic blocks namely counter, shift register and Pseudo Random Number Generator (PRNG) circuits have been designed and implemented using Hybrid clock gating technique.

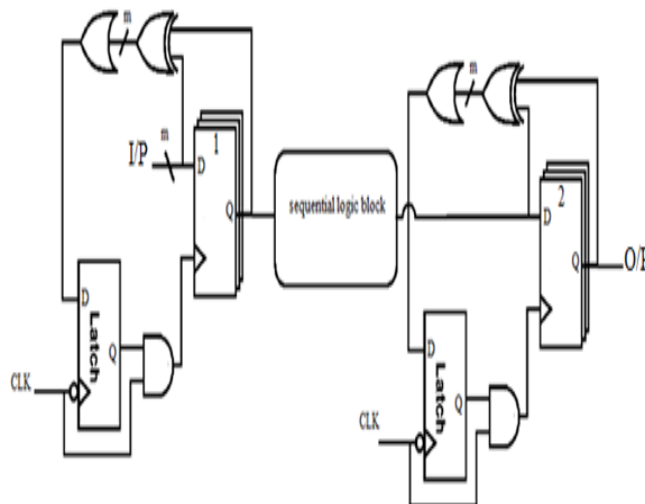


Figure 4(a): Proposed design for sequential logic block.

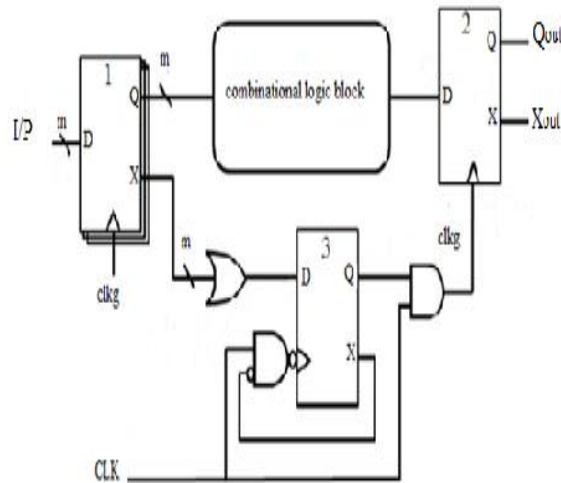


Figure 4(b): Proposed design for combinational logic block

Result

The design and implementation of 5-bit synchronous up-counter , a 10-bit Serial In-Serial Out (SISO) shift register and a 20-bit PRNG using Cadence Virtuoso using 90nm CMOS technology have been shown in the Fig. (5) - (10) given below.

A. Conventional 4-bit Synchronous Up-Counter

The synchronous 4-bit up counter with four master slave [12] FFs, 4 XOR gates and 3 AND gates has been designed as shown in Fig.5 and the corresponding waveform is shown in Fig.(6) . As, this is a synchronous counter hence same clock pulses have been given to each D-FF. Thus, with every clock pulse the counter counts one step up from 0000 to 1111 and then starts from 0000 again.

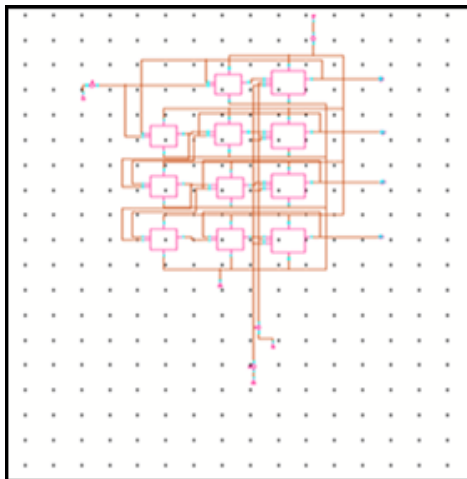


Figure 5: Schematic of 4-bit synchronous up counter

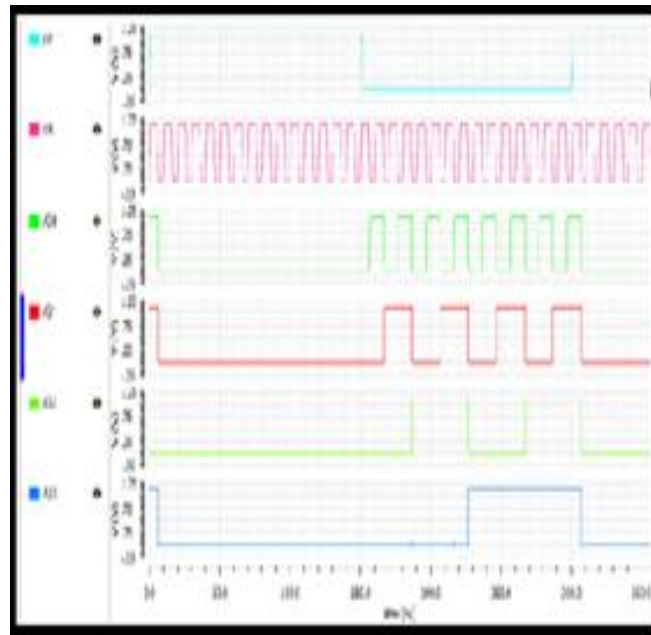


Figure 6: Waveform of 4-bit synchronous up counter

B. 10-Bit Shift Register

SISO Shift registers are sequential logic circuit, used mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. Each stage in a shift register represents one bit of storage capacity. Therefore the number of stages in a register determines its storage capacity. The SISO shift register accepts data serially, one bit at a time on a single line. It produces the stored information on its output also in serial form. Schematic of a basic 10-bit shift register and its waveform is shown in Fig. (7) and Fig. (8) respectively.

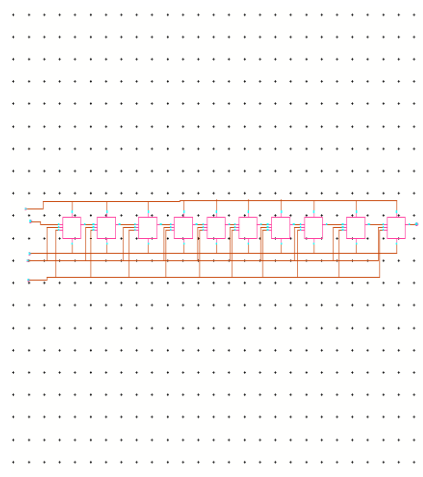


Figure 7: Schematic of 10-bit serial in serial out shift register.

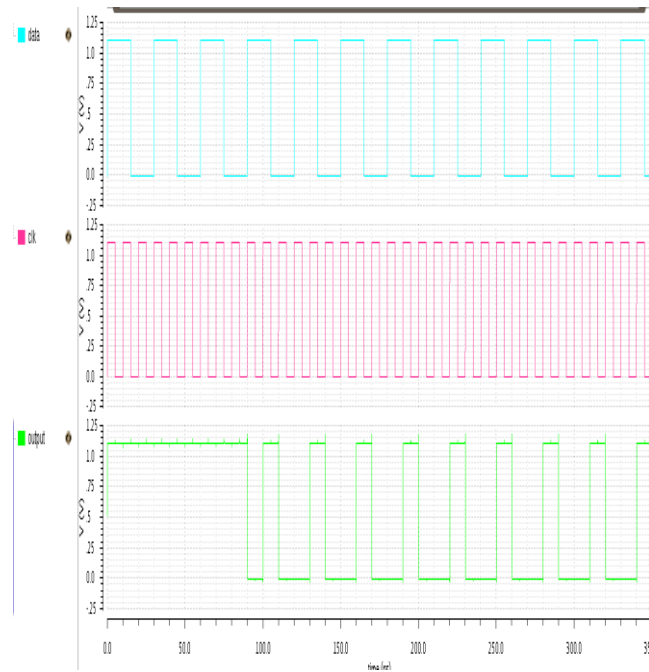


Figure 8: Waveform of 10-bit serial in serial out shift register

C. 20-Bit Pseudo Random Number Generator (PRNG)

A PRNG can be started from an arbitrary initial state using a seed state. It will always produce the same sequence when initialized with that state. These are extensively used in art, games, analysis, gambling, cryptography, testing and many other applications. The schematic diagram of PRNG with 20 flip-flops and its waveform is shown in Fig.9 and Fig. 10 respectively.

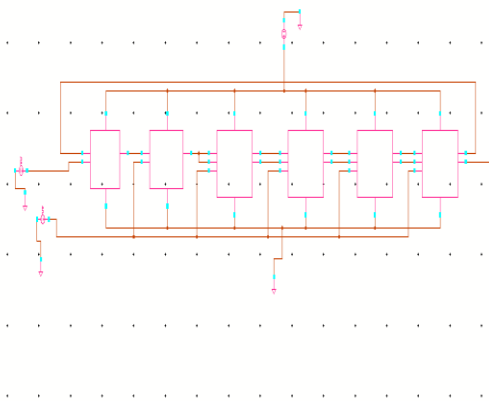


Figure 9: Schematic of 20-Bit PRNG

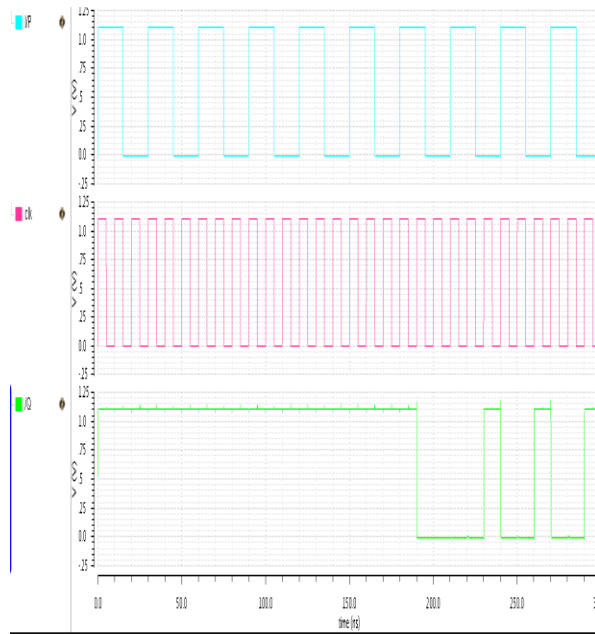


Figure 10: Waveform of 20-bit PRNG

Power Analysis

The power analysis is shown in Table I with the variation in the number of FFs. Here the power comparison has been made among the logic circuits with the clock gating technique and without the clock gating technique along-with the percentage in power saving due to the use of Hybrid clock gating technique. This table is then expressed in the form of a bar graph as shown in Fig. (10) for clear comparison.

Table 1: Power Analysis Of Logic Blocks Using Hybrid Clock Gating Technique

Logic Circuit	FFs count	Power Consumption (Without clock gating) (μW)	Power Consumption (With clock gating) (μW)	% Power Saving
Counter	5	5.12	4.02	21
Shift-Register	10	12	8.014	33.22
PRNG	20	27.7	13.03	53

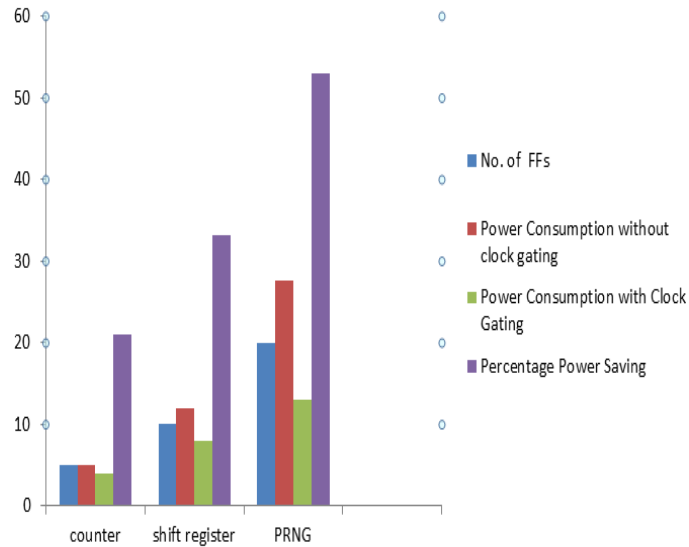


Figure 12: Bar graph for the comparison among three different logic blocks

Conclusion

The power analysis comparison in table.I concludes that using the proposed Hybrid Clock Gating technique the power consumption reduces as the number of FFs in a logic circuit increases . This is due to less overhead of the gating circuitry as compared to the conventional logic circuit. The results show that on an average a power reduction of 36 - 40% has been achieved using proposed Hybrid Clock Gating technique.

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