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Ultra Low Power Design Using Average 8t Differential Sensing Sub-Threshold Sram

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Abstract

Low voltage and Low power SRAM (Static Random Access Memory) design is critical in power concuss devices. To reduce the power in the concuss devices, a new average 8T write /read decoupled SRAM architecture is proposed .The proposed architecture deals with data independent leakage concept and read port that provides robust and faster read operation and reduce concern in half selected cell..The average 8T decoupled SRAM is compared with conventional 8T and simulation results of the proposed provides power consumption than the proposed.

Index Terms: average 8T decoupled SRAM, concuss devices, sub threshold.

Introduction

Static Random Access Memory (SRAM) continues to be one of the most fundamental and vitally important memory technologies today. Leakage power [1, 2] is a high priority consideration due to feature scaling in high performance processor design. In current processors, the leakage power of cache was a major source of power dissipation because cache occupies more than 50% of the chip area. Low Power and high-stability have been the main topic of SRAM designs.

The conventional transistor (6T, 8T) consumes more power. Approximately for 1 bit it consumes power in range 3.7677e-006 watts. Data independent leakage also plays an

important part in the conventional transistors .The scaling of gate length increases device leakage ascending So, the conventional transistors consume more power .To overcome this issue an Average 8T differential read write sub-threshold sensing SRAM is proposed.

High data activity leads large power consumption and delay in the read port memory. A new average 8T differential sensing sub threshold SRAM is proposed to improve speed and low power consumption in memory. Conventional transistors attains high leakage current[3] and large power consumption, so ARWD is used to overcome these problems. Comparison between conventional 8T and average 8T shows the low power consumption in the proposed.

The average-8T holds four bits through four back global read bit lines (RBL and RBLB*)*. This new write/read-decoupled (WRD) technique allows complete isolation of these four bits. In the idle state, when neither a write nor a read operation occurs on a block, the local bit lines are disabled. Block mask transistors are introduced to assure that LBL and LBLB are low when the block is not selected and their leakage is minimize.

A new read decoupling technique that decouples more than one bit at both Q and QB sides is proposed to improve read robustness. The access transistor is used as a selection switch among data bits.[4] This technique brings interesting features. As during a read operation there is no leakage in current, and the retained data turns one of the read-decoupling pair transistors on and discharges the other (RBL or RBLB*)*.[6] Therefore the leakage of the unselected blocks is not only minimized but also independent of the data stored in that block A write operation, is performed by selecting the intended block and bit in the same way as a read. [6]

Problem Analysis

A distinct difference between the proposed technique and the conventional 8T cell is data-independent leakage in the read bit line which is achieved by newly introduced block mask transistor. The second difference is the write decoupling transistors which minimize the write disturbance in the half-selected cells. The final is the 8T cell is the differential read port in the proposed architecture. The area is reduced by using decoupling transistor in the proposed method.

Results and Discussions

This section deals with the analysis of A-8T WRD SRAM for 4bits and 16 bits. Simulation results are based on the power consumption.

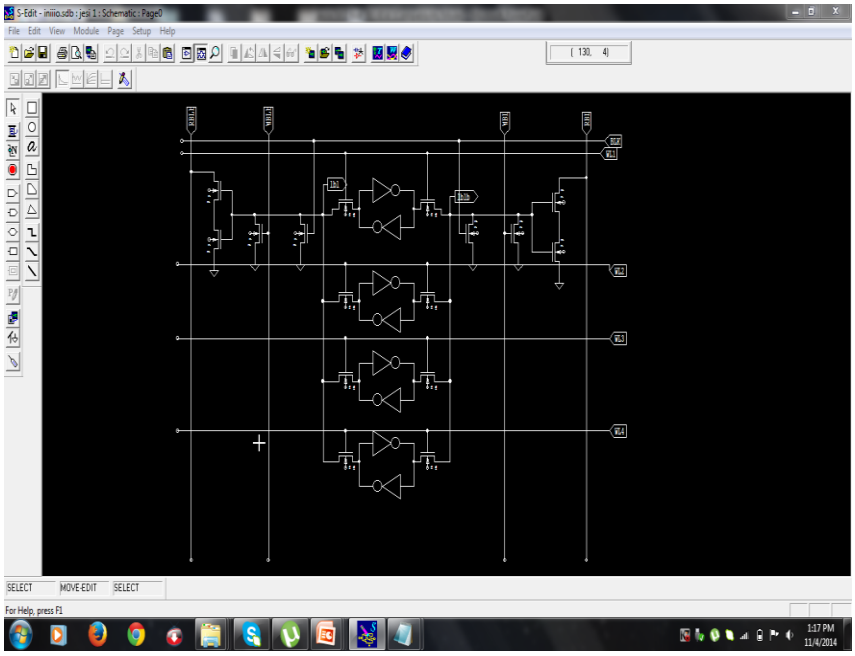

Figure 1: A8TWRD Sensing Sub-threshold Circuit Diagram for 4 bits

The above figure shows the schematic view of the proposed technique for 4 bits.

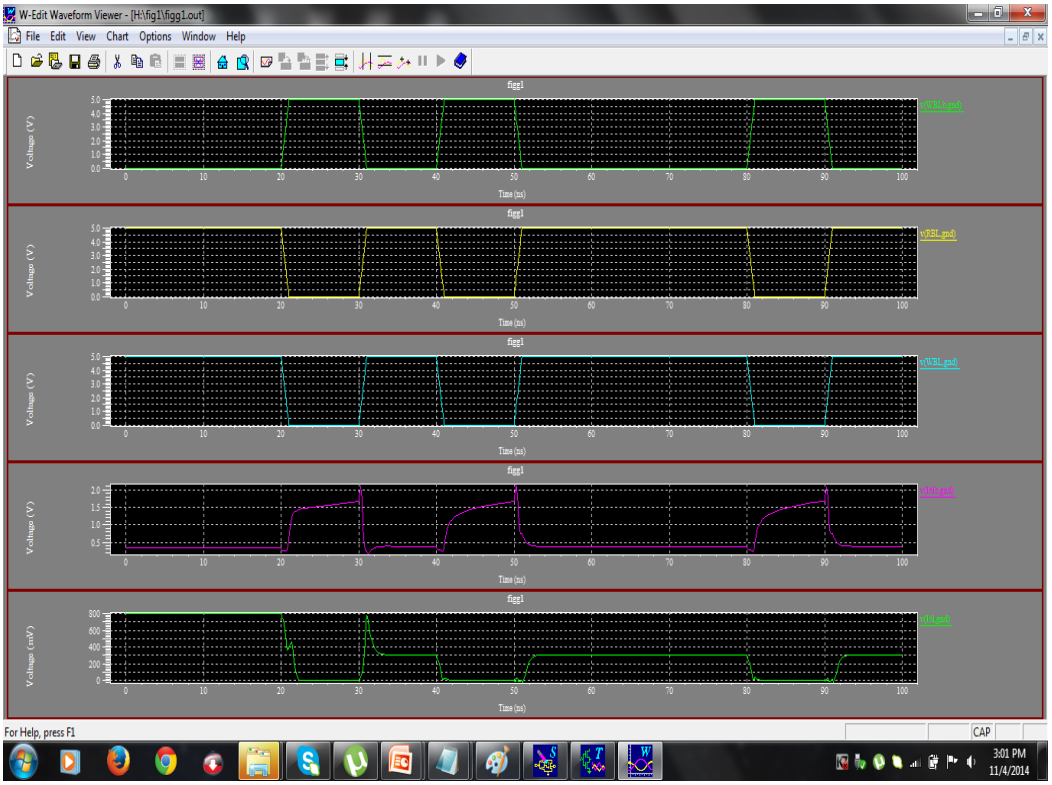

Figure 2: A8TWRD Sensing SRAM Transient Analysis

Above Fig 2 show the transient analysis of A8T-WRD Sensing Sub –threshold SRAM. Here, the first plot shows the word line, second read bit line, third write bit-line, fourth line is the local bit line and the output signal in the fifth graph.

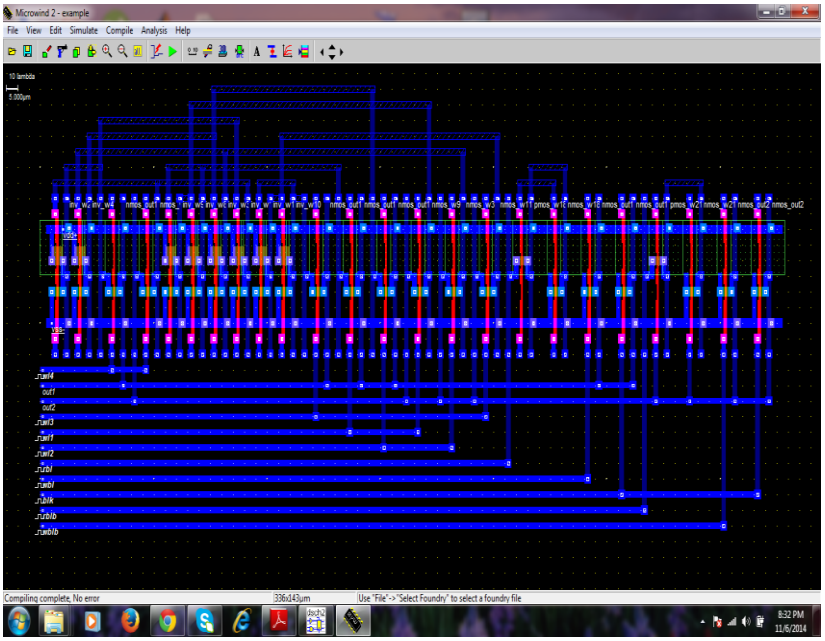

Figure 4: Layout of A8TWRD Sensing sub threshold SRAM for 4 bits

Fig 4 shows the layout of i average 8T write read sensing subthreshold SRAM (A8TWRD Sensing sub threshold SRAM). for 4 bits

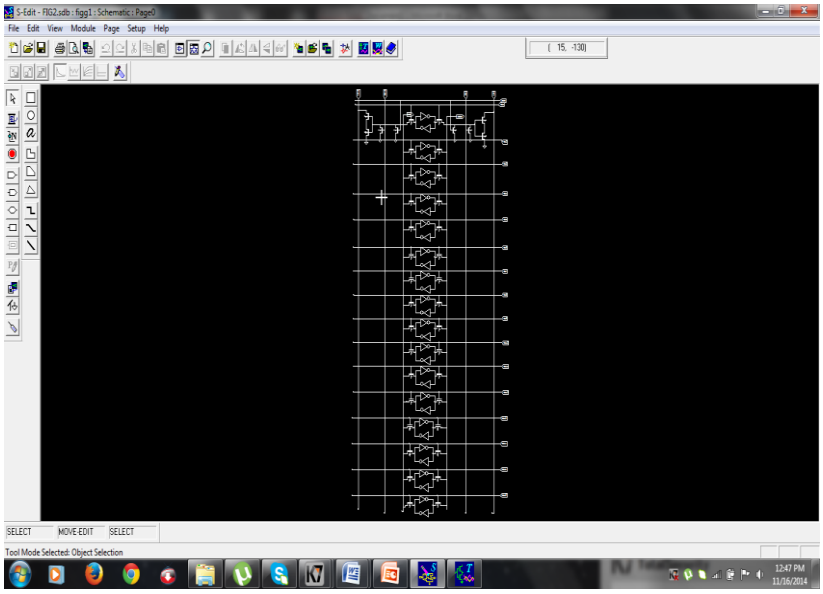

Figure 5: A8TWRD Sensing Sub-threshold Circuit Diagram for 16 bits

The above figure shows the schematic view of the proposed technique for 16 bits.

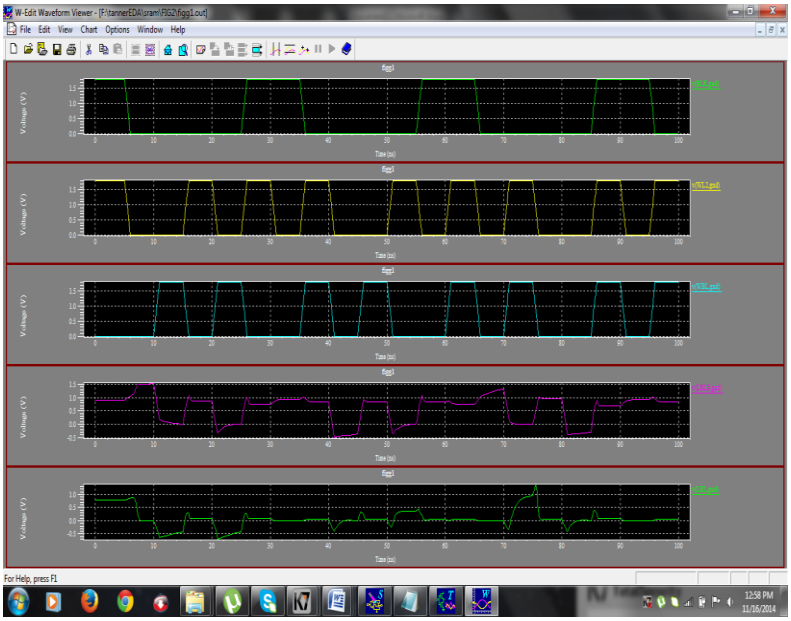

Figure 6: Transient Analysis of A8TWRD Sensing sub threshold SRAM

Above Fig 6 show the transient analysis of A8TWRD Sensing Sub –threshold SRAM. Here, the first plot shows the word line, second plot the read bit line, third plot the write bit line, fourth line is the local bit line and the output signal in the fifth line

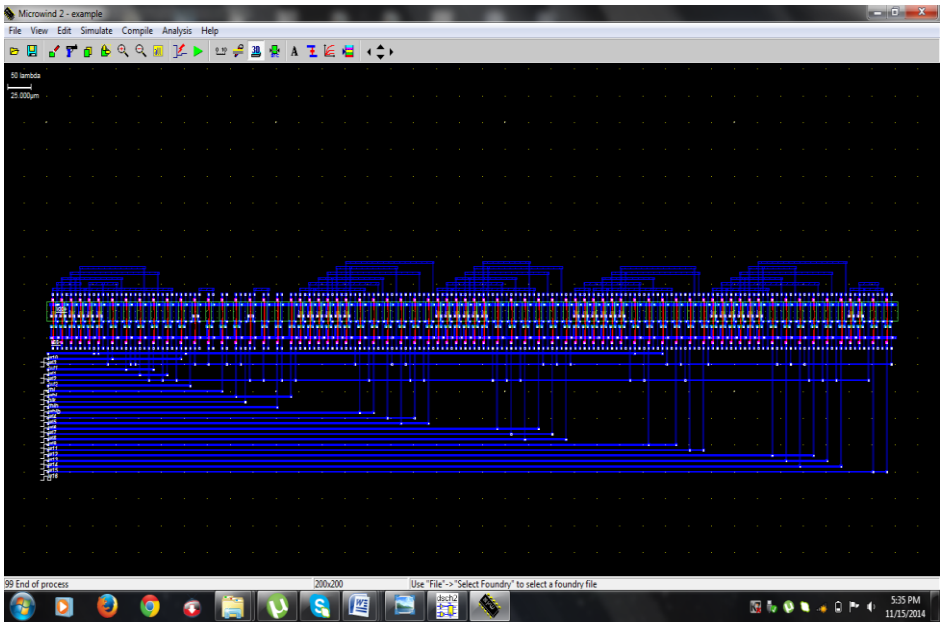

Figure 8: Layout of A8TWRD Sensing sub threshold SRAM for 16bits

Above Fig 8.shows the layout of 16 bits in the proposed system

Table 1: Power Consumption of different SRAM Circuits

SRAM Methods	**Power Consumption(μw)**
Conventional 8T SRAM	3.7661
A8T-WRD Sensing Subthreshold SRAM for 4 Bits	1.3677
A8T-WRD Sensing Subthreshold SRAM for 16 Bits	4.0956

Table 1 Shows comparison of different SRAM circuits. The proposed circuits consume less power than the existing method.

Conclusion

Low voltage and Low power SRAM design is critical in embedded systems. In this work, examining the related issues of simultaneously reducing the power consumption and leakage current, An average 8T write /read – decoupled (A8TWRD) SRAM cell architecture for sub/near –threshold embedded SRAM has been proposed..In the proposed method, power consumption is reduced by 30% than the existing method.

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