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CPW Based DMTL Phase Shifters: A Survey

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Abstract

Distributed MEMS Transmission Line (DMTL) circuits are widely used in the design and development of phase shifters that have various applications in instrumentation systems, wireless communication circuits and phased array antenna systems. In this paper we present a survey of DMTL phase shifters at different frequency bands and identify the various issues associated with it which helps the general readers have an overview of design, losses and frequency of operation with overall device performance. Major concerns in analog and digital design of DMTL phase shifters are highlighted. Fabrication and packaging issues are outlined and discussed.

Keywords: DMTL, CPW, Phased array antenna, Phase shifters, Loss.

1. Introduction

Microwave and millimeter-wave phase shifters are essential components in radar, wireless and satellite broadband communication network systems. Majority of the current phase shifters are either of ferrite or semiconductor device based design. Large size and high cost forbid use of ferrite based phase shifter phased-arrays in public communication and related industries. Semiconductor-device-based phase shifters have been used up to 100 GHz. There are varied designs of the semiconductor-device-based phase shifters. Some of the popular designs are switched-line [1], loaded-line [2], [3], branch-line [4], reflect-line and DMTL phase shifters. The switched-line phase shifter is a True-Time Delay (TTD) device but with limited bandwidth. The lossy effect and narrowband restriction of phase shifters based on FETs or P-I-N diodes have been overcome by replacing active switching element with Micro Electro Mechanical System (MEMS) technology. MEMS devices inherently have low insertion loss, high isolation, low drive power of the order of µW and extremely low series resistance at RF and millimeter wave frequencies. In addition to this, as MEMS devices do not contain a semiconductor junction they lack any measurable inter-modulation distortion [5]. Though the MEMS switches significantly minimize the circuit losses, they do not address the bandwidth issue. Bandwidth can be improved by periodically loading the transmission line with MEMS switches and forming a Distributed MEMS Transmission Line (DMTL).

In view of the low insertion loss, low power dissipation and broadband characteristics, the DTML phase shifters find more and more applications. A distributed phase shifter can be easily designed by ready adaptation of a tunable reactance to the transmission line. Most of the DMTL emphasizes on adding tunable shunt capacitors rather than inductors which are cumbersome to make. In DMTL, the high impedance transmission line (>50Ω) is loaded periodically with varactors or capacitors enabling tuning of the propagation constant. DMTL has a very low series resistance as compared to any solid state device. Thus it is possible to fabricate a low loss characteristic device on relatively low permittivity substrates such as Quartz and glass [6]. Improvement in phase shift is achieved by the appropriate choice of MEMS capacitance and the unloaded transmission line characteristics. In any DMTL, the phase variation is meliorated only by increasing the unloaded transmission line parameters. The present work becomes significant in synergizing all possible improvements in structure and fabrication methods possible with the DMTL phase shifters. The paper is organized as follows: Section 2 provides an outline of DMTL phase shifters. Section 3 briefs the primary concerns of analog DMTL phase shifters. Section 4 deals with digital DMTL phase shifters and Section 5 elaborates the fabrication techniques of DMTL phase shifters. The discussion and conclusions are covered in Section 6.

2. Outline of DMTL phase shifters

In this approach, uniform length of high-impedance Coplanar Waveguide (CPW) transmission line is loaded by periodic placement of MEMS switches which act as shunt capacitors/ varactors. Fig.1 shows CPW based DMTL phase shifter. Current microwave MEMS switches have been fabricated in both series and shunt configurations. In the series configuration, when the MEMS switch is actuated (i.e., the top electrode pulled down), the signal path is completed, whereas in the shunt configuration, the signal path is shorted to ground with the switch actuation. DMTL has a capacitive switch with a thin metal bridge suspended over CPW that moves with the applied dc voltage to bottom electrode with respect to metal bridge. A thin dielectric on the bottom electrode renders electrical isolation and takes the edge off stiction.

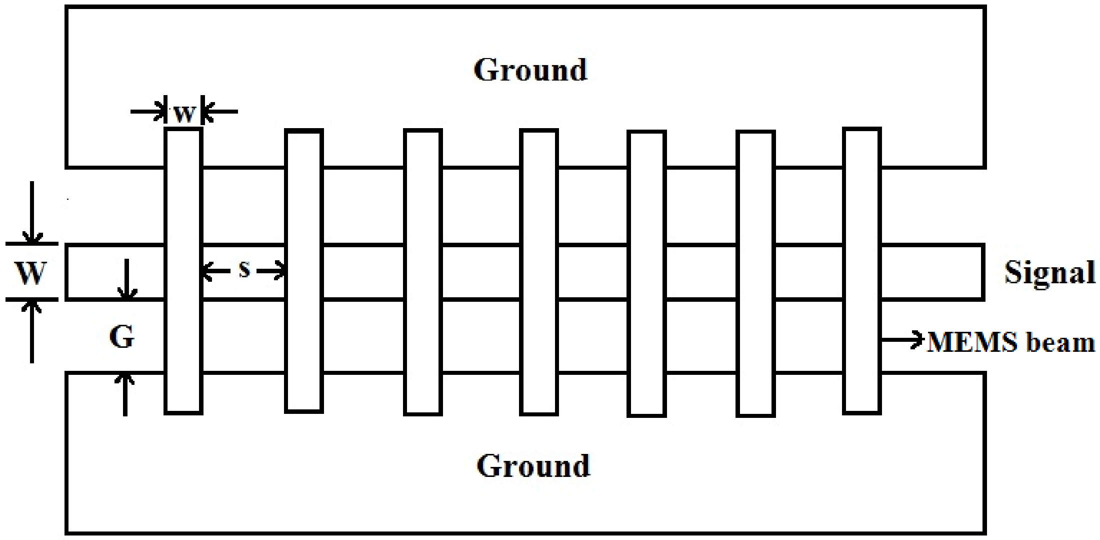

Figure1. DMTL Phase shifter on coplanar waveguide

The applied bias to the metal bridge modifies the height of the MEMS bridges which in turn alters the distributed capacitance in sequence resulting in changes in the loaded transmission line impedance and phase velocity effecting phase shift as follows

$$\Delta\phi = \frac{s\omega Z_o\sqrt{\varepsilon_{r,eff}}}{c}\left(\frac{1}{Z_{lu}} - \frac{1}{Z_{ld}}\right) \ldots.. \qquad (1)$$

In a DMTL phase shifter, the impedance and propagation velocity of the resulting slow-wave transmission line are determined by the dimensions of the MEMS bridges and their spacing periodicity. Distributed loaded line phase shifters have been implemented both in analogue and digital forms. An analog phase shifter allows continuous phase variation, while digital confines only to differential phase shifts at predetermined discrete values.

3. Primary concerns in Analog phase shifters

Analog DMTL phase shifter employs RF MEMS varactors to achieve the desired capacitance ratio that is usually limited to 2 in the 30 to 100GHz frequency range. Phase shifts of any desired resolution can be achieved in analog phase shifter as against digital phase shifters where resolution is determined by the number of bits. The structure acts as a phase shifter when the applied voltage is less than the pull-down voltage. The pull down voltage of the bridge is given by

$$V_p = \sqrt{\frac{8kg^3}{27\varepsilon_o A}} \; \ldots.. \qquad (2)$$

By applying a single bias voltage on the line, the distributed capacitance can be changed. The following sections present numerous approaches in analog DMTL phase shifters design

3.1. Tuning range

In an analog DMTL phase shifter, using RF MEMS switch, when the biasing voltage exceeds pull-in voltage, the membrane snaps until it touches the CPW line. The range of phase shift variations is limited as the movable range of the bridge is limited only to 1/3rd of the initial gap. To achieve the required phase shift, longer transmission line and increased number of bridges are required to be used. This entails increased insertion loss. Maximum tuning range of MEMS capacitor structures using flat bridges is approximately 33% of its initial height resulting in a 50% tuning. Higher tuning is achieved by using custom fabricated two-layered bridge that circumvents the pull-in phenomena by separating the capacitance from the electrostatic electrodes [7, 8]. In this method, higher deflection ratio at the capacitor is achieved due to pull in deflection at the electrodes [7]. Ativanichayaphong et al. proposed a multistep varactor structure for reactance variation with the remaining 2/3rd of air gap that is not utilized wherein a single bridge and single actuation voltage enables multiple phase shifts. The multistep varactor structure has layers of metal that are electrically separated from each other and connected to ground plane [9]. In the light of the available literature, it is apparent that to achieve wider bandwidth and low insertion loss, height of MEMS bridge is always confined to the limit of 2 to 5 µm range which usually produces a phase shift of less than 10 degrees. Wu et al. proposed a method to increase the capacitance ratio with a thin coat of insulation layer on center conductor under the bridges and by using saw-shaped transmission line [10].

3.2. Actuation voltage

The performance of distributed MEMS phase shifter is characterized by dc control voltage and operational frequency range. Consequently, a design with an optimum actuation voltage and Bragg frequency assumes significant importance [11]. For frequencies well below the Bragg frequency, the periodically loaded line in a distributed Phase shifter may be treated as a synthetic transmission line whose capacitance per unit length increases due to the loading period. The inductance per unit length for this synthetic line remains unchanged. Since loading capacitors are voltage dependent, the properties of synthetic transmission line also are voltage dependent. Hence it is possible to change the phase shift for a given length of line by changing the bias voltage [12]. It has been a significant issue to minimise the actuation voltages of the MEMS structures. The actuation voltage can be minimised by reducing the bridge height or choosing bridge materials such as polymer which have a comparatively low elastic modulus. However, it is not recommended to resort to decreasing the height of the MEMS bridges in order to achieve reduced actuation voltage, as it worsens the fabrication yield for the MEMS phase shifter. Ji et al. [13]

proposed that the best way to decrease the actuation voltage is by fabricating the MEMS bridges with polymers whose elastic modulus is around 5GPa, (much less than metals with 50–100Gpa). The novel concept to combine micro-stereo-lithography and thick-resist UV lithography technologies in order to make micro-gears presented by Bertsch [14] cannot be applied to the MEMS phase shifter directly because a metallization step is needed for the polymer MEMS bridges. Ji et al. demonstrated a method to combine the micro-stereo-lithography and the conventional silicon surface micro-machining technique in fabricating low-cost MEMS phase shifters with low actuation voltages.The actuation voltage can be lowered by changing the gap height between MEMS bridges and bottom electrode but it fosters the parasitic capacitance of the bridge in upstate. Kim et al. proposed a method of directly applying bias to MEMS capacitor avoiding the series MAM capacitors by utilizing choke spiral inductors in the bias circuit that greatly reduces the actuation voltage [15].

Generally any membrane design should provide highest mechanical stability and low actuation voltage for reliability and phase shifting of RF MEMS switch. Biasing RF MEMS varactor close to its pull-in-point affects the linearity of the device. This nonlinear effect is reduced by connecting two varactors with same equivalent capacitance and opposite DC biases that make the bridges vibrate in opposite directions leading to the cancellation of significant side bands [16]. As the control voltage between center conductor and ground plane is increased, the shunt capacitance of RF MEMS switch increases there-by increasing the capacitive loading of transmission line. In a DTML, when RF MEMS devices are used as loading capacitance, the capacitance ratio must be limited to 2-5. In order to provide a robust operation with low loss and excellent impedance coverage, a minimal contact RF MEMS switches is proposed by Shen and Barker [17].

Table 1 presents the results of various works published using analog implementation.

Year	Frequency (GHz)	Substrate	Insertion loss (dB)	Max phase shift	Bridge number	Voltage	Capacitance ratio	Reference
2007	13.7	Si	2.5	180^0	6	NA	NA	[18]
2006	40	Fused silica	2.4dB/cm	225^0/dB	17	16	3.4	[7]
2005	20	Si	2.3	250^0	16	35	1.8	[19]
2004	20.5	Glass	7	90.2^0/dB	12	NA	NA	[20]
2002	25 and 35	Si	2.1 3	150^0/dB-25GHz 211^0/dB-35GHz	11	37 69	7.5	[21]
2002	35	Quartz	4	372^0	8	32	NA	[22]
2000	40 and 60	Quartz	5.1 4	70^0/dB 90^0/dB	32 38	13	1.3-1.5	[23]
1999	20	GaAs	4.2	0-360°	15	0-10	NA	[11]
1998	60 and 40	Quartz	2 1.8	2dB-118^0 1.8dB-84^0	8 and 16	10-23	NA	[24]

NA – Not Available

4. Primary concerns of Digital phase shifters

With the limitation on the control range of the bridge height in analog DMTL using varactors, the resultant phase shift is relatively small. For increase in relative phase shift, unacceptable long structures may be needed because of small loading. This problem is overcome in digital phase shifters [11] by operating the MEMS bridges in the digital mode, where two distinct capacitance states (ON: bridge snapped and OFF: bridge as is) are defined with a high capacitance ratio. Digital phase shifters with this approach achieve large phase shift and are less vulnerable to noise. Discontinuity introduced by MEMS bridge loading on CPW adds shunt capacitance [25]. This shunt capacitance is in parallel with the distributed capacitance of the transmission line and is included as a primary design parameter of the loaded line.

Digital DMTL phase shifters having a capacitive ratio up to 20 enables, higher phase shift per unit length resulting in shorter structures, but at the cost of increased impedance mismatch. Best return loss performance is obtained when MEMS devices are spread evenly along the line to avoid long section of different impedances. Equation 1 shows that broad deviation in impedance results in more phase shift but at the detriment of return loss. Besides, the phase shift could be doubled if the tolerable reflection coefficient is 10dB instead of 15dB. For Cascading two phase shifter sections to obtain two bit phase shifter, the maximum reflection coefficient is preferred to be 15dB so that the resultant cascaded structure will have values less than 10dB [26]. Slow wave structures are created in cascadable transmission line sections using MEMS ohmic switches where capacitance and inductance can be simultaneously increased at constant ratio without affecting impedance matching. Inspite of impressive figure of merit, the ohmic switch can consume high stand by power. Hence a capacitive switch with negligible stand by power consumption was proposed by Palego et al.[27].

Performances of digital phase shifters available in literature are compiled in Table 2.

Year	**Frequency (GHz)**	**Substrate**	**Bit number**	**Insertion loss**	**Max phase Error**	**Bridge Number**	**Size mm^2**	**Static capacitor**	**Actuation Voltage**	**Reference**
2010	10	Si	5	1.54	2.14%	32	19.11×2.646	MAM	15	[28]
2010	10	Quartz	2 and 3	0.3 to 1	NA	18	NA	MIM	15-20	[29]
2010	10	Si	5	1.49	2.24% (3.17^0)	31	5.36×4.72	MAM	20	[30]
2010	35	Quartz	5	4	NA	31	NA	MAM	50.7	[31]
2006	50	Quartz	4	1.2	5.5^0	10	4.6mm long	MAM	30-35	[40]
2006	15	Glass	3	1.5	NA	128	60×50	MAM	16	[6]
2004	78	Glass	2 and 3	1.8 to 2.1	$\pm 3^0$	2bit-24 3bit-28	2bit-4.3×1.46 3bit-5.04x1.92	MAM	30	[33]
2003	Ka-37.7 X-13.6	Quartz	2	Ka-1.5 X-1.2	13^0	21	8.4×2.1	MAM	13-14	[34]
2002	60 and 65	Quartz	2 and 4	2.2 and 2.8	6.5% and 1.3%	2bit-24 4bit-30	2bit-6.3×1.5 4bit-7.9×1.5	MAM	15-35	[15]
2001	16	Si	2 and 4	3	8.5^0/-6^0	29	NA	Microstrip-MIM	NA	[35]
2000	10	Quartz	1 and 2	1.5	NA	8	22	MIM	40	[36]

NA-Not Available

Conventional CPW DMTL design necessitates a high capacitance ratio giving rise to a poor return loss performance. The enhancement of MEMS capacitance ratio affects the impedance variation and decreases the return loss performance despite improvement in phase shift. In order to take the advantage of increased phase shift per unit length, it is prudent to place a small capacitor (that does not infix significant loss) in series with RF MEMS switch. Alternatively a tapered transmission line in different configuration like stepped impedance, linear taper, bow-tie configuration can also accomplish improved phase shift [21, 37] that enables a wide working frequency range and allows adjustment of return loss independent of phase shift tuning. While endeavoring to minimize insertion loss, the importance of device length is usually neglected that degrades the process uniformity during fabrication. Minimization of device length is achieved by duly considering the parasitic parameters [32].

Ka band DMTL phase shifter at 30–40 GHz utilizing high- metal–air–metal (MAM) capacitors instead of the standard metal–insulator–metal (MIM) capacitors was proposed [34]. The high- MAM capacitors are responsible for a drastic improvement in the performance of the DMTL phase shifter. Hayden and Rebeiz proposed cross-over between the MEMS bridge and the CPW ground-plane to build high-Q MAM capacitor [38]. Also, high-resistivity bias lines have been introduced for lower voltage actuation of the MEMS switches. Furthermore, the system losses and size are reduced by implementing the RF MEMS phase shifters in a phased array monolithic structure manufactured by micromachining technology [6]. The low capacitance per unit area and high-Q factor of the MAM capacitors make them better suited than MIM capacitors for V-band applications [15]. Use of series connected MEMS switch to maintain a low down state capacitance value endures the design of extremely small fixed capacitor. Hence Yu Liu et al. proposed tapering the center conductor and depositing 6000 Å SiN layer at the contact area of the switch with conductor to reduce down state capacitance value [39]. The desired return loss poses a restriction on the amount of phase shift in view of impedance matching considerations. Hence Lakshminarayanan and Weller proposed a cascaded switchable slow wave CPW sections that accomplishes high return loss in both states using a semi lumped equivalent-circuit model [40].

Distributed MEMS TTD phase shifters using both inductors and capacitors were proposed by Afrang and Majlis [32] to decrease the size of the structure by sustaining the maximum amount of phase shift with the minimum amount of insertion loss and with a low return loss per unit cell. It is well-known that the inductor changes the phase of a signal the same way as the capacitor. They utilized MEMS switches and inductors to change loading capacitance and inductance on a high-impedance t-line such that the return loss is within a satisfactory range for the two phase states of DMTL design. Issues like microwave interference among adjacent component coupling between signal line and ground line, radiation loss to open space are addressed using a bridge like a coplanar waveguide structures that covers a MEMS bridges. Increase in capacitance ratio is achieved by an insulation layer in the center conductor under the bridge [41].

4.1. Reliability issues

For long term reliability of DMTL phase shifters, depending upon the applications, fulfillment of environmental requirements like temperature, vibrations and variations of signal strength are crucial [42]. Excessively long length poses a challenge to implementation of MEMS distributed phase shifter. For a 5 or more bit phase shifter, the device is so long that it is easy to break, which will decrease the reliability of the device and increase the cost and difficulty of packaging. Switch reliability issues arise due to intimate contact that occurs between beam and the dielectrics with repeated operations. Reliability of the MEMS switch can be significantly improved by reducing the contact area between the actuation section of the MEMS device and substrate. Digitally controlled RF MEMS varactor with outstanding performance between 20 to 50 GHz can be created using minimally contacting MEMS switch [43]. Capacitance ratio (C_r) must be limited to 2-5 while RF MEMS devices are used as loading capacitance in any DMTL. One method to limit C_r is to place a metal-air-metal capacitor in series with RF MEMS capacitor. But here the reliability issue is not addressed. Contactless RF MEMS address both issues. C_r can be controlled by limiting the range of motion of RF MEMS beam with standoff at its bottom that prevents the beam contacting center conductor.

With the device becoming longer, process consistency will suffer sharp degradation which results in a relatively larger deviation between designed and actual results. Lacroix et al. proposed fast miniature RF MEMS switched capacitors that are less susceptible to residual stress, temperature variation and charging in the dielectric layer to provide an impedance transformation allowing a phase shift along the total length of the line [44].

4.2. Bragg frequency

The guided wavelength approaches the distributed periodic spacing at Bragg frequency wherein DMTL has almost total reflection and the linearity of phase shift increases with it at the expense of smaller separations between the MEMS bridges. Higher reflection loss occurs in the periodic structure beyond Bragg frequency. It is required to optimize the Bragg frequency much higher than frequency of operation of switch. The effect of creating periodic structure is to bring the Bragg frequency near the point where guided wavelength approaches the periodic spacing of the discrete components. As a rule of thumb, operational frequency is approximately half of the Bragg frequency [45]. Generally for a maximum reflection coefficient of 15 dB the Bragg frequency must be at least 2.3–3 times that of the design frequency [26]. MEMS bridge cannot be completely patterned by single capacitor due to the presence of some inductance and resistance in the bridge. Although resistance has negligible effect it is found that inductance creates a noticeable effect on the position of Bragg frequency that affects performance of DMTL's [23].

5. DMTL fabrication technologies

Lack of control on bulk and gradient stress makes the released bridge to curl imposing greatest challenge on fabrication of the bridges [26]. Among two important silicon micro machining- bulk and surface micro machining, former is utilized in manufacturing of majority of commercial devices. In Bulk Micromachining, the micro mechanical structures are realized within single crystal silicon by selective removal etching process. In surface micro machining structures are located mainly on the surface of silicon wafer and exists as thin film. They can be easily integrated with IC components [46]. MEMS phase shifters that utilizes surface micro machining of metal bridges over CPW endures issues like thermal incompatibility between micro bridges and substrate and causes creeping. This is subdued by bulk micro machining [20]. Losses originating from silicon substrate are the major drawback of DMTL phase shifter. At high frequencies attenuation of RF signal is high on CMOS grade low resistive silicon substrate. In contrast, high resistivity silicon substrate suffers from parasitic capacitance and resistive losses. However, polymers between CPW transmission line and low resistivity silicon substrate acts as a passivation layer and minimize the losses.

Insertion loss could further be reduced by etching away the silicon substrate there by leaving only polymer under CPW line. Losses related to conductivity of silicon substrate are mitigated by fabricating the whole device on a thick silicon dioxide. Surface isotropic etching used on low losses high resistivity silicon is not suitable for low resistivity silicon as the fixed lines pervades much deeper than the depth of the silicon etched out by micro machining. Complete etching on silicon and oxide beneath CPW center conductor and selectivity below the ground planes by bulk micro machining reduces the losses due to low resistivity silicon substrate [47]. A thin dielectric layer on the bottom electrode prevents a dc contact when the switch is actuated. This results in a capacitive switch suitable for 10-40GHz applications. But then, charging of the dielectric layer is one of the biggest issues related to capacitive MEMS switches. To get rid of this problem, dielectric-less capacitive MEMS switches have been developed by several research groups. Still, thicker electroplated layers are used in all of these components, which make fabrication rather tardy and difficult to be carried over to mass production. Vaha and Ylonen developed a surface micromachining process and components that use only thin-film techniques [48]. Inspite of low insertion loss and wide bandwidth operation, commercialization of DMTL are hindered by lack of production worthy wafer level packaging. Generally distributed MEMS phase shifters packaging processes are based on traditional IC wafer bonding processes like fusion bonding, anodic bonding, eutectic bonding, glass-frit bonding and thermo compression bonding. As the distributed MEMS phase shifters packaging are made of movable and fragile structure, challenges like clean and stable environments, ambience stability, low process temperature, light weight, small size, low loss and high performance need to be overcome. These problems are subdued in a packaging MEMS device on thin high resistivity silicon substrate with vertical feed through using wafer level micro packaging [49].

6. Discussion and conclusion

The proposed paper briefly discussed a vital survey of existing literature on DMTL phase shifters. Table 1 and 2 provides the general performance of the various analog and digital phase shifters. Analog based approaches attempt to achieve desired phase shift using pull-in phenomenon i.e. tuning based on the 1/3rd gap height rather than complete blocked state. The main advantage of the analog system is that they are used to obtain any desired resolution using continuous tuning of varactors. However, as mentioned above, this same property is their farthermost drawback too, since there is a confine on the control range of the bridge height before the bridge snaps and they showed comparatively small phase shift. This problem has been resolved by functioning the MEMS bridges in the digital mode, where two distinct capacitance states (ON and OFF) were defined with a high ratio. Digital phase shifters with this approach allow large phase shift and low sensitivity to electrical noise. In the published CPW digital phase shifters, a small metal–insulator–metal (MIM) capacitor or metal-air-metal (MAM) in series with the MEMS bridge capacitor was used to trim down the total shunt capacitance seen by the line, resulting in an satisfactory return loss for both switching states over a wide band. Subsequently, the digital phase shifters performance is mainly limited by the small fluctuation in bridge capacitance that could be accomplished using electrostatic actuation in the region before the bridges are pulled down. One effort made at increasing this fluctuation in bridge capacitance is to increase the stable actuation region by integrating series capacitors in the bias route of DMTL. However due to dielectric charging the increased capacitance variation was never achieved. This problem has been reported by several researchers using capacitive MEMS switch technology. The disparity in the theoretical and practical capacitance variation is due to bridge thickness and residual stress that arises due to non-uniformity across the wafer during the fabrication process.

Fabrication process plays a spoilsport in limiting the results of DMTL for wideband operation. Advances in MEMS fabrication and static capacitor Q loss reduction attributes to the success of incurring low loss digital phase shifters. Exceedingly flat membranes which have predictable up/down capacitance states and have a life span of millions of cycles are the outcome of advancements in MEMS switch fabrication. The major aspects limiting even better performance of these phase shifters is the attenuation from MEMS switch biasing line which effectively lower the Q of static capacitors. Effect of bias line is lowered by changing the layout of bias resistors or using high resistive materials. Insertion loss, return loss and isolation are the parameters often used as system of measurement to ascertain the performances of DMTL phase shifters. Improvement in isolation is achieved through use of micromachining/micropackaging .Isolation was limited by outflow of signal through substrate modes. Several techniques could be used to lower the effect of substrate modes letting in distinguished layout to limit the coupling between the two sides of the switch. Important issues and statuses that make substantial contributions to the performance of DMTL phase shifters were highlighted in this work with the purpose of providing an overview to prospective researchers in this field.

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