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Design of An Enhanced Double-Tail Comparator For High Speed Adc

B.V.Anusha[1], A.Nandhini[2]
[1]II[nd] Year M. Tech VLSI Design, Sathyabama University, Chennai, India
[2]Assistant Professor Department of ECE, Sathyabama University, Chennai, India
Email id: anushaboyapati903@gmail.com, abnandhu@gmail.com,

Abstract

The need for ultra low-power area efficient and high speed analog to digital converters is pushing towards the use of dynamic regenerative comparators to maximize speed and power efficiency .Double-Tail comparator is one of the high speed comparator with small chip area .It can operates efficiently even at lower suppy voltages .In this paper ,an analysis on the power consumption and delay of the Double-Tail comparator will be presented .Based on the presented analysis ,a new dynamic comparator is proposed ,where the circuit of conventional Double-Tail comparator is modified for low-power and high performance even at low supply voltages .The proposed comparator will be designed by changing the input stage with an inverter based amplifier concept .It is shown that in the proposed Double-Tail comparator both the power consumption as well as delay time are significantly reduced compared to the conventional Double-Tail comparator .In this paper a Flash ADC is designed with proposed Inverter based Double-Tail comparator which will give low power consumption when compared to the conventional Double-Tail Comparator, The simulation will be done using Tanner tool.

Key words: Conventional double-tail comparator, Inverter based double-tail comparator, High speed Analog to Digital converters such as Flash ADC, low power design.

Introduction

A Comparator is a device that compares two voltages or currents and outputs a signal indicating which is larger. The comparator is designed to produce well limited output voltages that easily interface with digital logic. Comparators, on the other hand, are designed to operate in the open loop configuration without any negative feedback. In most of cases, they are not internally compensated. The speed and slew rate are maximized by using the comparator. The overall gain is also usually higher. The use

of an op-amp as a comparator leads to an unoptimized situation, where current consumption versus speed ratio is low.

Comparator is one of the fundamental building block in most of the Analog to Digital converters(ADCs).Many high speed ADCs such as Flash ADCs, require high speed, low power comparators with small chip area. Designing high speed comparators is more challenging when the supply voltages are smaller. Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Conventional dynamic comparator is one of the comparator which will give low power consumption at low voltages. A Double Tail comparator will give lower power consumption at low supply voltages when compared to the conventional dynamic comparator .High speed and delay time also reduced using this double tail comparator.

A clocked comparator is a circuit element that makes decision as to whether the input signal is high or low at every clock cycle .Most comparators are triggered by periodic clocks and therefore can be treated as linear, periodically time varying systems which mend themselves well to the periodic simulation framework of RF circuit simulators including Spectre RF and ADS .The latched comparator is a building block of virtually all analog to digital converter architectures .It uses a possitive feedback mechanism to regenerate the analog input signal into a full scale digital level. Flash ADCs contain many clocked regenerative comparators.

In this paper, an analysis about the delay and power consumption of the clocked regenerative comparators have been presented .The operation of the conventional Double-Tail comparator as well as Inverter based amplifier and their advantages and disadvantages of each structure have been discussed.

Existing Works

Clocked Regenerative Comparators:

Clocked regenerative comparators have been widely used in many high speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Conventional Double-Tail comparator can operates efficiently even at low supply voltages with high performance[1].

Conventional Double-Tail Comparator:

Fig 1 shows the schematic diagram of the conventional double-tail comparator. It gives better performance in low voltage applications, and it has been designed based on the double tail structure. The Latch regeneration speed can be increased by increasing $\Delta V_{fn/fp}$. Two control transistors (MC1 and MC2) have been added in the first stage in parallel to M3/M4 transistors but in a cross coupled manner for the purpose of increasing the speed of the comparator.

Operation of the Conventional Double-Tail Comparator:

There are two modes of operation .During the reset phase i.e (CLK=0,Mtail1 and Mtail2 are OFF, avoiding static power),M3 and M4 pulls both fn and fp nodes to VDD, the control transistors are cut off stage .The intermediate stage formed by MR1

and MR2 passes the differential voltage to the cross coupled inverters and also provides good shielding between input and output .The Intermediate stage transistors will reset both the latch outputs to the ground.

During the comparison phase the CLK=VDD,Mtail1 and Mtail2 are ON And the transistors M3 and M4 will turn OFF. Furthermore, at the begining of this phase, the control transistors are still in off posision. Thus, fn and fp start to drop with the different rates according to the input voltages. Suppose VINP>VINN, thus fn drops faster than fp.(since M2 provides more current than M1).As long as fn continues falling, the corresponding pMOS control transistor (Mc1)starts to turn ON, pulling fp node back to the VDD. So other control transistor (Mc2)remains off, allowing fn to be discharged completely .In other words, unlike conventional double-tail comparator, in which Vfn/fp is just a function of input transistor transconductance and input voltage difference .Therefore after some time, the difference between fn and fp increases in an exponential manner, leading to the reduction of latch regeneration time. In this circuit i.e Fig 1,when one of the control transistors(e.g Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor(e.g Mc1,M1,and Mtail1),resulting in static powerconsumption. To overcome this issue, two n MOS switches can be used below the input transistors(Msw1& Msw2)as shown in Fig 2.

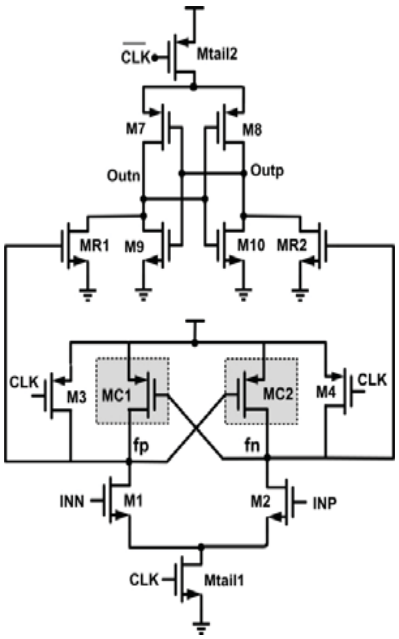


Figure 1: schematic diagram of conventional double-tail comparator

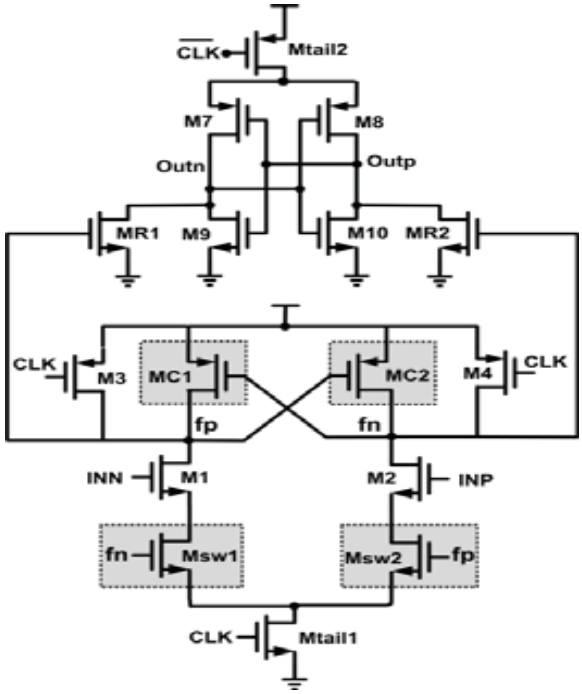


Figure 2: final schematic of conventional double-tail comparator

At the begining of the comparision phase, due to the fact that both fn and fp nodes have been precharged to VDD(During the reset phase),both the switches will be closed and fn and fp starts to drop with different discharging rates depending upon the inputs .Suppose if fp is pulling up to the VDD and fn was discharged completely, so the switch in the path of fp will be opened but the other switch connected to fn will be closed for allowing the complete discharge of fn node.

The operation of the existing comparator can be shown in Fig 3.It will shows the transient simulations of the conventional Double-Tail Comparator.

Simulation Output

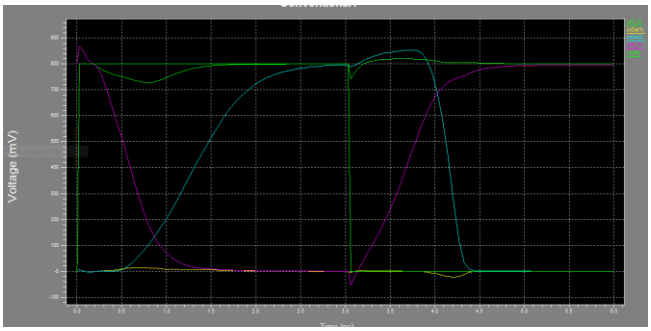


Figure 3: Transient simulation output of the conventional double-tail comparator.

The main disadvantage of this comparator is area can be increased .Power consumption will be more and delay also increases .To overcome all these issues we proposed a new comparator that can be explained below.

Proposed Method

Inverter Based Double-Tail Comparator

The proposed double-tail comparator has been designed based on the Inverter based amplifier concept .The main idea of the proposed comparator is to achieve high performance with lower power consumption and less area .In the proposed comparator there are two stages they are input stage and the latching stage .Here we have used the inverter based amplifier concept in the input stage .It can operates at subthreshold region. Subthreshold conduction or subthreshold leakage or subthreshold drain current is the current between the source and drain of the MOSFET, when the transistor is in subthreshold region, or weak-inversion region, that is, for gate-to-source voltages below the threshold voltage. In digital circuits, If a state that would ideally have no current then subthreshold conduction can be viewed as a parasitic *leakage* . To reduce the sub threshold effect here we uses the stacking scheme an design of inverter based double-tail comparator has been proposed as shown in Fig 4.

The schematic diagram of proposed Inverter Based Double-Tail Comparator is as shown in the Fig 4.Two inverters cross coupled acts as a latch as shown in Fig 5..Double-Tail comparator enables both large currents in the latching stage as well as small currents in the input stage .If this structure is implemented in lower supply voltages the transistors forming the inverters will operate in weak inversion region. Bias currents and power consumption can be reduced .A tail current source can be added for better controlling the current flow through the inverters, pushing the transistors further into the subthreshold region and to reduce the power .The use of tail seperates the need for low power consumption and low input offset voltage .The tail can also improves the CMRR.

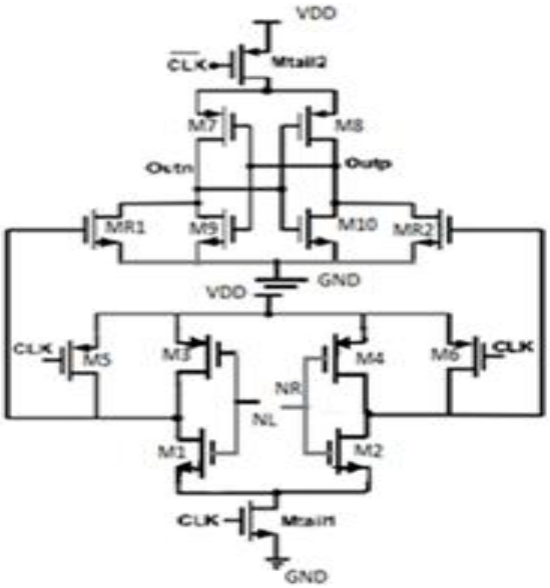


Figure 4: Schematic diagram of the Proposed Inverter Based Double-Tail Comparator

Operation of the Inverter Based Double-Tail Comparator

The operation of the proposed Inverter based Double-Tail comparator is as fallows .There are two phases of operation .They are Reset phase and the comparision phase .During reset phase CLK=0,Mtail1 and Mtail2 are off the transistors M5 and M6 will turn on .Maximum VDD will flows through the transistors M5 and M6.Depending upon the inputs NL and NR the charging and discharging of output nodes will occur. Suppose if NL=1 the inverter output will be 0 but here max VDD will flows through M5 so we are considering the output as 1.This output will be applied to the MR1 as shown in the Fig 4.MR1 will turn on and the inverter formed by (M7 and M9) output i.e out n will discharge to the ground .so here we have out n=0 and it is applied as input to the other inverter formed by M8 and M10. so max VDD will stores at out p .if NR=1the operation is viseversa.

During the comparision phase CLK=1,Mtail1 and Mtail2 are on and M5 and M6 will turn off .The maximum VDD will be stored in outp and outn .In this case depending upon the input values charging and discharging of output nodes will occur .If NL=1 then the inverter output will be 0 so the MR1 transistor is off .outn restores the value of VDD .If NR=0 the output of the inverter will be 1 and the MR2 transistor will on and the out p discharges to ground .If NL>NR ,out p discharges faster than out n .If NR>NL the operation will be vise versa .In this way this proposed Inverter based Double-tail comparator will operates.

Advantages:

The main advantage by using this Inverter based Double-tail comparator is data storage will be more .Area can be reduced by using this comparator .Another advantage is power consumption can be reduced by using this and it will give high

performance .It can be operate efficiently even at low supply voltages .By using this we can achieve high output gain and Bandwidth .This input stage has the advantage of combining the trans conductance of the n and p transistors .The inverter based amplifier is having lower equivalant noise compared to the conventional common source amplifier.

The transient simulation of proposed Inverter based double-tail comparator is as shown in the below Fig 5.

Simulation Output

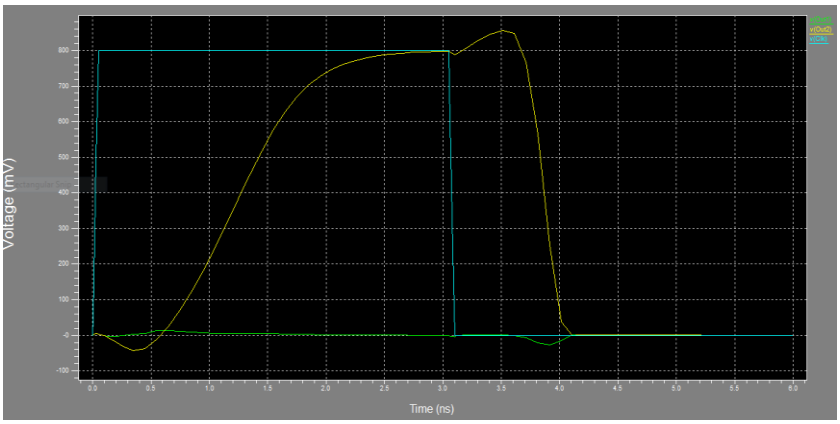


Figure 5: Transient simulation of Inverter based Double-Tail Comparator

Application

Application In Flash ADC:

Flash ADC is one of the high speed Analog to digital converter.Designing high speed ADCs is more challenging when the supply voltage is smaller.Many high speed ADCs such as Flash ADC require high speed low power comparators with small chip area.Flash ADC is designed using the conventional as well as proposed comparators.The block diagram of Flash ADC is as shown in the Fig 6.

Flash ADC block Diagram

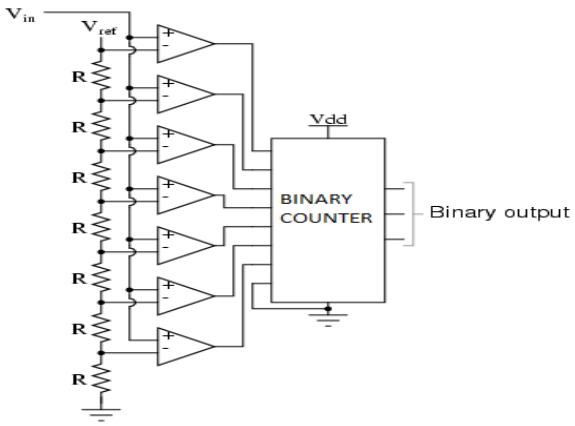


Figure 6: Block diagram of Flash ADC

Binary Counter Design:
K-Map Solutions For Outputs:

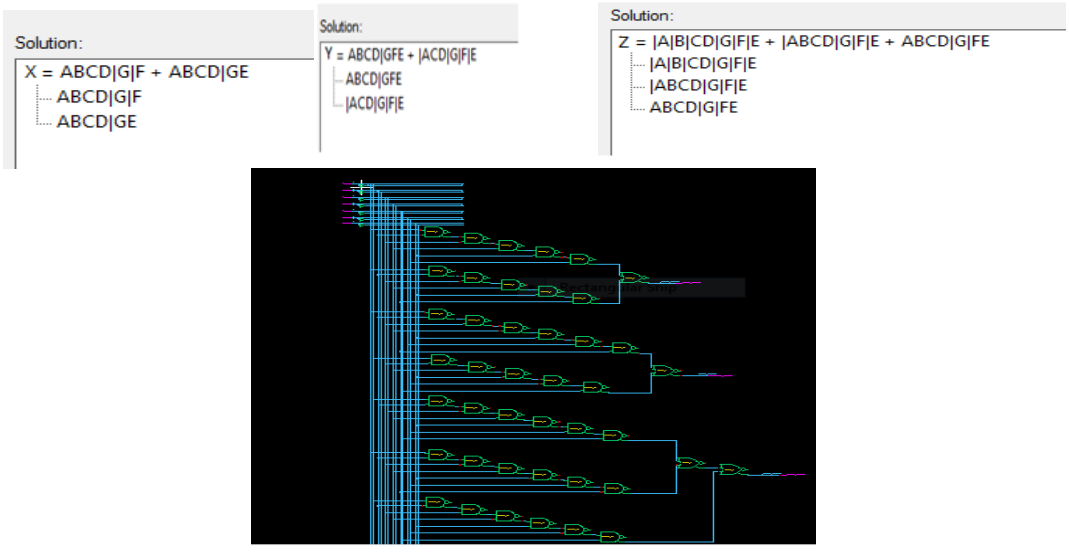


Figure 7: Design of Binary Counter

Design of Flash ADC With Proposed Inverter Based Double-Tail Comparator:

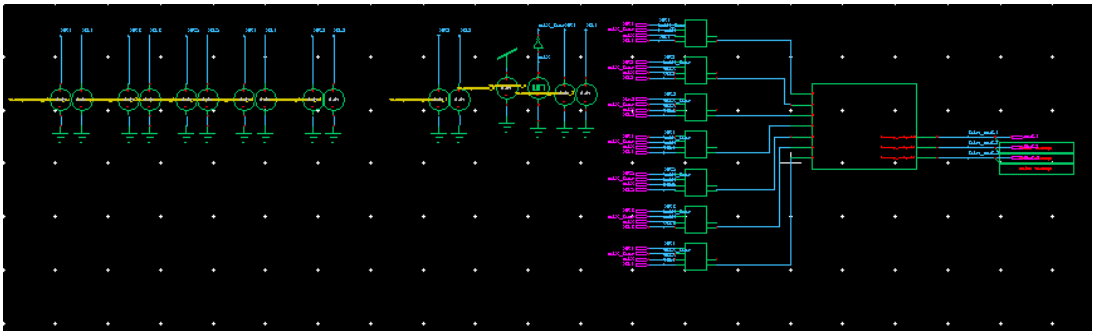
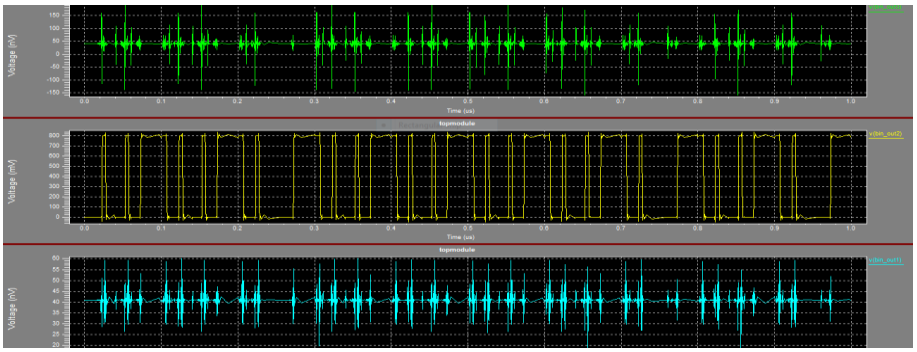


Figure 8: Design of Flash ADC using Inverter based double-tail comparator

Output Waveform



Design of Flash ADC With Conventional Double-Tail Comparator:

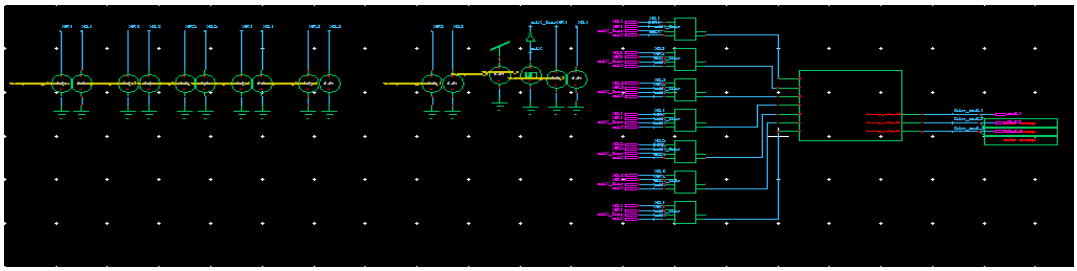
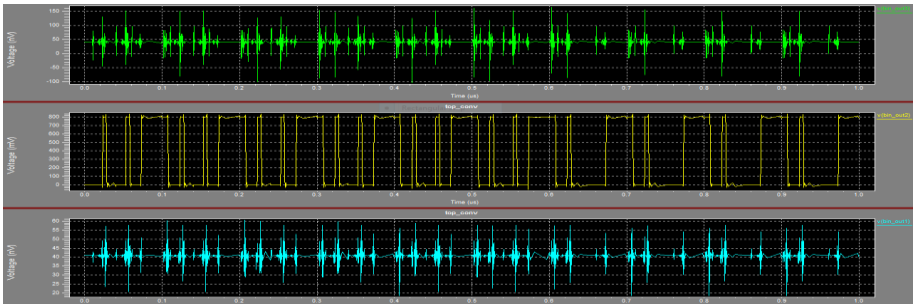


Figure 9: Design of Flash ADC using conventional double-tail comparator.

Output Waveform



Simulation Results

In order to compare the proposed comparator with the conventional double-tail comparator, all the circuits have been simulated in a 0.18µm CMOS technology with VDD=0.8V.The below comparision table shows the performance of the proposed inverter based double-tail comparator when compared to the conventional double-tail comparator.

Comparision Table 1:

Comparator Structure	Total No. of Transistors	Power Consumption	Delay
Conventional Double-Tail Comparator	18	13.6103µw	0.16074ns
Inverter Based Double-Tail Comparator	16	11.6692µw	0.018774ns

Comparision Table 2:

Flash ADC Structure	Power Consumption
Flash ADC With Conventional Double-Tail Comparator	30.73137µwatts
Flash ADC With Inverter Based Double-Tail Comparator	29.31218µwatts

Conclusion

In this paper, we presented the structures of conventional double-tail comparator and the final structure of conventional double-tail comparator has been analyzed. Also, based on the analysis, a new double-tail comparator with low-voltage low-power

capability was proposed in order to improve the performance of the conventional double-tail comparator .The designs of Flash ADC using the proposed double-tail comparator and the conventional double-tail comparator have been presented in this paper .The analysis shows that flash ADC using the proposed Double-Tail comparator will give less power consumption and high performance than the conventional double-tail comparator .The area also reduced by using this Inverter based Double-Tail comparator.

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