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A Survey ON MCML Logic Using Different Implementation And Techniques

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ABSTRACT

MCML (Mos Current Mode Logic) is a method used for the purpose of reducing the delay and power of the circuit. In high speed application this method is used to reduce the power. In this method the sleep transistor is inserted in series with the supply voltage (or) current source to reduce the power. Different power gating techniques are been used to reduce the static power and to improve the speed and efficiency of the circuit.

KEY WORDS– Mos Current Mode Logic (MCML), power gating, static power, efficiency and delay

1. INTRODUCTION

The VLSI design is mainly based on less area, speed of the circuit, low power and low cost. In order to achieve these requirements, simple process, small area, small signal swings and low voltage circuits are needed. Most of these goals can be obtained from improving process technology, such as shrinking devices. The static CMOS design style is adopted in almost all digital applications. Such a wide spread diffusion is mainly due to its robustness and the negligible static power consumption. There are the specific requirements which cannot be fulfilled by static CMOS.

The advances in semiconductor technology have led to the integration of high performance digital and analog circuits on the same silicon substrate. The CMOS logic style does not provide an analog friendly environment due to the large switching noise. CMOS circuits suffer from simultaneous switching noise (SSN), a significant source of on-chip noise.

However, low-power high-speed processors will require new circuit techniques, than by just improving process technology. The current mode Logic (CML) is a popular logic style for high-speed circuits. This type of logic was first implemented using bipolar transistors and extended for application with MOS transistors.

A logic style that is becoming increasingly popular is MOS Current Mode Logic (MCML). This technique could be used to realize high-speed circuits. MCML has large static consumption due to its constant operation current. Its high-speed switching and reduced output voltage swing contribute to its high-performance. MCML having low switching noise because it's adapted in the mixed signal ICs to avoid the degradation of resolution. The advantage of this technique is that their speed and power consumption can be simply adjusted by altering the bias current of the gates without the need for resizing the devices. The near constant current of MCML produces significantly less on-chip simultaneous switching noise.

This technique exhibits better power delay than the traditional CMOS logic style at high frequencies. MCML is preferred for mixed analogue-digital signal environments in order to reduce the digital interferences between the analogue and digital blocks. MCML architecture provide higher immunity to supply noise due to their differential structure, lower cross talk due to the reduced output voltage swing and lower noise generated due to the constant current flowing through the supply rails. Power dissipation of MCML circuits is much larger than the conventional CMOS at low operating frequency.

2. MCML OPERATING PRINCIPLE

The MCML gate consists of four main blocks, (i.e) the logic function block, current source Ics, power switch, and the load resistors RL. Differential pair of NMOS transistors is used to implement the logic function. Depending on the complexity of the function levels, the NMOS transistors have to be stacked one upon the other to implement the logic function. The constant tail current Iss is provided by using a current source. This current will be switched based on the logic function to one of the output branch, which finally reach voltage level (Vdd-IssRd), which corresponds to logic '0' due to the entire current flowing through the load resistor. The other output will stay at logic '1'.The operation is elaborate in the next section. During *sleep* mode the power switch is used to cut the current, which will force both the outputs to logic '1', since there will be no current in the output branch.

In this MCML circuit, the design parameters include the voltage gain, total power dissipation, circuit delay and voltage swing. These parameters can be controlled by the variables such as bias current, current source transistor size, differential pull-down network transistor sizes, and the current source bias voltage.

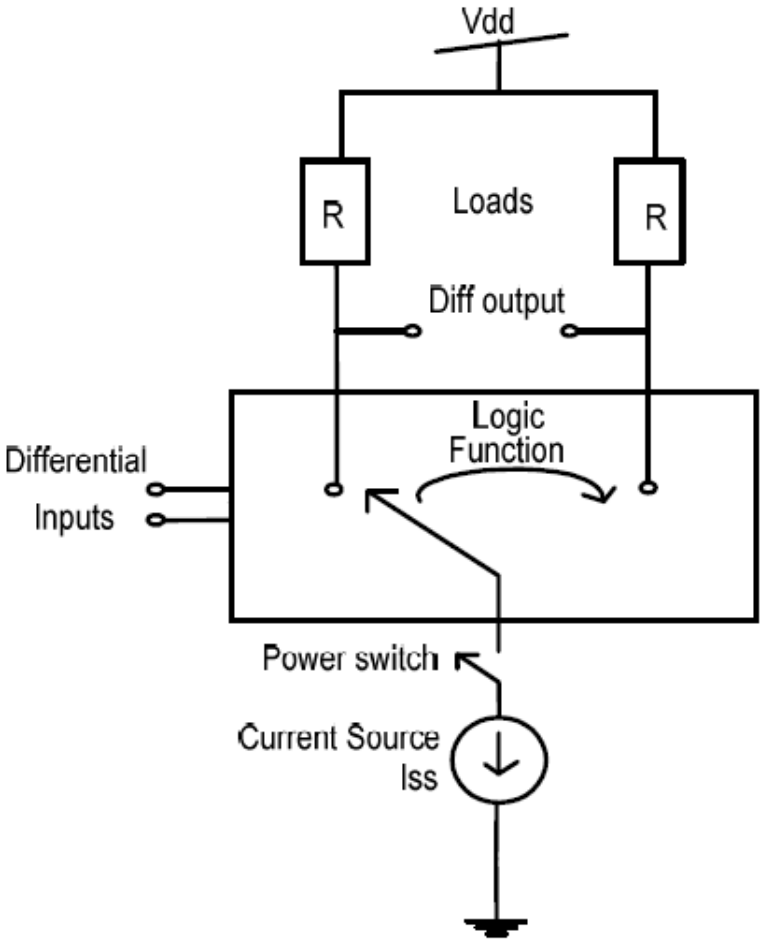

Figure 1. Basic MCML logic circuit

3. SURVEY ON DIFFERENT IMPLEMENTATION OF MCML LOGIC

A.K. Tripathy et al (2013) implementing the crypto-processors for enhanced security of electronic data. It is used to determine the power of the different circuits. In this paper biasing of sleep transistors using pass gate transistor is proposed. It uses pass gate transistor for power gating the circuits. The power variation of the proposed circuits is compared against the standard CMOS. For DPA circuits the MCML logic is proposed. Based on the power the security key is fixed for the individual circuits. 180nm CMOS technology is used in this method.

Alessandro Cevrero et al (2011) is proposed the power gated MCML. This technique is mainly designed for embedded systems which have to be robust against power analysis attacks.. The PG-MCML is used to reduce the power of the circuit. In this method, the sleep transistors are inserted in every cell. In this power gating technique which reduces the static power consumption of a digital circuit by inserting power switches in the supply path. Coarse-grain power gating and fine-grain power gating have been proposed. 90nm CMOS technology is used in this method. In this

method fine grain power gating technique is implemented in MCML logic. Insertion of sleep transistors does not reduces the performances of the MCML cell is proved. The PG-MCML consumes three times less power than the CMOS. It does not introduce the negative effect on robustness against power analysis attacks. The important goal of this method is minimizing the power, cost and battery life.

Yangbo Wu et al (2013)is developed the power gating technique. It is used to reduce the standby power of the near-threshold MCML. 45nm technology is used in this method. Using this method adder and mod-10 counter are designed and simulated to verify the effectiveness and validation. The sleeping control cell is used to control the gate bias voltage of the current source to implement in sleep mode. The results shows the larger standby power consumption saving can be achieved and the performance is also not affected.

Jianping Hu et al (2013) is developed the standard cells of the high-speed low-power MCML circuits with near threshold computing. Near-threshold computing for MCML circuits is investigated by scaling down the supply voltage. The result shows that the power consumption of MCML circuits that operate on near-threshold regions can be reduced without performance degrading. The layout simulation is done for the basic logic gates. 45nm technology is used in this method. The layout result shows that the MCML basic gates can save more energy and better performance.

Kirti Gupta et al 2013 are proposed the low-voltage MOS current mode logic. The proposed low-voltage MCML D-latch is analyzed based on two factors such as power efficient and high-speed, and the performance is compared with the traditional MCML D-latch for each design cases. Based on the transistor sizes, the bias current and the voltage swing are used to express the delay value so it can be trade off with the power consumption. TMSU 0.18µm CMOS technology is used in this method. The delay value is also measured in this method, and the delay has lesser compared to the CMOS technology.

Yavuz DELICAN et al (2011) are developed the high-performance 8-bit mux based multiplier design using Mos Current Mode Logic (MCML). Multiplier based algorithm is used to get the high performance circuit. Transistor size is reduced in this method. The area of the circuit is also reduced in this method. UMC 0.18µm CMOS technology is used in this method. The main advantage of this circuit is the absence of the power supply current spikes which makes the circuit.

Alexander Shapiro et al (2014) are proposed the MOS current mode logic near threshold circuits (NTC). A 14nm Fin Field Effect Transistor technology is used in this method. The MCML logic and NTC are combined in this method. The combination of NTC with MCML is used to reduce the leakage power level. In this method the MCML gate had differential in nature because of this nature it requires a smaller voltage swing at the output, which is used to reduce the gate delay. The MCML technology provides enhanced speed, but consumes a constant high power. The speed of the NTC is increased due to the high speed nature of MCML technology. This technique has more power efficient than the standard CMOS.

Masayuki Mizuno et al (1996) is designed a GHz MOS adaptive pipeline technique using MOS current mode logic (MCML). This paper describes about the adaptive pipeline (APL) technique. This is the new pipeline scheme capable of

compensate for device-parameter deviations and for operating environment variations. This technique is used for compensate for operating environment variation. 0.4µm MOS technology is used this method. The MCML logic circuits used in the APL technique, based on the control ports the propagation delay time can be varied. The MCML circuits as well as APL technique is used to increase the die size of the chip.

Ni Haiyan et al (2012) is addressed the method of high-speed low-power sequential logic MCML. The layout implementation is presented in this method. NCSU FreePDK 45nm technology is used in this method. The mod-10 counter based on the circuit is designed and the efficiency of the circuit is verified. The d-latch is designed in this method.

Marko Aleksic et al (2008) is analyzed the occurrence jitter of nonautonomous MOS current-mode logic circuits. This method is used to transform the noise signal into jitter. Jitter generation is characterized with its system function in the frequency domain and impulse response function in the time domain. Linear time-variant process is used to model the jitter generation. They estimate the jitter of a CML frequency divider flicker device noise and white noise. It is used to identify the main jitter contributors in the circuit. They analyze jitter due to determine the ground noise in a CML buffer. The conclusion of this method illustrates the suppressing deterministic noise sources for low jitter performance.

Massimo Alioto et al (2006) are proposed the design of High-speed power-efficient MOS current mode logic (MCML) static frequency dividers. 0.18µm CMOS technology is used in this method. Because of its simplicity, it can be used in a pencil-and-paper approach, avoiding time-consuming trial-and-error approach based on the simulations. The analytical approach is used to understand the power-delay tradeoff in the design. An analytical strategy is proposed to size the bias current in the stages of a static frequency divider to achieve a high speed performance. The overall power consumption is reduced because in every successive stages the bias current is scaled.

Dr.Luqman Sufer Ali et al (2012) are done the comparison between MOS Current Mode Logic (MCML) and Complementary Metal Oxide Semiconductor (CMOS) circuits operating in low power application. MCML logic circuits had a minimum delay and the power delay product is also reduced compared with the CMOS circuits. 0.18µm technology is used in this method. MCML logic circuits reveal high efficiency and good performance at low power and high speeds. The gain of the circuits has been compared in this method. The MCML circuits had larger gain than the CMOS circuits. In MCML circuit cross talk must be avoided because of its low switching noise. Based on the comparison the MCML circuits are having the better performance.

Venkat Srinivasan et al (2004) presented three digital multiplier architectures capable of operating in the gigahertz range, based on the MOS Current Mode Logic (MCML). TMSC 0.18µm CMOS technology is used in this method. Different 8-bit MCML binary-tree multiplier architectures are designed and compare the performance in terms of latency, throughput, area, power dissipation and power consumption. The Ripple Carry Adder is designed in this method. This RCA is used to design a gigahertz range multiplier. The ability to build logic gates that operate at high speed, while dissipating relatively small power, makes MOS current mode logic

(MCML) a promising technique for designing gigahertz-range arithmetic circuits. To enhance the throughput, they pipelined our multipliers by inserting a register stage after every compressor cell.

Hong li et al (2012) designed a basic single-rail MOS Current Mode Logic (SRMCML) circuits. SMIC 130nm CMOS technology is used in this method. The power dissipation of the basic SRMCML cells are compared with the conventional dual-rail MCML. The power dissipation of the proposed SRMCML circuit is almost the same as the conventional dual-rail. The SRMCML circuit can attain smaller power delay product than dual-rail MCML.

Lisha Li et al (2005) are proposed the CMOS Current Mode Logic gates for high speed application. TMSC 0.25µm technology is used in this method. Phase detector has been designed in this method. The main application of the proposed block is illustrated in a typical mixed-signal circuit, the high-speed phase locked loop for a phase detector with good speed improvement over conventional CMOS logic. The proposed gates may be easily integrated with conventional CMOS logic with minimal interface.

Ravindar Kumar et al (2012) proposed 6T SRAM cells using MCML technology which will reduce the leakage power in SRAM cell and it will control the sub-threshold current. 45 nm technologies are used in this method. MCML technology is the best technology because it reduces the power dissipation. Because of the insertion of MCML logic gives the lower power dissipation. The static power dissipation is also reduced in this method.

Ayman H.Ismail et al (2004) are derived the oscillation frequency of MOS current mode logic (MCML) based ring oscillators. The cycle to cycle factor jitter of MCML ring oscillators is also discussed. MCML ring oscillators are compared of identical MCML inverters cascaded together. The delay of a single MCML inverter has been derived. MCML ring oscillators is devised that leads to minimum power dissipation of the oscillator designed for a given oscillation frequency and jitter. It can be designed to satisfy the speed requirements at arbitrary power dissipation. Power dissipation of the circuit is reduced. MCML ring oscillator consumes less power. Static power dissipation of the circuit is reduced because of its low voltage.

E.PATTANAIK et al (2013) are analyzed the MCML 8-bit multiplier for high speed application. 0.6µm CMOS technology is used in this method. The main purpose is to recommend high-speed operation that can optimize the throughput. The main advantage is speed in current mode operation.

4. CONCLUSION

The MCML circuit has better performance compared to the CMOS circuits. Based on the following parameters the performance of the circuit is measured.

1. MCML is preferred for mixed analogue-digital signal environments in order to reduce the digital interferences between the analogue and digital blocks.
2. MCML architecture provide higher immunity to supply noise due to their differential structure, lower cross talk due to the reduced output voltage swing

and lower noise generated due to the constant current flowing through the supply rails.

3. Power dissipation of MCML circuits is much larger than the conventional CMOS at low operating frequency.
4. The advantage of this technique is that their speed and power consumption can be simply adjusted by altering the bias current of the gates without the need for resizing the devices.

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