International Journal of Applied Engineering Research
ISSN 0973-4562 Volume 10, Number 4 (2015) pp. 10707-10718

http://www.ripublication.com

High Throughput and Low Power Reconfigurable DAB/DAB+ Architecture using On-Chip Vector Transition Coding

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Abstract

Digital audio broadcasting technology (DAB) is the modern digital radio technology designed for fixed and notably for mobile receivers. DAB+ is the enhanced version of DAB and provides better audio quality. The proposed system explains the design of power-efficient high throughput multimedia DAB/DAB+ processor and is implemented in Cyclone III of FPGA family. Maximum likelihood Viterbi decoder using finite state machines is used here to minimize both static and dynamic power and to provide high signal-to-noise ratio (SNR). The I/O power can also be minimized by reducing the switching activity of system level buses and higher throughput can be achieved. The experimental results are demonstrated and analyzed using Modelsim and Quartus II of Altera 6.4a. MATLAB Simulink tool is used to compute SNR, which provides the reliable communication of the system.

Keywords— Digital audio broadcasting (DAB), maximum likelihood Viterbi decoder, signal to noise ratio (SNR), switching activity.

I. INTRODUCTION

In today's digital world, the radio broadcasting technology has been evolved and is being grown tremendously. Digital audio broadcasting (DAB) technology, also termed as a Digital Radio, used by several countries which replaces existing AM and FM technologies. DAB+ is the enhanced version of DAB. The several advantages over conventional broadcasting are that it provides high spectrum efficiency by employing single frequency networks (SFN), provides superior audio quality and it is

pertinent to mobile reception.

Generally there are two types of coding in a digital communication system, they are source coding and channel coding. In order to obtain efficient communication in DAB/DAB+ systems, source coding techniques can be utilized. It aims to reduce the information as much as possible by removing the unnecessary bits and superior sound quality is achieved. All communication channels are prone to errors and to obtain reliable communication in DAB/DAB+ systems, channel coding techniques can be applied. Here redundancy bits are appended and channel noise can be reduced at the receiver end.

DAB system has preferred MPEG1- Layer II (MP2) as its audio coding standard. To optimize the coding efficiency in band-limited applications, high-efficiency advanced audio coding version 2 (HE-AAC V2) audio coding standard has been designed and added to DAB systems hence forms DAB+ systems. HE-AAC V2 architecture includes advanced audio coding (AAC) low complexity (LC) profile, parametric stereo (PS) and spectrum band replication (SBR) technologies. There exists a trade-off between bit rate and performance parameter of PS and SBR technologies. Since PS and SBR technologies are used for low bit rate programs, its performance gets decreased as bit rate increases. Due to the disadvantages of PS and SBR technologies, AAC-LC is used in DAB+ system. Hence, for the enhancement of the digitization process, MP2 and AAC-LC are used to design DAB/DAB+ audio decoder in compatible DAB/DAB+ system.

Finite state transition convolution encoder with Viterbi decoder and embedded transition inversion (ETI) coder has been used for our proposed design. The AAC-LC decoder [1] is complex and comprises of bit stream demultiplexer, inverse quantizer, synthesis filter and many decoders such as Huffman, M/S decoder, PNS decoder, IS decoder and TNS decoder. It consumes more power and area and moreover, in Huffman coder, the encoded bits are of variable length, i.e., the decoder does not know whether the last bit has been received and it is time consuming than other techniques. These drawbacks have been overcome in the proposed system. The signal to noise ratio (SNR) is used to describe the reliable communication of DAB/DAB+ systems and is achieved using forward error correction (FEC). FEC is a combination of Convolutional and Viterbi decoding, which improves the capacity of the channel. The major issue in the current VLSI design is power consumption. It can be reduced by decreasing the switching activity for random binary data which is performed by ETI coder.

The rest of this paper is framed as follows. Some of the coding techniques of audio have been reviewed in Section II. In Section III, a reconfigurable DAB/DAB+ architecture using on-chip vector transition coding is described. In Section IV, the simulation results and analysis of the parameters have been made. The inference of the paper has been given in Section V.

II. RELATED WORK

The coding techniques of audio are classified into two groups, in this section a brief analysis on the type of audio coding is discussed.

The first category is [1] [2] [3] and [4] describes the source coding techniques. For many types of multimedia services, the usage of perceptual audio coding (PAC) has been increased. For compressing the digital audio, the irrelevant information is removed in the PAC. Some of the issues are, when encoders of low bit rate used are, temporal masking issue and the fundamental issues introduced by quantization and coding blocks. In [2], the author J Herre has discussed the approaches to overcome it. In order to obtain high coding efficiency and audio quality at low bit rates, HE-AAC [3], also called AAC+, has been designed. It includes AAC-LC profile and SBR technology. To further optimize the coding efficiency in bandwidth limited applications, HE-AAC v2 [4] is designed. It comprises both AAC+ and PS technologies and provides better robustness compared to other standards. To provide high quality for portable applications, an MPEG-2/MPEG-4 AAC-LC audio codec [11] is presented. Optimization features such as low power and low cost are achieved by considering memory and calculation units. In mobile multimedia systems, this audio codec can be embedded because it has a simple interface. The computations of the AAC decoder is optimized in the inverse quantization block by analyzing the quantized spectrum samples [12]. It can be used in portable DAB+ receivers by achieving good audio quality and low power consumption. Wang et al in [1], low cost and low power decoder which is flexible to both DAB and DAB+ is designed. To provide high stereo quality and to overcome the complexities of utilizing SBR and PS technologies, AAC-LC profile is used. For the enhancement of the digitization process, MP2 and AAC-LC are used to design DAB/DAB+ audio decoder. Quality alone is examined in this first classification, but the data efficiency is not considered.

Another classification depends on the channel coding techniques. To provide data efficiency, the extra bits are appended before transmitting it to the channel. The enhanced processing efficiency is obtained in MPEG 2 [8] by utilizing a new method for Huffman decoding. Comparatively it requires less space for AAC audio codec, but it is of variable length. The efficiency is examined and validated in DAB channel decoder [5] using FPGA. During transmission, to evaluate the performance such as speed and efficiency of the system, the system parameters are varied. Gao et al in [6] designed the ASIC for DAB systems which is used to estimate the transmitted data by decoding the punctured codes. The power dissipation is reduced by using low power traceback approach. In this paper [13] convolutional encoding along with Viterbi decoding is designed and implemented to provide efficiency and reliability to communication systems. It is realized using Matlab by considering parameters such as code rate ½ and constraint length 3. Even though the data efficiency is obtained, in order to obtain low power dissipation the switching activity should be reduced. To minimize transitions in block of data transfer [14] encoding technique is utilized. It checks for number of transitions if it exceeds then the transition states are inverted and uses extra word instead of extra line to indicate the inversion. This leads to transition reduction and power consumption. It is also used for detecting the errors. The extra bit used in the transition inversion coding (TIC) scheme is eliminated in the ETI scheme [15]. The bit inversion can be indicated by using the phase difference which is obtained from the clock and data. Here Hogge phase decoder is used to decode the data and hence low power and area are achieved. The extra indication bit,

which is used to indicate whether there has been a transition, increases the overhead. In order to avoid the overhead, ETI coding [9] is proposed which uses the phase difference to indicate the inversion occurrence.

III. PROPOSED SYSTEM

The proposed system describes the design and implementation of high throughput and low power reconfigurable DAB/DAB+ architecture using on-chip vector transition coding. The procedure is as follows, the random binary data is encoded using convolution encoder and ETI encoder; then the encoded data is passed through the noisy channel and finally to recover the original data, the received symbols are decoded using ETI decoder and maximum likelihood path decoder. In order to achieve error free data, convolution encoder with Viterbi decoder is used.

All communication channels are prone to errors and hence to improve the communication efficiency forward error correction (FEC) method is used. FEC is most widely used in digital and multimedia applications and it is used for controlling the errors that occur during transmission of data bits over the channel. Viterbi decoder along with convolutional coding is one of the FEC methods used as error correction codes. High throughput and low power are achieved by employing ETI coder in this proposed design.

The transmitter section of the DAB/DAB+ system is depicted in fig. 1. The salient concept is that the incoming audio signal from streaming media and the microphone is converted into bits and is convoluted with the impulse response of the convolution encoder which is explained in Section A. The incoming stream of data is first divided into blocks, encoded, and then transmitted. During the training mode, FSM calculates the frequency threshold which is considered as the normal frequency level of the input audio. If the incoming audio signal has a frequency at in the range or out of range, then FSM cut off is exceeded. Then to reduce the switching activity of the random data, ETI encoder is used, explained in Section B, where high throughput and low power is achieved. The ETI encoded bits are converted into an analog signal and transmitted through the channel. Matrix interleaver is used here in order to ignore from burst errors.

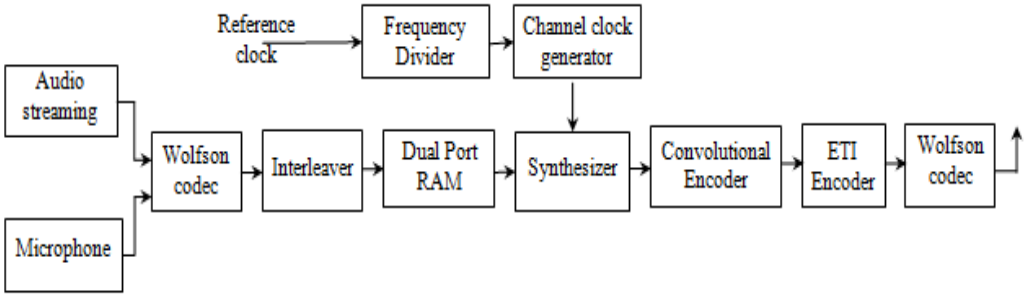

Fig. 1 Transmitter Architecture

The receiver section of the DAB/DAB+ system is depicted in fig. 2. The received signal is converted into bits and ETI decoder decodes received data based on the phase difference. Thus, it reduces the power consumption and high throughput is achieved. There is a possibility of error in the received sequence because the channel is prone to errors. To recover the original data, maximum likelihood path Viterbi decoder is used and the concept is explained in Section C. Thus, high SNR is achieved when compared to existing systems.

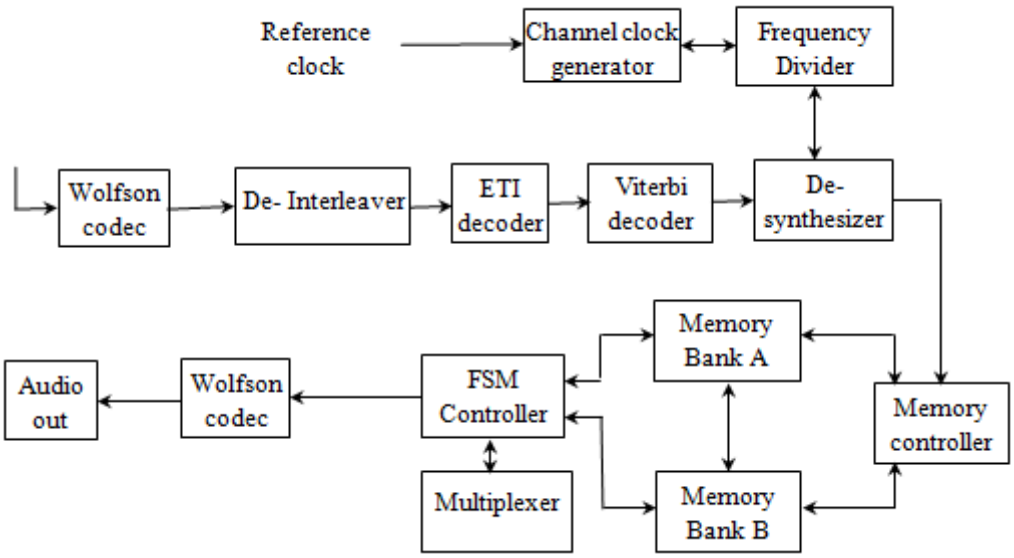

Fig. 2 Receiver Architecture

A. Convolution encoder

Convolution encoder is one of the error correcting coders, used to generate parity symbols to the input data stream. Fig. 3 depicts the implementation of Convolutional encoding using shift registers. A sequence of data bits, u is considered and is divided into k data symbols $d_k = (d_k^{(0)},.., d_k^{(k-1)})$. The encoder sequentially maps the data symbols on coded symbols $x_k = (x_k^{(0)},..., x_k^{(\eta-1)})$ of η bits. The code rate is one of the parameters used to describe the extent of redundancy and is given by $R = k/\eta$. The encoder consists of shift registers M which is used to find number of states, 2^M states and is characterized by $S^{(m)}$ with $m = 0, ..., 2^M - 1$.

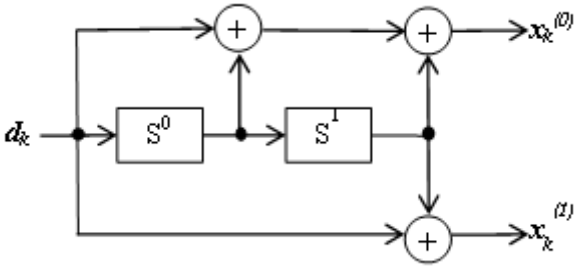

Fig. 3 Convolution Encoder

In the proposed system, convolution encoder is a finite state machine (FSM). It is designed with trellis diagram instead of using shifters and adders [7]. All possible state transitions are depicted in the trellis diagram fig. 4, where input 0 is represented by solid edges d_k = 0 and input 1 is represented in dash edges d_k = 1. Therefore, convolution encoder is a 2^M FSM.

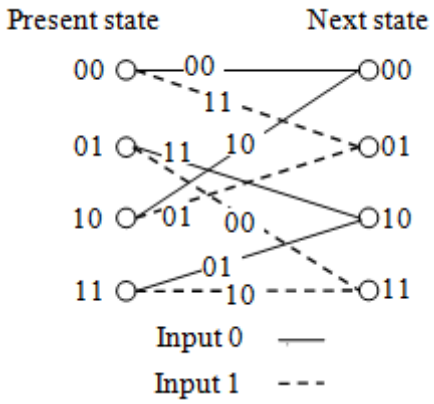

Fig. 4 Part of Trellis diagram

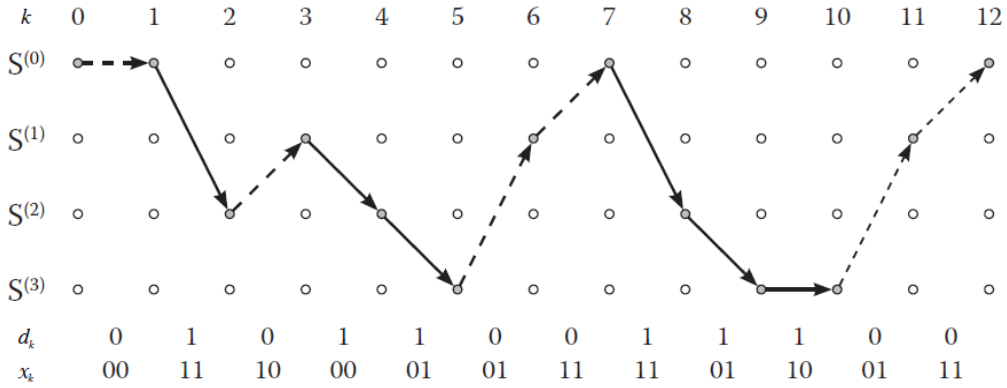

Fig. 5 Trellis diagram for exemplary information sequence

Suppose the input sequence d_k = (0, 1, 0, 1, 1, 0, 0, 1, 1, 1, 0, 0) is encoded using trellis diagram, the encoded output sequence x_k = (00 11 10 00 01 01 11 11 01 10 01 11) is achieved and is illustrated in the fig. 5. Hence, to achieve high throughput in DAB/DAB+ systems ½ bit rate encoder is designed.

B. ETI Coder

In order to decrease the switching activity of the random data, TIC is used. It reduces the transition between the bits by inverting it, which in turn reduces the power dissipation. To minimize transitions in block of data transfer [14] encoding technique is utilized. It checks for number of transitions if it exceeds then the transition states

are inverted and uses extra word instead of extra line to indicate the inversion. This leads to transition reduction and power consumption. It is also used for detecting the errors. The extra bit used in the transition TIC scheme is eliminated in ETI scheme [15]. The bit inversion can be indicated by using the phase difference which is obtained from the clock and data. Here Hogge phase decoder is used to decode the data and hence low power and area are achieved. The only disadvantage is that the extra bit is required to know whether there is an inversion or not and it increases the switching activity. In the proposed system, ETI coder [9] is used to overcome the issues in TIC. ETI scheme eliminates the transition indication bit by employing the phase difference between clock and data, i.e., the phase difference occurs only when there is an inversion in the data. ETI encoder is used at the transmitted side and is depicted in the fig. 6 and ETI decoder is used at the receiver side to decode the receiver bits.

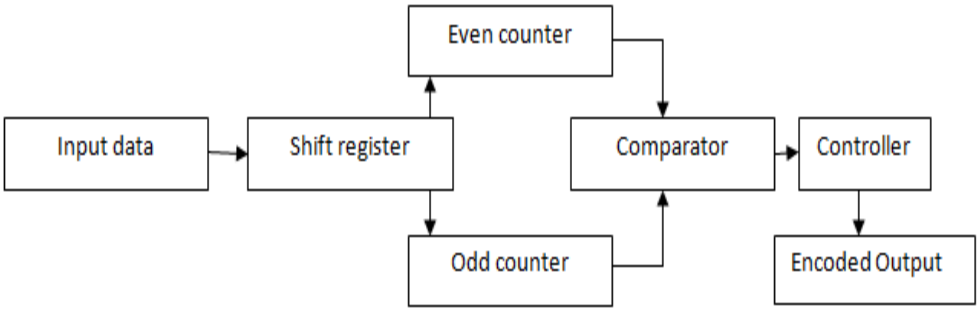

Fig. 6 ETI encoder for proposed system

The ETI encoder module is our proposed design which encodes transmitting signal based on number of zeroes and ones. It defines the data to be inverted based on zeroes and ones. It consists of internal modules such as shift register, even counter, odd counter, comparator, and inverter. The ETI decoder decodes the received data by considering two bits. Decoding should be inverse process of odd invert, even invert, full invert, and on invert.

C. Viterbi decoder

Viterbi decoder (VD) along with convolutional coding is one of the FEC method used as error correction codes. VD is used to estimate the transmitted data, where there is a high chance of getting corrupted mainly through AWGN when transmitted through the channel.

In the proposed approach, the VA is executed using maximum likelihood (ML) path decoding. ML decoding technique is used to find the most likely transmitted code branch, where hamming distances are computed for each branch. The end to end calculation cannot be executed in all available paths and hence complexity arises. To overcome it, VA is implemented using ML decoding which rejects the path that is least likely to be transmitted.

Since the communication channel is prone to errors, there might be a chance to get encoded bits corrupted which in turn reduces the efficiency of the system. For example, consider the encoded message x_k is corrupted; the received sequence will be different from transmitted sequence which is depicted in the fig. 7.

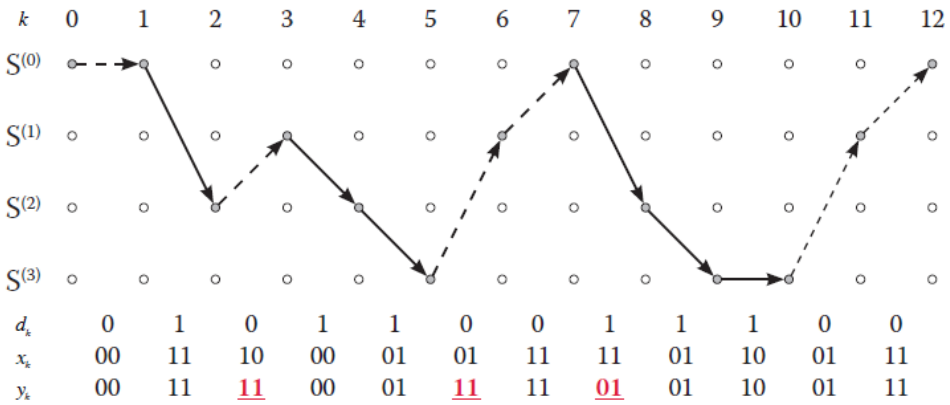

Fig. 7 Received message with bit errors

The received error sequence can be recovered from errors by implementing the VA using ML decoding. It consists of functional units; they are branch metric unit (BMU), add-compare-select unit (ACSU), survivor memory unit (SMU) and trace back unit (TBU). Their functional operation [10] is explained in the below-mentioned steps:

Step 1: The received symbols are given to VD as its input and Hamming distance, i.e., number of bits of received symbol is different from the potentially received symbol, are calculated for each branch.

Step 2: For each stage *k*, the path metric is calculated by cumulating all the branch metrics in the path till stages *k-1*. ACSU module performs its operation by comparing the metrics of the path recursively and selects the smallest metric as survivor till the last symbol is decoded and those values are stored in SMU.

Step 3: Now the TBU selects the survivor paths by tracing back and the original data bits are found based on the values of the survivor path.

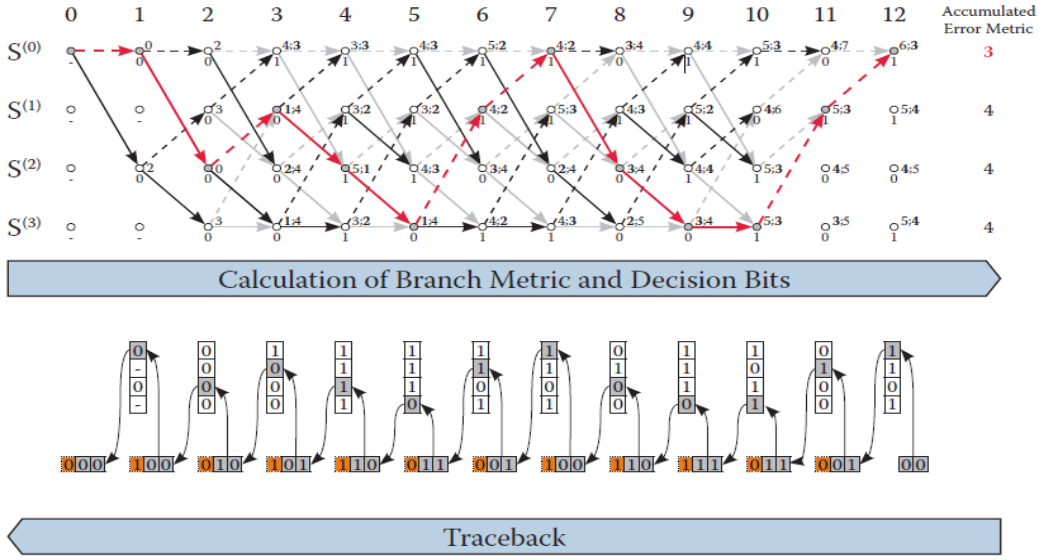

Fig. 8 Trace back of survivor path

The lowest acquired error metrics are stored in the shift register and the traceback is initialized. The order of the output bits is in reverse manner and hence specific instructions are required to restore the original order of the symbols.

By implementing VA using ML decoding, the original data symbols can be recovered from the errors and is illustrated in fig. 8. Thus, the errorless data can be achieved using VD in DAB/DAB+ system.

IV. RESULT AND ANALYSIS

Fig. 9 shows the simulation waveform of reconfigurable DAB/DAB+ architecture using on-chip vector transition coding with the help of ModelSim Altera 6.4a. It also depicts that the efficient output audio signal of a DAB/DAB+ system is achieved and is analyzed using FPGA family CYCLONE III and device EP3C16F484C6.

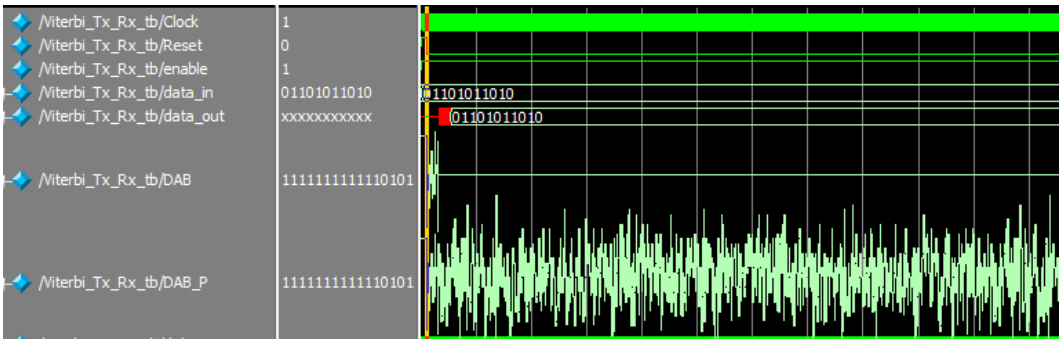

Fig. 9 Simulation waveform

Table I depicts the signal-to-noise ratio of the existing and proposed system. It can be inferred that the proposed reconfigurable architecture has 23.5967dB and 32.0537 for DAB and DAB+ system respectively and shows that it is comparatively 10% more efficient than the existing system.

Table 1 Signal to Noise Ratio (SNR) (dB) of existing and proposed system

SNR (dB)	Existing system (dB)	Proposed system (dB)
DAB system	21.2	23.5967
DAB+ system	28.6	32.0537

Throughput Analysis

Throughput evaluates the efficiency of the DAB/DAB+ system. Table II depicts the design of area efficient, high throughput DAB/DAB+ system. It is designed using a single chip based on system-on-chip design in Verilog hardware description language (HDL). The proposed system provides faster communication and supports multimedia rate audio input and also to reduce the design complexity compared to existing system [1]. The data transfer rate is 3.30 GigaBytes per second (Gbps) and hence high throughput is achieved.

TABLE II Throughput Analysis

Coder	Existing system	Proposed system
Throughput (Gbps)	1.82	3.30

Power Analysis

Power is now a major concern in the current VLSI design. Hence, the proposed approach reduces the power dissipation for reconfigurable DAB/DAB+ architecture. The total power dissipation is subdivided into static and dynamic power dissipation. Static power dissipation prevails when there is no any activity in the circuit and dynamic power dissipation prevails during the transient state condition. Table III shows the power dissipation of the existing and proposed system. Due to reduced switching transient activity by the ETI coder the total power dissipation is 62.85 mW.

TABLE III Power Analysis

Coder	Existing system	Proposed system
Dynamic power dissipation (mW)	88.75	2.17
Static power dissipation (mW)	46.35	46.18
I/O power dissipation (mW)	35.32	14.49
Total power dissipation (mW)	170.42	62.85

V. CONCLUSION

In this paper, the power-efficient high throughput, reliable multimedia DAB/DAB+ processor is designed. Simulation results and analysis shows that the maximum likelihood Viterbi decoder using finite state machine is used to provide reliable communication and is 10% more efficient than the existing system. The power reduction is obtained by minimizing the transient switching activity. High throughput of about 3.30 Gbps is achieved here, which is depicted in Table II. By ignoring the issues of DAB and DAB+ standards, the proposed reconfigurable DAB/DAB+ architecture will obviously provide simplicity to digital radio industry.

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