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Wideband Inductorless Balun-LNA using 0.13 Micrometer CMOS Technology

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Abstract

The wideband low noise amplifier (LNA) for multi-standard radio application is proposed. The Common gate (CG)-common source (CS) based balun topology is used. Noise and distortion cancellation property of CG-CS topology is utilized to get noise and power efficient design. The design emphasizes on low power dissipation for low power applications. The design uses 0.13 micrometer process CMOS technology, which operates from 0.2 to 2 GHz from 1.2 V supply. The Balun-LNA design provides 7.37 dB maximum gain, 3.78 dB minimum noise figure, -10 dB input matching and -8 dB output matching with only 4 mW power dissipation.

Keywords— **Balun, LNA, CG-CS Balun-LNA, Noise Figure, CMOS Technology.**

I. INTRODUCTION

The emerging telecom system conceives ubiquitous wireless connectivity that supports multiple radio standards across multiple frequency bands and features re-configurability for agile service switching and adaptive power consumption. Multi-standard radio receivers have drawn attention because future communication devices have to support multiple standards and features on a single chip [1]. This type of radio requires multiple narrowband low-noise amplifiers (LNAs) or a wideband LNA that covers multiple frequency bands. A single wideband LNA shared among different standards is preferred to save power and reduce complexity. Such an LNA should achieve good impedance matching, high gain, and low noise figure (NF) across a wide frequency band. The conventional solution employs several LC-tuned LNAs to cover a dedicated small band over the desired frequency span [2]. The other extreme is a wideband LNA [3] with more flexibility and better efficiency in terms of form factor, cost, and power, but its performance must be comparable to or even better than narrowband tuned LNAs due to concurrent reception of unfiltered multi-standard signals.

Recently evolved scaled CMOS technologies demonstrated high-performance LNAs with low cost. LNAs with on-chip inductors occupy a large area. Although inductors resonant with parasitic capacitors lead to higher gain and better NF, the lack of accurate inductor modeling complicates the circuit design, resulting in possible trial-and-error tape-outs. Off-chip inductors have higher values than on-chip inductors. However, they increase the cost and reduce the yield. Thus, employing an inductorless LNA becomes an attractive choice for many low-cost applications.

A balanced and symmetrical architecture is favored over an unbalanced one due to its robustness to substrate noise and power-supply. When differential (balanced) signaling in the receive chain is adopted, second-order distortion in the receive chain is significantly reduced. Single-to-differential circuitry is required in the receiver because antennas and RF filters typically produce single-ended input/output (I/O) [4]. Passive components have been used to implement the single-to-differential conversion, but this solution is usually bulky and therefore not suitable for integrated circuits [5]. A passive-balun is lossy and narrowband so that several components dedicated to each frequency band are required for wideband operation, leading to higher costs. Current RF systems with high-sensitivity requirements demand high-performance baluns that have low loss and small area. An active-balun fulfills these requirements very well since it provides sufficiently high power gain and low noise over a wideband. Also it shows good performance in power supply rejection, output balancing, and linearity, especially without a pre-filtering stage. Several topologies exist presently, which are: 1) a single transistor with common-source (CS) and common-drain (source follower) outputs [6]; 2) a differential pair with a single input ac grounded [7]; and 3) CS and CG pair [8]–[10].

This paper has proposed wideband inductorless balun-LNA based on CG-CS topology. Previous studies used either noisy bias resistor [8] or a noiseless bulky inductor [10] which causes noise and headroom issues. Also passive device used as a current source suffers from process, voltage, and temperature (PVT) variations, in contrast with the stable operation, if a bias scheme based on current mirror is employed. The proposed current-mirror biasing with a PVT insensitive current source (or sink) presents strong immunity to process and temperature variations. The proposed architecture employing negative feedback features lower power and achieves better bandwidth with minimal noise due to the active bias current source.

This paper is organized as follows. Section II describes the proposed wideband balun-LNA and Section III presents simulation results, and concluding remarks are given in Section IV.

II. PROPOSED WIDEBAND BALUN-LNA

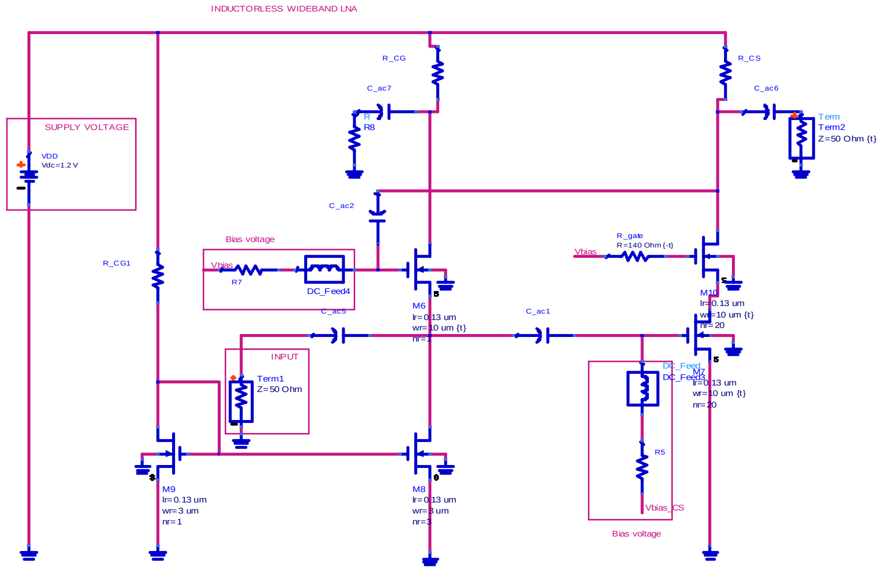

Fig. 1. **Proposed schematic of wideband inductorless balun-LNA.**

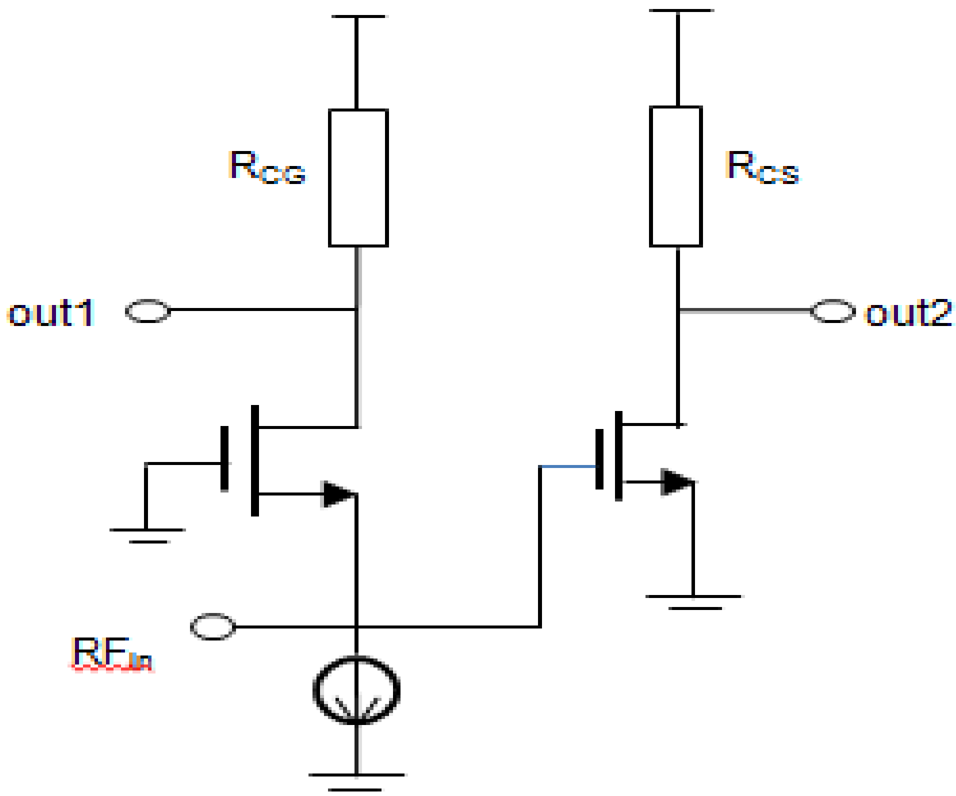

Fig. 2. **Active balun CG–CS topology.**

The proposed balun-LNA architecture shown in figure 1 is realized using CG-CS topology. Figure 2 shows CG-CS topology [8]-[10] where RF input is given to gate of one transistor and to source of other transistor. The gate terminal of CG transistor and source of CS transistor are grounded and are cascoded. This is a well-known architecture which have at least 15 to 20 year old reference [11, 12]. However, all these past references use CG-CS devices with same size and bias. By changing the device parameters in CG-CS structure, it shows better performance as shown in section III. This topology has wideband matching, noise and distortion cancellation property.

The proposed design has negative feedback arrangement. The negative feedback is proposed for low power consumption. The feedback is given from CS stage transistor to gate of CG transistor to boost the trans-conductance of CG transistor. Therefore the required trans-conductance is reduce which result in reduction in device size and power consumption. Also negative feedback has advantage of noise suppression of CG stage bias transistor due to reduced current demand of CG transistor by current mirror bias transistor. To minimize current noise source, we have to increase voltage headroom. So there is tradeoff between noise figure and supply voltage requirement. Both parameters cannot be optimized at same time. Previous studies use either noisy resistor bias with large resistance to minimize noise at the expense of higher voltage headroom or use noiseless or area inefficient inductors.

A. ***Balun operation***

In common gate stage, relation between voltage gain ($A_{V,CG}$) and input impedance ($R_{in,CG}$) is as follows

$$I_{in} = \frac{V_{out,CG}}{R_{CG}} = \frac{V_{in} . A_{V,CG}}{R_{CG}} \quad (1)$$

So, input impedance of CG stage is

$$R_{in,CG} = \frac{V_{in}}{I_{in}} = \frac{R_{CG}}{A_{V,CG}} \quad (2)$$

For ideal transistor, output resistance should be infinite. In that case, input impedance is R_{in}= 1/gm and gain equals

$$A_{V,CG} = gm . R_{CG}$$

For impedance matching at input, source resistance R_S is equals to CG stage impedance $R_{in,CG.}$ Gain of CG stage becomes

$$A_{V,CG} = R_{CG}/R_S.$$

To create balun, the gain of CS stage should be equal but with opposite sign

$$A_{V,CS} = -\ A_{V,CG} = -R_{CG}/R_S.$$

B. Noise canceling

The principle of noise cancelling is as follows. The channel noise of transistor (CG) generates a noise current which generates a noise voltage on source resistor and a large voltage anti-phase across load resistance. This input noise voltage is amplified by CS stage which is in-phase and fully correlated to noise voltage of CG stage. Thus, this noise is fully cancelled at differential output while signal contribution to output signal add to create balanced output.

The CG-CS topology is widely analyzed in [11, 12, 13 and 14]. With reference to this, noise figure and gain can be improved by trans-conductance scaling of CS and CG stage. We can reduce the noise figure by keeping the trans-conductance and load resistance of CS stage 'n' times bigger than CG stage. As we increase the trans-conductance of CS stage, gain increases but it causes increase in power dissipation of a circuit.

III. Simulation Results

The Balun-LNA was designed using TSMC (Taiwan semiconductor manufacturing company) 0.13 micrometer CMOS technology transistors. Agilent's Advanced design system tool is used to design and simulate the circuit. As balun-LNA circuit provides single ended input and differential output, a wideband off-chip balun is employed to convert the differential output to single ended output for measurement of S-parameter, stability factor and noise figure.

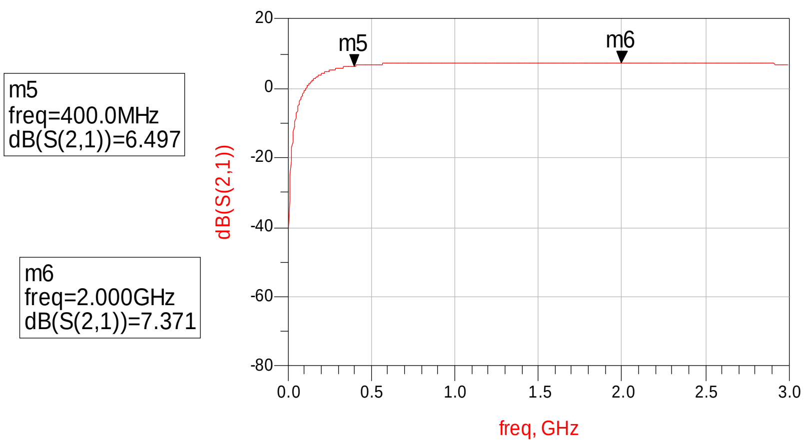

Fig. 3. Simulated gain (S21) versus frequency

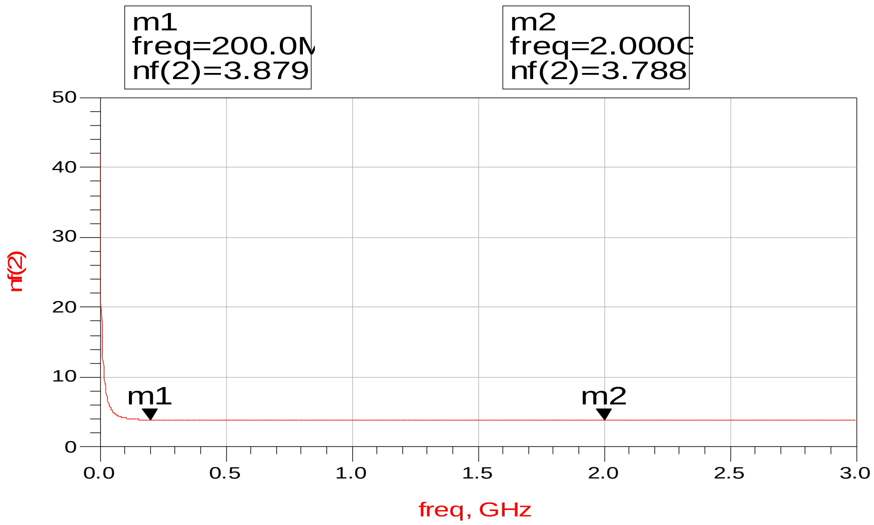

Fig. 4. Simulated noise figure versus frequency

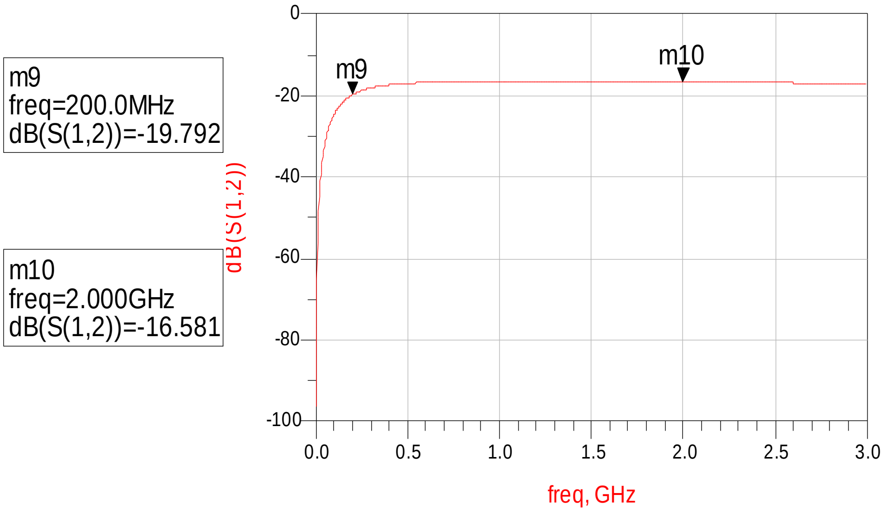

Fig. 5. Simulated Isolation (S_{12}) versus frequency

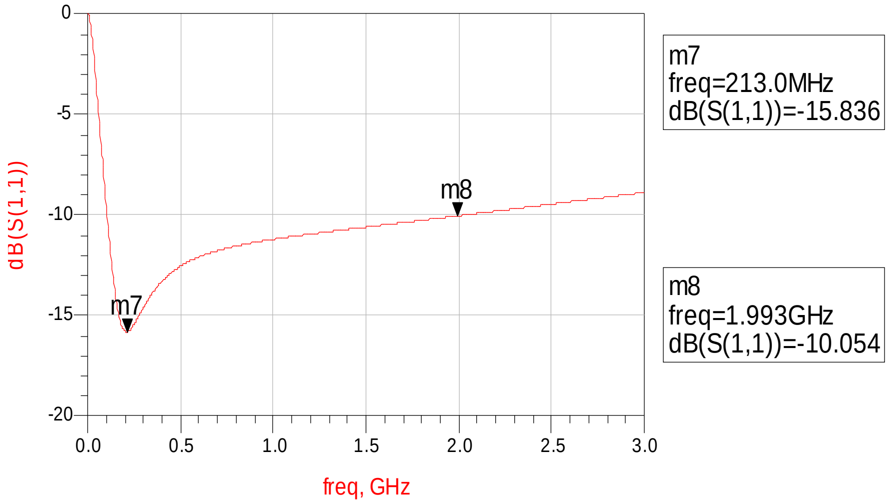

Fig. 6. Simulated Input Return loss (S_{11}) versus frequency

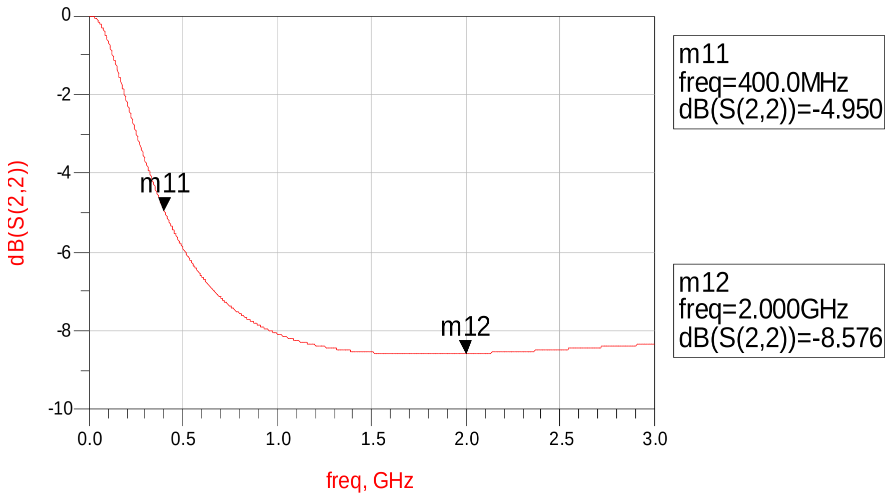

Fig. 7. Simulated Output return loss (S_{22}) versus frequency

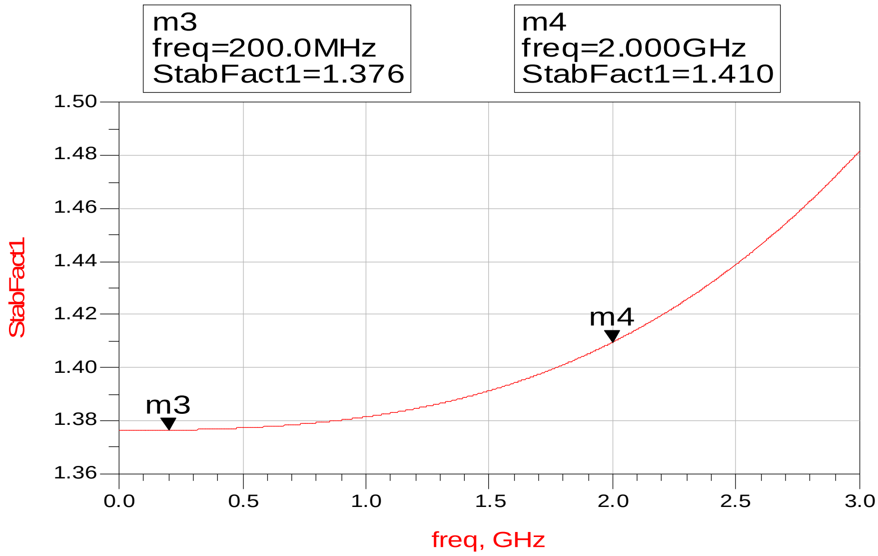

Fig. 8. Simulated Stability factor versus frequency

Simulated S-parameter results are shown in figure 3 to 8. Figure 3 shows simulated maximum power gain (S_{21}) of 7.371 dB with 3 dB bandwidth at 2 GHz and 6.49 dB at 400 MHz which is better. Figure 4 shows simulated noise figure of proposed Balun-LNA core. The maximum simulated noise figure is 3.78 dB at 2 GHz over 3 dB bandwidth which is low. Figure 5 shows simulated isolation (S_{12}) and figure 6 shows input return loss of Balun-LNA core. Within 3 dB bandwidth, simulated S_{12} is better than -15 dB and S_{11} is -10 dB which shows better input matching. Figure 7 shows simulated output return loss of -8.57 dB and Stability curve in figure 8 shows approximately 1.41 stability factor of a circuit for frequency band from 200 MHz to 2 GHz.

Conclusion

This paper has presented balun-LNA architecture and provides simulation results for its performance parameters like gain, noise figure, stability. The CG-CS balun LNA topology is use for noise and distortion cancellation. Current mirror based biasing is used for stable operation over power, voltage and temperature variations. The size of design is reduced by inductorless design. The negative feedback is applied to CG transistor for noise suppression and trans-conductance boosting which result in low power supply requirement.

Fabricated in a TSMC 0.13 micrometer RF-CMOS process technology, the LNA achieves a gain of 7.37 dB and low noise figure of 3.78 dB over 3 dB bandwidth with 1.2 V of minimum power supply. The main advantage of this design is that it dissipates only 4 mW of power. Benefiting from topology used in this paper, the proposed LNA achieves comparable and better noise figure, gain with low supply voltage without using inductors.

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