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Performance Analysis of Ring Oscillator in sub-micron CMOS Technology

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Abstract

This paper deals with the Design, Analysis and comparative study of unique stages of Ring oscillator in sub-micron CMOS technology. In this paper, CMOS oscillators are implemented as "Ring Oscillator" (RO) in 45nm CMOS technology. An RO consists of series of gain stages which are designed and implemented in Cadence Virtuoso Analog Design Environment and Analysis are performed in Cadence Spectra. In this paper, have designed CMOS RO in unique stages such as three, five, seven and nine stages and their performance metrics are tabulated. The comparative study clearly reveals five stage RO shows a better performance for many low power application, as a signal generator with a frequency of 7.8 GHz and Peak noise voltage of 310.94μV @ 203mHz.

Key Words: Oscillator, RO, LO, CMOS, VLSI, gain, Noise.

I. INTRODUCTION

Ring Oscillator is an active device which produces an indefinite and periodic output without an input. It consist of a feedback network, a negative feedback system may oscillate. It is also called as a badly-designed feedback amplifier. If the amplifier experiences the phase shift at high frequencies the feedback become positive, thus an oscillation occurs. For an oscillation to begin, a loop gain of unity or greater is necessary. A negative-feedback circuit has a loop gain which satisfies two conditions they are stated as 1) The loop gain is equal to unity in absolute magnitude 2) Phase shift around the loop is zero or an integral multiple of 2π. These conditions are named as Barkhausen criteria to which circuit will sustain steady state oscillation. It is a

necessary condition for oscillation but not the sufficient condition. The ring oscillator are most widely used integrated circuit of all. Ring oscillators are used to monitor the gate delays and speed power product of MOS inverters. A ring oscillator is a closed loop comprising odd number of identical inverters, which forms a unstable feedback network. Period of oscillation is twice the sum of the gate delay in the ring. CMOS inverter based oscillator was first used for clock recovery in an Ethernet controller.[1] the application range from clock generation in microprocessors to carrier synthesis in cellular telephone, it also become popular in random number generator and also for monitoring in communication circuits [2].

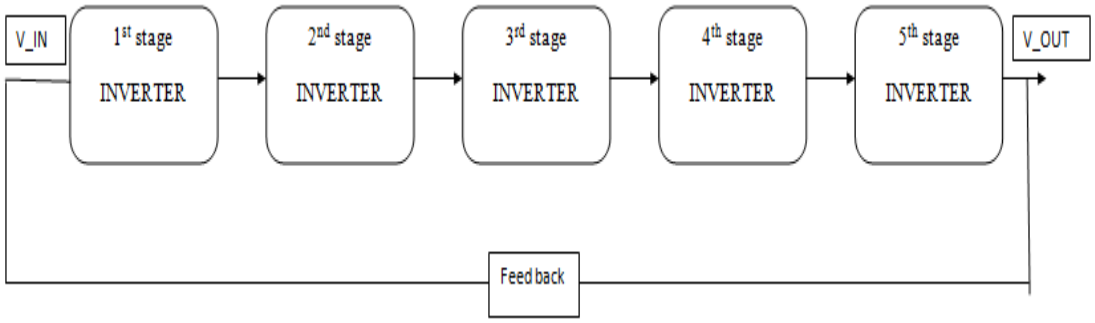

Fig 1. Block Diagram of Five stage Ring Oscillator

II. RING OSCILLATOR

Ring oscillators can attain the multiphase output. There are many methods to implement ring oscillator. we chose the most common method in this paper i.e., implementation of ring oscillator as a cascade of odd number of inverter stages, connected in a closed loop chain. Fig. 1. shows the ring oscillator employing five inverters. the Frequency of oscillation of ring oscillator is varies with number of inverter stages used in the ring structure. There must be a phase shift of 2π and unity voltage gain at the oscillation frequency to achieve sustained oscillation. In a ring oscillator with m inverter stages, a phase shift of π/m is provided by each stage. while the remaining phase of π is provided by the dc inversion. The signal undergoes m delay stages in a time of $m\tau_d$ to provide a phase shift of π and another time of $2m\tau_d$ to obtain the remaining phase of π.[1] Therefore frequency of oscillation can be given by,

$$f_o = \frac{1}{2m\tau_d} \qquad (1)$$

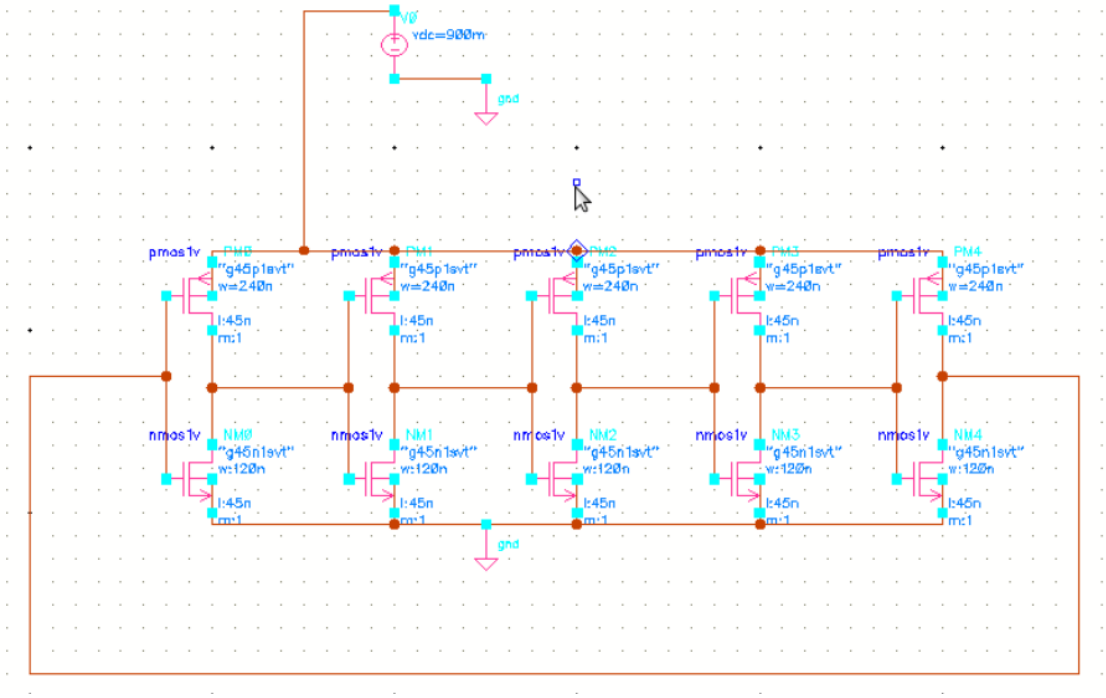

Fig 2. Five stage ring oscillator schematic in Cadence Virtuoso.

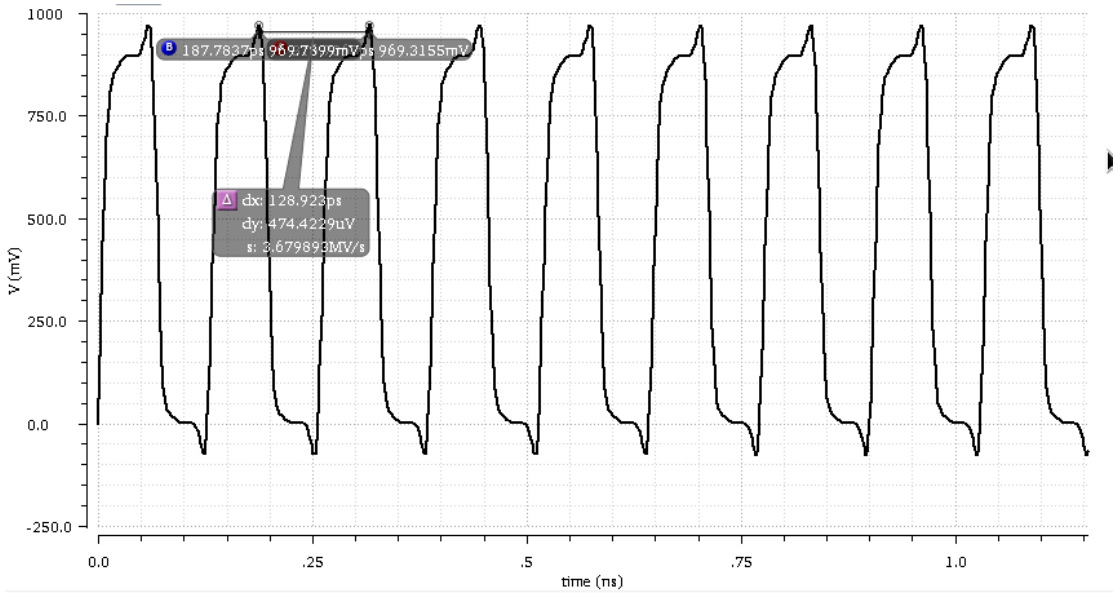

Fig 3. Transient analysis Output waveform of Five stage Ring Oscillator

III. RESULTS AND ANALYSIS

3.1 Transient analysis :

It solves the complete non-linear algebraic-differential equations of a circuit. Effects

such as non linear distortion, intermodulation, saturation, clipping and oscillations can be modeled with this analysis. In this analysis only DC component of the sources is applied to the circuit. Through transient analysis we find the time period and the frequency of the oscillation.

3.2 Power Analysis :

Power is one of the important analysis in the VLSI field, reduction of power is much necessary in day to day world. In this paper we have calculated the average power, static power, Dynamic power and leakage power.

3.2.a Average Power :

It is the rate of energy flow averaged over one full period. since there is no input for ring oscillator it is calculated in V_{dc}. It can be easily calculated in Spectra by a calculator using a formula in tool.

$$average(v(t) * i(t)) \quad (2)$$

where,

v(t) - supply voltage, i(t) - supply current

Normally, average power can be calculated using

$$P_{avg} = P_{stat} + P_{dyn} + P_{leak} \quad (3)$$

3.2.b Static Power :

Static power is calculated when circuit is powered and ideal. In MOSFET static power derives from the length of the transistor channel. It is a function of both area as well as circuit design. It can be easily annotated in the tool.

3.2.c Dynamic Power :

Dynamic power occurs whenever logic toggles from 0-1 or 1-0. It can be easily calculated by difference of static and average power.

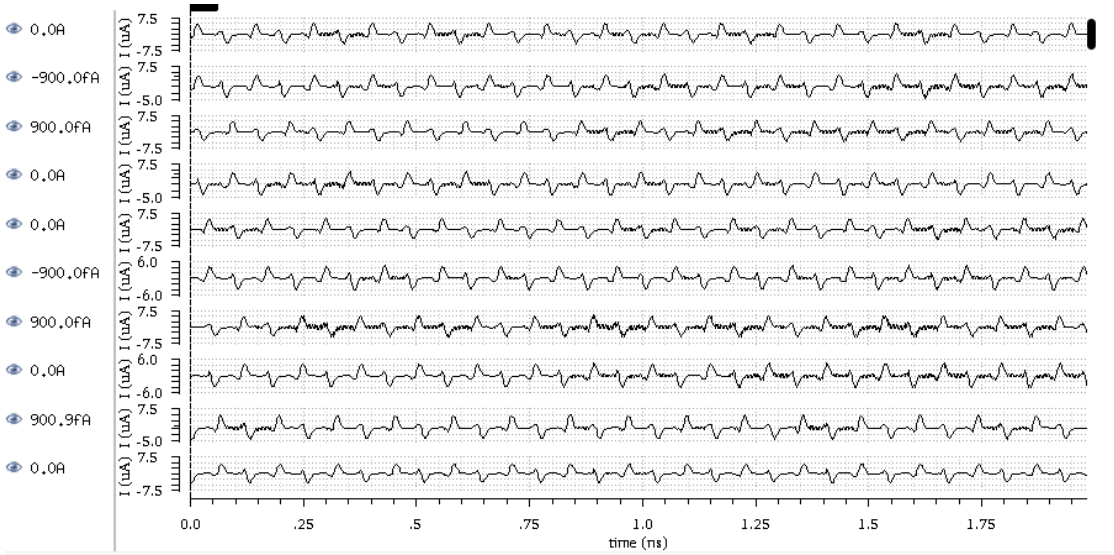

Fig 4. Transistor Leakage current output waveform for five stage RO

3.2.d Leakage Power :

Leakage power occurs when circuit is not operated. sources of leakage power are sub-threshold leakage, gate leakage, pn-junction leakage. Here in this paper we calculate the transistors leakage current. For each transistors values are given and the sum of the values gives you the total leakage current of the circuit.

3.3 Propagation Delay :

It is the time required for a signal to travel from the inputs of a logic gate to the output. this can be calculated easily using spectra.

3.4 Noise :

Noise limits the minimum signal level that a circuit can process with acceptable quality. Various noises are present in the waveform of oscillators such as jitter, phase noise. In this paper we compare the peak noise voltage in the waveform at 203 mHz.

3.5 Table 1.Design Parameters :

W_p (nm)	120
W_n (nm)	120
L (nm)	45

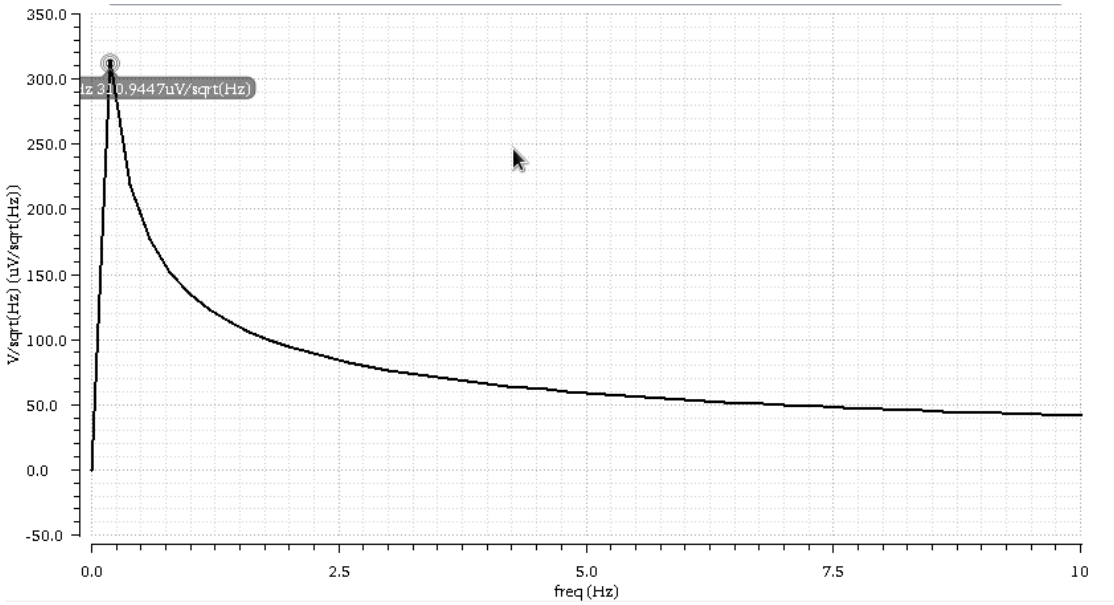

Fig 5. Noise response of Five stage ring oscillator

IV COMPARISON AND INFERENCE

Table 2. Comparison of parameters with various stages of Ring Oscillator

Parameters	Stages of Ring Oscillator			
	3	5	7	9
Time Period (s)	0.217 n	0.128n	0.073n	0.0178n
Frequency (Hz)	4.6 G	7.8 G	13.6 G	56.17 G
Average Power (W)	2.43 µ	12.3 µ	21.8 m	88.79 m
Static Power (W)	0.059 µ	1 µ	2.9 m	3.87 m
Dynamic Power (W)	2.4 µ	11.3 µ	18.9 m	84.92 m
Leakage Current (Amp)	700 f	900.9 f	1.5 µ	1.24 m
Propagation Delay (s)	51.46 p	72.87 p	48.31 n	85.67 n
Peak Noise @ 203 m Hz	64.70 nV	310.94 µV	1.21 mV	24.15 mV

In this paper we have compared the three, five, seven, nine stages of ring oscillator. Various performance parameters are there to analyze the RO, in which we have taken a few particularly noise, frequency, delay and power. We always go for odd number of stages not the even one because when we go for even number of stages the circuit exhibits positive feedback near zero frequency due to signal inversion through each stages, it simply latches up rather than oscillates. Providing negative feedback near zero frequency eliminates the problem of latch up. Differential ring oscillators can be implemented in even number of stages, it shows its flexibility. Here

in RO average loop gain is equal to unity. The number of stages in RO are determined by various requirements including speed, power, noise. Mostly Five stage provides optimum performance.[2]

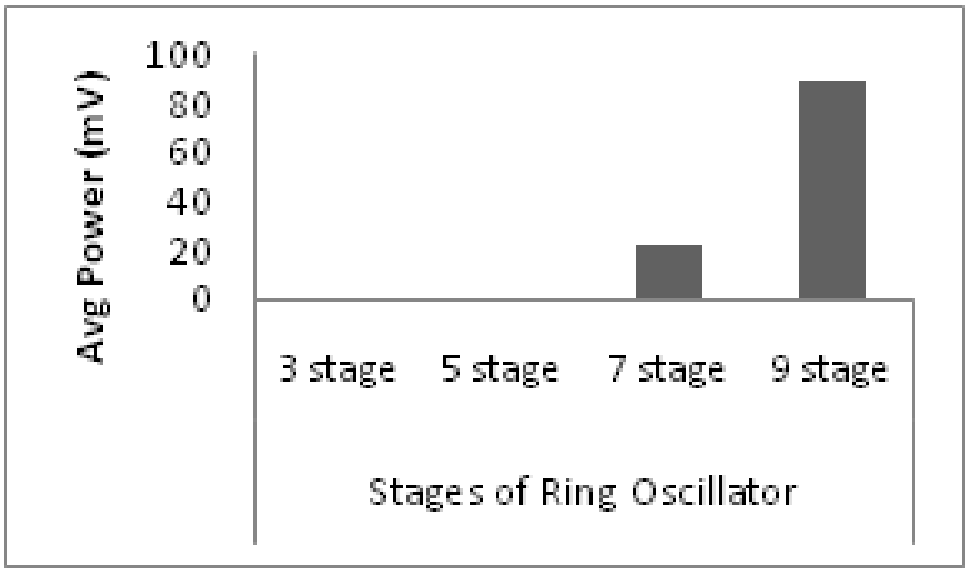

Fig 6. Comparison of average power

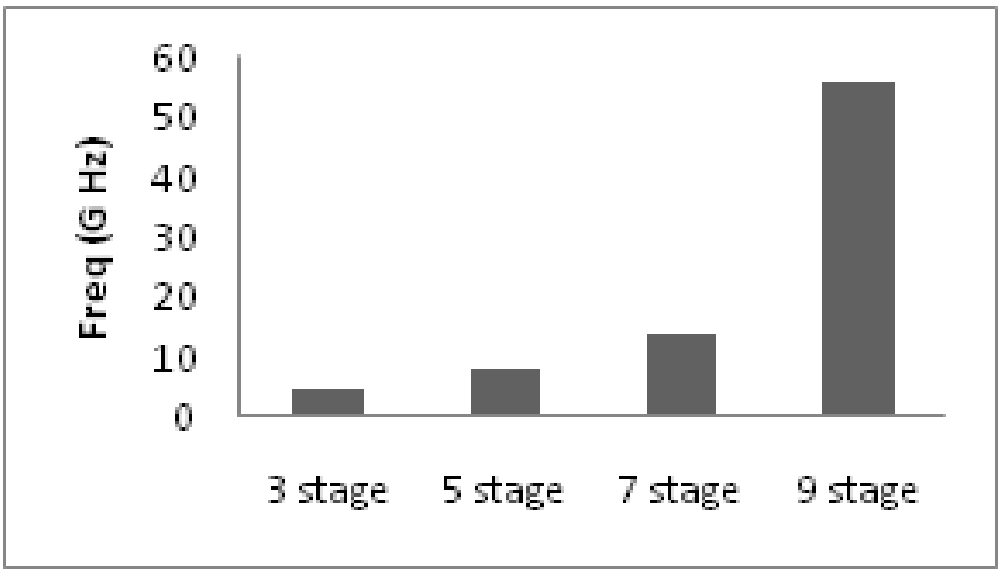

Fig 7. Comparison of Oscillator Frequency

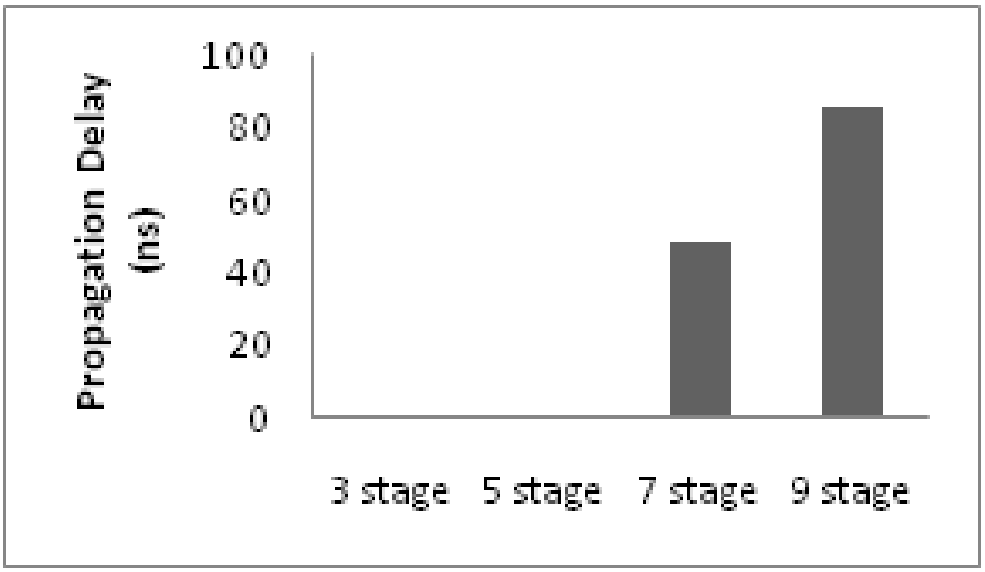

Fig 8. Comparison of Propagation Delay

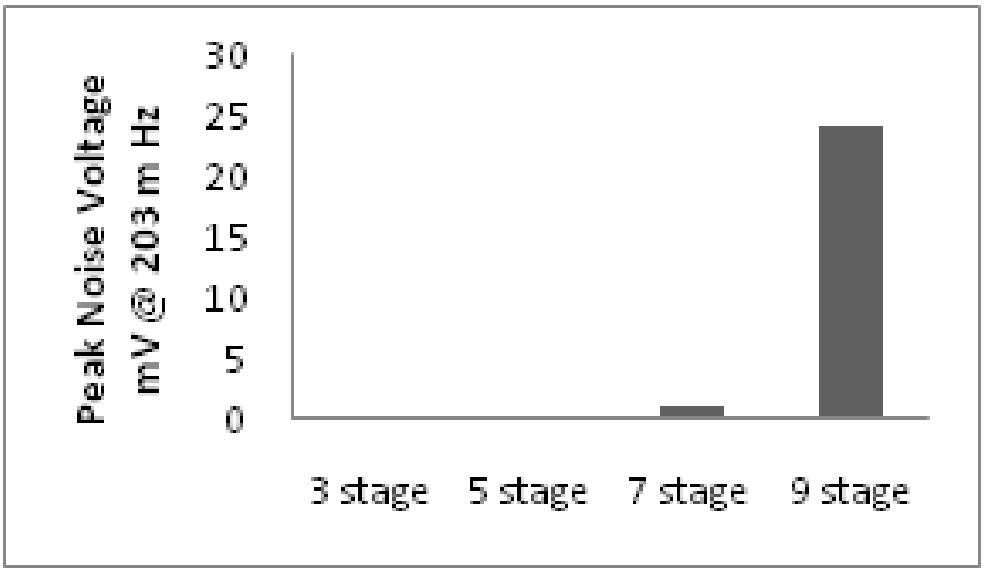

Fig 9. Comparison of Peak Noise

Power is one of the important analysis in any VLSI design. Here the supply voltage is 0.9V and the power consumption increases when the gain stages are increased. From Fig 6. it is clear that three and five stages showed they are optimum for any power saving application. When number of transistor increases the power consumed is increased. while nine stage showed with high performance in everything the five and seven stages showed that they fit best for moderate range.

While considering oscillator Frequency, each stage contribute the frequency divided phase shift of 72 degree for five stage RO and also a low frequency signal inversion, at each node the signal is 140 degree out of phase with neighboring node. The ability to generate multiple phases is a useful property of ring oscillator. From Fig 7. it is clear that the frequency is increased with number of gain stages. Thus according to the application the stages can be chosen. Here we model the oscillator by the linear feedback system. To avoid saturation loop gain should be greater than unity.

While considering Propagation Delay, the first signal after an inverter delay it forces to charge up to V_{dc} and begin to fall soon since it experiences the high input, after another delay cell it falls to zero thus it begin to oscillate, but it oscillates with the delay of T_d with consecutive node, yielding high delay when stages increases and lower when stages are less. Thus from Fig 8. three and Five stages suits for high speed application while nine stage suits for high frequency application.

While considering noise, noise response in three and five stages are neglected since its very minimum, but in nine stages its peeping out due to number of transistors. Therefore three and five stages are chosen for low noise applications. [2]

From Table2. the comparative analysis clearly reveals that three stage RO are suitable for low power wireless RF transceivers due to negligible power (2.43µ) and produces a low frequency around (4GHz). similarly nine stage RO are suitable for High Frequency (56.17GHz) application such as PLL but since five stage provides negligible power (12.3µ) and also higher frequency (7GHz) than three stage it can be widely used for low power, high and moderate frequency applications.

V. CONCLUSION

We have successfully designed and implemented various unique stages of ring oscillator in sub-micron CMOS technology. Various parameters such as delay, power, noise and frequency are compared, analyzed and results are tabulated and one can understand the overall performance of the oscillator. According to the application needed the stages of RO can be chosen, For low power, high frequency signal generators and PLL five stage RO are suitable.

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