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Graph-based Optimization of Area and Delay in Multiple Constant Multiplication

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Abstract
Serial input data is multiplied with constant pair to produce constant multiplication called Multiple Constant Multiplications (MCMs). For transposed form multiplier construction of digit serial Finite Impulse Response (FIR) filter design with a minimum number of shifting, addition/subtraction operations, graph-based algorithm is proposed in this paper. Based on the performance of area utilization and delay constraints graph-based algorithm provides better response than low complexity digit-based recoding algorithm and Common Sub-expression Elimination (CSE) algorithm. Experimental results show the efficiency of the proposed algorithm.

Keywords: FIR filter, graph-based algorithm, matlab, multiple constant multiplications.

Introduction

In signal processing applications, the impulse response of Finite Impulse Response (FIR) filter is of finite duration because it settles to zero in finite time. This means that the impulse response of an N^{th} order discrete-time FIR filter exist for N+1 samples and then settles to zero. FIR filters can operate with discrete-time or continuous-time digital and analog signals [1]. FIR filter require no feedback which means that any rounding errors are not compounded by summed iterations, and this system can be easily implemented. The same relative error occurs in each calculation and is inherently stable, since the output of the filter is sum of finite number of finite multiples of input values. The system is easily designed to be linear phase by making the coefficient sequence symmetric. This property is desired for phase sensitive applications such as data communications, crossover filters and mastering [2]. FIR filters are very much used in Digital Signal Processing (DSP) applications, because their characteristics behavior is in linear phase and the feed forward implementation is useful in building stable high-performance filters. Figure 1 and 2 illustrates the direct-form FIR filter and transposed-form FIR filter implementation respectively. Direct-form and transposed-form FIR filter have similar complexity in hardware. But because of the high performance and power efficiency transposed-form FIR filters is more used than the direct-form FIR filter.

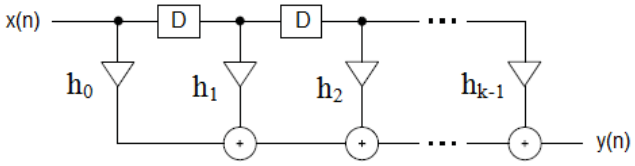

Fig. 1 Direct-form FIR Filter

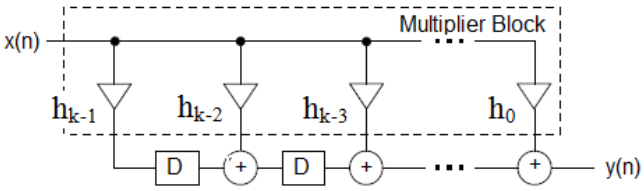

Fig. 2 Transposed-form FIR Filter

The operation of the direct-form FIR filter is described by the following equation, and the equation defines the output sequence y[n] in terms of the input sequence x[n].

$$y[n] = h_0\, x[n] + h_1\, x[n-1]$$

$$+ h_2\, x[n-2] + . + {}_{hk-1}\, x[n-k+1] \quad (1)$$

$$y[n] = \sum_{i=0}^{k-1} h_i \; x[n-i] \quad (2)$$

where, x[n] is the input signal, y[n] is the output signal, and h_i is the filter coefficient. The multiplication of filter coefficients in the multiplier block of transposed form has significant impact on the complexity and the performance of the design. This is because of the huge number of constant multiplications. The MCM is a central operation and the performance bottleneck many other systems that uses Fast Fourier Transforms (FFT), Discrete Cosine Transforms (DCT), and error-correcting codes. The following are the advantages of FIR filter over IIR filter [3].

- FIR filter is finite
- FIR filter is non-recursive
- Impulse response of FIR filter eventually reaches zero
- FIR filter is not used in classical analog filters

- FIR filter has linear phase
- FIR filter is stable
- FIR filter only depend on inputs
- FIR filter consist of only zeros

The rest of the paper is organized as follows. Section 2 reviews about the related literature on FIR filter design applied for various applications. Section 3 describes implementation of multiple constant multiplications and simulation. Finally conclusion is given in section 4.

Related Work

In this section, we review the prior work on the various design and implementation of FIR filters. Saeed et al [4] described the guidelines for a moving average filter based phase-locked loop, which can act as an ideal low-pass filter. The system is compared with different moving average filter based phase-locked loop and its tuning approach is evaluated. The control parameters are designed with two systematic methods such as proportional integral type loop filter in the phase-locked loop and using a proportional integral derivative type loop filter.

Chao et al [5] developed a dynamic soft-sensing model combining finite impulse response and support vector machine to describe dynamic and nonlinear static relationships. The model parameters are then estimated within a Bayesian framework. The evaluation result from both the simulated and the industrial case describes the superiority to conventional static models in terms of dynamic accuracy and practical applicability.

Pavel et al [6] introduced decomposition filter banks based on narrow-band linear-phase finite impulse response (FIR) filters consisting of inner and lateral FIR filters. The inner filters are optimal narrow band pass FIR filters based on isoextremal polynomials. The inner filters are supplemented by lateral narrow-band low and high pass FIR filters. This enables flexibility in the resulting frequency response of the filter bank.

Keshab et al [7] presented a low-complexity algorithm and architecture to compute power spectral density using the Welch method. The Welch algorithm provides a good estimate of the spectral power at the cost of high computational complexity. A new approach is proposed to reduce the computational complexity of the Welch power spectral density computation. The architecture not only consumes less energy compared to the original method but also reduces the latency for 8 overlapping segments.

Saha et al [8] discussed the opposition-based harmony search for the optimal design of linear phase FIR filters. The original harmony search algorithm is chosen as the parent one, and the opposition-based approach is applied. Random population is chosen during initialization and fitter one is selected as priori guess. In harmony memory, each solution passes through memory consideration rule, pitch adjustment rule, and then opposition-based re-initialization generation jumping. This gives optimum result corresponding to the least error fitness in multidimensional search space of FIR filter design.

Chia et al [9] presented a practical method for designing fixed-point FIR filters. The method takes both the filter's magnitude response and its hardware cost into consideration in the design process. The method constructs a basis set based on the fixed-point coefficients that have been synthesized already. The elements in the basis set are used to synthesize the undetermined fixed-point coefficients and the method employs some strategies to speed up the design process.

Innocent et al [10] developed and tested frequency adaptive Phasor Measurement Unit (PMU) algorithms with wider linearity range than specified in IEEE std C37.118-1, with three different concepts encompassing robust state-of-the art design approaches like FIR bandpass filtering, extended Kalman filtering, and discrete Fourier transform demodulation with FIR low pass smoothing. FIR-based PMU are linear phase with no overshoot in either phase or amplitude step responses and the extended Kalman filtering PMU is more computer-intensive but allows for a reduced group delay and better out-of-band interference rejection at the cost of a phase step response with overshoot.

Herrick et al [11] presented a stable inversion of non-minimum phase systems with highly efficient computation for high-sampling rate applications. The stable filter that inverts the dynamics of a non-minimum system is based on cascading a stable pole-zero cancellation Infinite Impulse Response (IIR) filter with a high-order Finite Impulse Response (FIR) filter which inverts the unstable zero dynamics. The high-order FIR is realized based on efficient IIR filter implementation introduced by Powell and Chau then later modified by Kurosu.

Fernando et al [12] developed a real-time, digital algorithm for PWM with distortion-free baseband. The algorithm not only eliminates the intrinsic baseband distortion of digital PWM but also avoids the appearance of side-band components of the carrier in the baseband even for low switching frequencies. The algorithm uses several FIR filters and a few multiplications and additions and is implemented in real time on a standard DSP.

Wail [13] presented a stable explicit depth wavefield extrapolation using sparse frequency-space (*f*-*x*) FIR digital filter. The ideal impulse response of the wavefield extrapolation filter is nonsparse in nature, and designing such filters was formulated as an L_1-norm minimization that is convex with a quadratic constraint. Sparse filters were obtained by employing hard thresholding to the filter coefficients magnitude. The method is used to design high accuracy sparse extrapolation filters.

Felipe et al [14] proposed an efficient estimator of optimal memory for discrete-time FIR filters in state-space. The crucial property is to measure and filter the output that involved with no reference and noise statistics. Testing by the two-state polynomial model has shown a very good correspondence with predicted values.

Kwang-Jin et al [15] proposed a theory of harmonic filters and their mathematical models applicable to periodically time varying systems perturbed by a large periodic signal. The harmonic filters are based on a series of finite time delay and weighted sum operations, which allow selection or rejection of an input fundamental tone and/or its harmonics in a periodic manner.

Multiple Constant Multiplications

MCM is used to produce constant multiplication in Digital Signal Processing (DSP) systems, Multiple Input Multiple Output (MIMO) systems, error correcting codes, frequency multiplication, graphics and control applications. In these applications full fledge usage of multipliers are not required because the coefficients are constant to produce constant multiplication. Once the MCM architecture is constructed, MCM can be called and used as many times as required. Constant multiplication either can be done by digit parallel design or digit serial design. Digit parallel design of constant multiplier needs external wire for shifting and requires more area while implementation takes place in FPGA or any other ASIC. Digit serial design overcomes area constrain with acceptable delay timing. Multiplication with constant is called constant multiplication and the process is used in filter operation. There are two types of constant multiplication; Single Constant Multiplication (SCM) and Multiple Constant Multiplication (MCM). Input is multiplied with single specific coefficient to produce SCM. Canonical Signed Digit (CSD) number representation is used to implement SCM multipliers. Input is multiplied with multiple numbers of specific coefficients to produce multiple outputs called MCM. In this multiplication is a process of shifting and addition operation. Constant multiplier consists of number of adder, subtractor and shifter according to the coefficient pair.

FIR filter output can be obtained by multiplication of input and impulse response. Multiplication operation takes place in multiplier block. The transposed-form multiplier blocks in FIR filter are replaced by MCM architecture. FIR filter gives guaranteed feed forward, stable and linear phase response. FIR filter impulse response is equal to the number of coefficients and is not in Infinite Impulse Response (IIR) filters. Hence this FIR filter implementation is sometimes called as multiplier less digit based recoding method. The objective is to eliminate the multiplier block and introduce MCM architecture in digit serial FIR filter for the reduction of multiplication. This is implemented in the form of shift and adds operations as shown in figure 3.

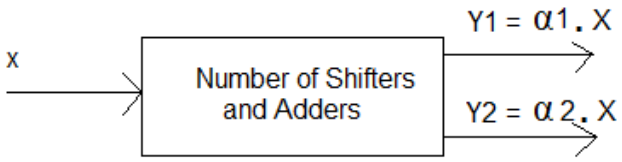

Fig. 3 MCM Operation

In the MCM operation, the input is represented by X, the filter coefficients of two outputs Y1 and Y2 are represented by α1 and α2 respectively. The operation with same input is multiplied by a set of coefficients and is said to be MCM. Here, the serial input data is multiplied with two pair of coefficients and produces the outputs Y1 and Y2. The following section describes the different algorithms for MCM architecture and the algorithms are not successful in some particular operations, especially with shifting operations.

A. Digit-based Recording Algorithm

Digit-based recoding is a simple method like Canonical Signed Digit (CSD) representation and binary method representation. In binary method decomposition are generated directly from the digit representation of the constant. These methods are the fastest and the worst performing but use different number systems to yield considerably better solutions. The main advantage of digit-based recoding is the low computational cost, typically linear in the number of bits. As a consequence, these methods can be easily applied to constants with thousands of bits. Figure 4 shows that digit serial operation needs less number of delay elements such as flip-flop for addition or subtraction. In digit-serial operation, the input data is divided into *d* bits and processed serially by applying each *d*-bit data in parallel. The bit-serial and bit-parallel operation occurs when the digit size *d* is equal to 1 and equal to input data word length. The digit-serial computation is important when the bit-serial implementations cannot meet the delay requirements and the bit-parallel designs require more hardware. Thus, an optimal tradeoff between area and delay can be explored by changing the digit size *d*.

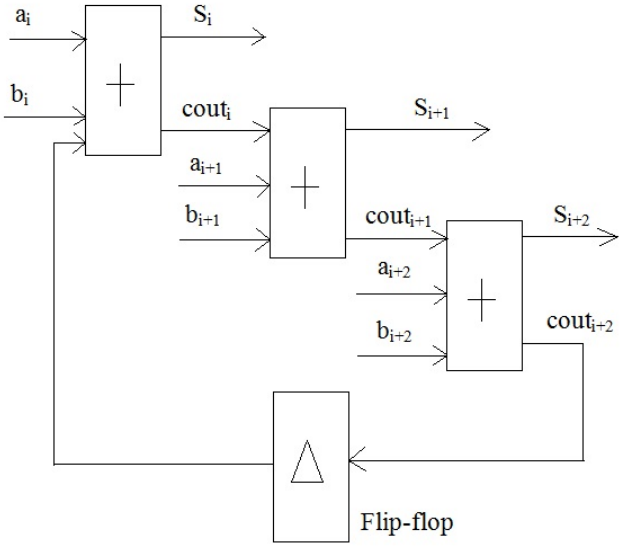

Fig. 4 Digit Serial Operation

B. CSE Algorithm

Common Sub-expression Elimination (CSE) algorithm as shown in figure 5, is the direct descendants of digit-based recoding methods. In this common sub-patterns are obtained in the representations of the constants after the constants are converted to a convenient number system such as CSD. CSE is used to minimize the complexity of the multiple constant multiplication operation. The coefficients of the multiple constant multiplications are represented using the binary signed digit number system. The binary signed digit representations of each coefficient are enumerated using the representation tree. The algorithm traverses the tree to calculate the possible sub expressions at each node. Each sub expression is used to find a possible decomposition for the

coefficient to be encoded. A complexity formula is proposed to compare the decompositions. The algorithm is designed to reduce the tree when it finds decomposition with minimum complexity. This reduces the search space while minimizing the hardware complexity. The disadvantage is that the performance of this algorithm depends on the number representation.

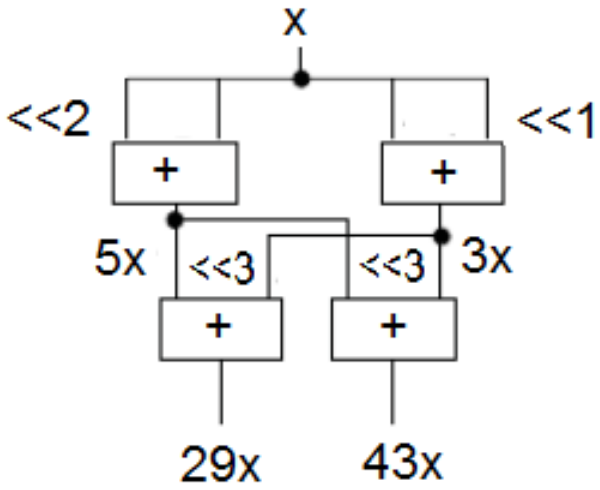

Fig. 5 CSE Algorithm

C. Graph-based Algorithm

Graph-based algorithms as shown in figure 6 are bottom-up methods that iteratively construct the graph representing the multiplier block. The graph construction is guided by a heuristic that determines the next graph vertex to add to the graph. Graph-based algorithms offer more degrees of freedom by not being restricted to a particular representation of the coefficients, or a predefined graph topology and produce solutions with the lowest number of operations. The graph-based algorithm finds a solution with the minimum number of operations by the sharing the common partial product 7x in both multiplications. This algorithm assume the input data x is processed in parallel. In digit-serial arithmetic, the data words are divided into digit sets, consisting of *d* bits that are processed one at a time. Digit–serial operators occupy less area and are independent of the data word length. Also, digit-serial architecture offer low complexity designs when compared to bit parallel architectures.

Table 1 shows the comparison of digit-based recoding algorithm, CSE algorithm, and graph-based algorithm. From the table graph-based algorithm is an efficient technique for filter implementation.

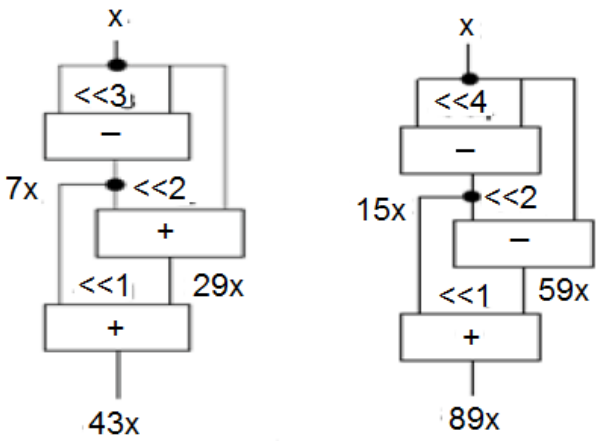

Fig. 6 Graph-based Algorithm

TABLE 1 Comparison of MCM

Sl. No.	Digit-based	CSE	Graph-based
Area (mm^2)	375	398	179
Delay (ps)	958	929	912
Power (nW)	295	315	310

Conclusion

In this paper, the formalization of designing digit-serial MCM operation with minimum area is implemented using digit-based algorithm, CSE algorithm, and graph-based algorithm. Results show that the graph-based algorithm is best and yield the optimal gate level area in digit-serial MCM design.

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