# VLSI Architecture for Impulse Noise Reduction Using Modified Decision Tree Based Denoising Method

#### S. Arul Jothi<sup>1</sup>

ECE Department, Sri Ramakrishna Engineering College Coimbatore, Tamilnadu, India. <sup>1</sup>arulbe2005@gmail. com

# Dr. N. Santhiya Kumari<sup>2</sup>

ECE Department, Knowledge institute of technology, Salem, Tamilnadu, India. <sup>2</sup>santhiyarajee@rediffmail. com

# M. Ramkumar Raja<sup>3</sup>

ECE Department, Coimbatore Institute of Engineering and technology Coimbatore, Tamilnadu, India.

<sup>3</sup>ramkumar raja@ gmail. com

#### **Abstract**

An impulse noise reduction using modified decision tree based denoising method (MDTBDM) and its VLSI architecture has been presented in this paper. The MDTBDM is used to detect and remove the impulse noise in the image and its VLSI architecture is used to achieve the goal of low cost and low complexity. Noisy pixels are identified using decision tree based impulse detector followed by adaptive median filter to reconstruct the noisy pixels. The MDTBDM method is a low cost, low complexity technique in terms of area, memory and power. The architecture takes a memory usage of 1MB less than decision tree based denoising method (DTBDM) and number of lookup table used is 169 which is 0. 18% better than the existing DTBDM, power is 0. 22W less than DTBDM. The computational complexity is less and it can be applied to many real time applications as its hardware cost is low.

**Keywords:** Very large scale integration (VLSI), image denoising, DTBDM, MDTBDM, Decision tree.

### 1 Introduction

Two main tasks of image processing are noise filtering and enhancement. During image acquisition and transmission the images are corrupted by noise which will affect the performance of image processing methods, Therefore to improve the performance efficient denoising technique is necessary for image processing methods[1], [2]. Denoising methods can be classified into two low complexity methods and high complexity methods. In low complexity method the computational complexity is low but the image quality is not good. In high complexity method the computational complexity is high but the image quality is good. The presented paper focuses only on the low complexity denoising methods for salt and pepper noise removal. I. Andreadis and G. Louverdis [3] described a adaptive median filter [AMF] and its hardware module to detect the noise in the image. An adaptive median filter followed with regularization method has been used for salt and pepper noise removal was discussed by R. H. Chan. et al [4]. P. E. Ng and K. K. Ma[5] stated a switching median filter with the boundary discriminative noise detection(BDND) for denoising the corrupted images. P.-Y. Chen and C.-Y. Lien[6] devised an algorithm for salt and pepper noise removal in which the impulse noise detector followed with edge preserving filter is used for denoising the corrupted images. Y. Dong and S. Xu[7] described a new impulse detector, which identifies the noisy pixel using the difference between the current pixel and the aligned direction of the neighborhood pixel. B. De Ville [8] demonstrated a decision tree algorithm which is used for business intelligence and data mining application. The salt and pepper noise from the corrupted images are removed using the hybrid impulse detector was described by H. H. Tsai et al [9] A. S. Awad and H. Man [10] stated a method for impulse noise removal from the corrupted images using high performance detection filter. X. Zhang and Y. Xiong [11] described a adaptive mean filter which is based on switching operation is used for impulse noise removal. S.-C. Hsia [12] devised an algorithm based on digital signal processing approach for impulse noise removal. V. Fischer[13] et al demonstrated a VLSI implementation of e video filtering scheme for computer vision applications. T. Matsubara [14] et al described about a low complexity noise removal method and its FPGA implementation. P-Y. Chen et al [15] demonstrated an edge preserving method and its VLSI implementation for impulse noise removal. C.-Yuan et al[16] described a DTBDM and its VLSI architecture for the impulse noise removal. In this view an attempt has been made for noise reduction using MDTBDM and its VLSI architecture is discussed in this paper.

# 2 Decision Tree Based Denoising Method(DTBDM)

Two components of DTBDM [16] are Decision tree based impulse detector and a filter which is used to preserve the edges of an image.

Fig. 1. shows the flow diagram of DTBDM in which the decision tree based impulse detector followed with edge preserving filter is used to identify the noisy pixel and reconstruct its value.

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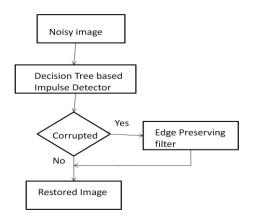


Fig. 1. Flow Diagram of DTBDM

# 2. 1 Decision Tree Based Impulse Detector

Three modules such as Isolation module(IM), Fringe module(FM) and Similarity module(SM) are used to detect the noisy pixel.

# 2. 2 Edge Preserving Filter

Fig. 2 shows the steps to filter the noise and preserve the edges of an image using edge preserving filter.

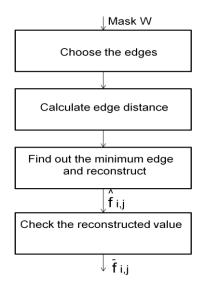


Fig. 2. Flow diagram of Edge preserving filter.

# 3 Proposed MDTBDM

Decision Tree based impulse detector[16] and adaptive median filter are the two main blocks of MDTBDM.

Fig. 3. shows the flow diagram of MDTBDM in which the noisy pixels are identified using the detector and adaptive median filter is used to reconstruct the value.

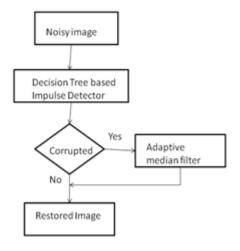
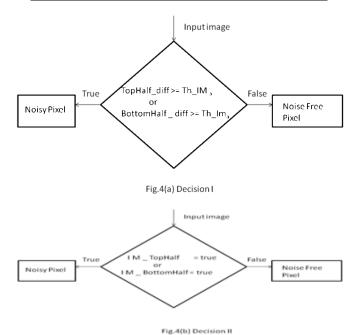


Fig. 3. Flow Diagram of MDTBDM

# **3.1 Decision Tree Based Impulse Detector Algorithm** Decision tree based impulse detector components and its output are discussed in Table. 1

Table. 1 Components and output of decision tree based impulse detector

	S. No	Components	Output		
Γ	1	Isolation Module	Decision I, Decision II		
Γ	2	Fringe Module	Decision III		
Ī	3	Similarity Module	Decision IV		



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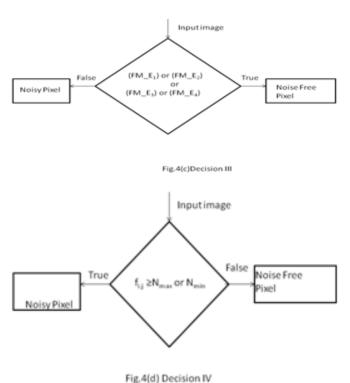


Fig. 4(a), 4(b), 4(c), 4(d) shows the output of the isolation module, Fringe module and similarity module respectively. These decisions are used to identify the noisy pixels.

# 3. 2 Adaptive Median Filter

The salt and pepper noise in the gray scale images can be filtered using the adaptive median filter. It is used to identify the existence of noise in the image and remove it using the median filter.

#### 4 VLSI Architecture of MDTBDM

#### 4. 1 Architecture

VLSI architecture for MDTBDM is shown in Fig. 5. The architecture is made up of the components such as line buffer, register bank (RB), decision-tree-based impulse detector and Adaptive mean filter.

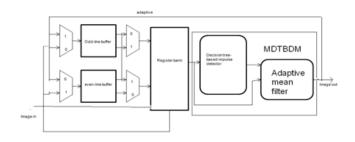


Fig. 5. VLSI Architecture of MDTBDM

#### 4. 2 Line Buffer

Pixels in the odd and even rows are stored using odd line buffer and even line buffer respectively as shown in Fig. 6

#### 4. 3 Register Bank

The nine registers in the register bank are used to store the pixel value of the current mask W. Fig. 6 shows its architecture where the series connection of three registers are used to calculate the pixel values of a row in a mask W.

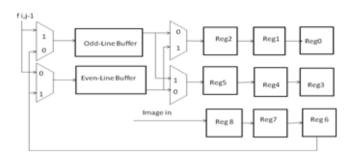


Fig. 6 Architecture of register bank in MDTBDM.

# 4. 4 Decision Tree Based Impulse detector

The three modules of decision-tree-based impulse detector is isolation module (IM), fringe module(FM), and similarity module(SM).

#### 4. 5 Isolation Module(IM)

Fig. 7 shows the components of IM.  $CMP_L$  and  $CMP_S$  are used to calculate the larger value and smaller value from the two given inputs respectively. The difference between the inputs are given using the subtractor and OR operation is done to obtain the final decision.

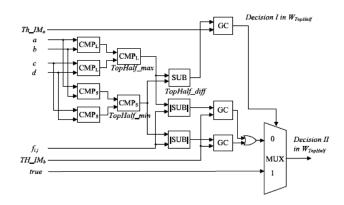


Fig. 7. Building blocks of IM

#### 4. 6 Fringe Module (FM)

The components of FM is shown in the Fig. 8. The four modules, FM\_1 to FM\_4, are used to determine the direction. This direction is used to identify the noisy pixel.

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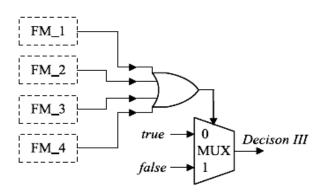


Fig. 8 Architecture of FM

# 4. 7 Similarity Module(SM)

The Fig. 9 shows the components of similarity module which will give the Decision IV output to confirm the noisy pixel.

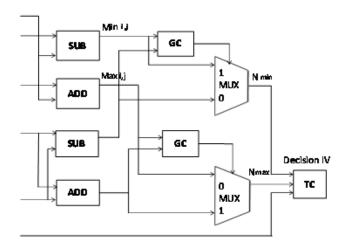


Fig. 9. Architecture of similarity module

#### 4. 8 Adaptive Median Filter

Fig. 10 shows the architecture of adaptive median filter. In this threshold value is calculated by multiplying a parameter a with a value of maximum neighbourhood pixel. The comparison is done between the centre pixel value and the threshold value, if the output is greater or lesser than the threshold value then the centre pixel value is noisy pixel. The median value of the neighbourhood pixel is taken and substituted to filter he noise. If the centre pixel value is noise free then the value is no changed and the procedure is repeated for next neighbourhood window.

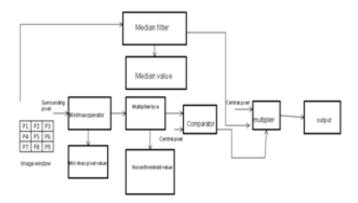


Fig. 10. Architecture of Adaptive median Filter.

#### 5. Results and Discussion

The simulation results of DTBDM and MDTBDM techniques have been implemented in MATLAB 7. 11 System Generator. It has been synthesized with Xilinx ISE Design Suite 13. 2 with Virtex 5 xc5vlx50t3ff1136. Area and power have been calculated and its values are simulated from the target device are shown in the Fig. 11 and Fig. 12. The obtained results from the similarity module for both DTBDM and MDTBDM is unity. Edge preserving filter and adaptive median filter has been used to determine its reconstructed value.

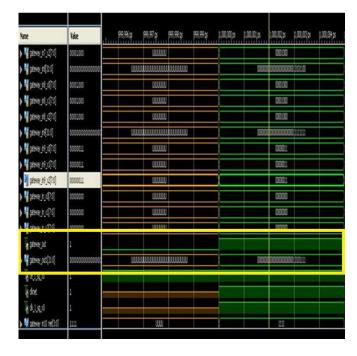


Fig. 11. Simulation Result of DTBDM



Fig. 12. Simulation Result of MDTBDM

Table. 2. Comparison of various performance parameters of DTBDM and MDTBDM

Parameters	DTBDM	MDTBDM
Memory usage	218 MB	217 MB
Minimum Time Period	2. 576 ns	2. 250 ns
Maximum frequency	388. 199	444.
	MHz	444MHz
Power	0. 639 W	0. 617 W
Number of LUTs	265	169
Number used as Logic	253	157
Number of Bonded IOBs	410	183
Average Fan-Out of Non-Clock	1. 74	1. 79
Nets		

The performance of various parameters such as area, power, frequency, memory usage of DTBDM and MDTBDM are compared and it is shown in the Table. 2. From the table it is clear that the area, memory usage and power of MDTBDM is better than DTBDM.

#### 6 Conclusion

In this paper, MDTBDM technique has been used to suppress the impulse noise in the gray scale image. Noise present in the image has been identified and filtered out using the adaptive median filter. The obtained results from the architechture designed provides better performance in terms of area, frequency and power. It have been implemented using MATLAB 7. 11 System Generator and synthesized with Xilinx ISE Design Suite 13. 2 with Virtex 5 xc5vlx50t3ff1136 as the target device. Performances of DTBDM and MDTBDM have been compared. It has been observed that MDTBDM is better than DTBDM. It has been found that the power utilized by MDTBDM architecture is 0. 617 W which is lesser than the 0. 639 W as it is obtained in DTBDM architecture. The peak memory usage of MDTBDM architecture is 217 MB

which is 1 MB less than that obtained in DTBDM architecture. Number of LUTs used in MDTBDM architecture is 169 which is very much less as compared to 265 for DTBDM architecture and the maximum frequency obtained by MDTBDM architecture is also high (444, 444 MHz).

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