International Journal of Applied Engineering Research ISSN 0973-4562 Volume 10, Number 17 (2015) pp 37668-37678

Improved Performance Dynamic Voltage Restorer with Seven level Multilevel Inverter

K.Chandrasekaran[1]
[1]*University Tunku Abdul Rahman, Kampar, Perak. Malaysia.*
[1]*E-mail: kchandra@utar.edu.my Contact no. 019-5584754*

V.K. Ramachandaramurthy[2]
[2]*Power Quality Research Group, University TenagaNasional, Malaysia*

Abstract
In this paper, a seven level cascaded multilevel inverterbased Dynamic Voltage Restorer (DVR) using multicarrier SPWM technique controller is proposed to handle deep voltage sags, swells and voltage harmonic disturbances on a threephase system.New innovative simple controller schemes based d-q theory to overcome the disadvantages of the existing controller schemes by reducing the complexity, number of signal measurements and computing time has been developed for this model. The control scheme provides ability to control the zero sequence voltage during unbalance fault period, capable to track the phase angle of the supply voltages continually and adaptivelyand low switching frequencies of the phase shift PWM which decrease the switching loss and increase the efficiency.The improved DVR is verified through extensive simulation using PSCAD/EMTDC. The DVR gives good control dynamics with minimum transient current overshoot. Good results under transient performance obtained.

Keywords: Voltage harmonics, RLC filter, Voltage sag, Multilevel H-Bridge inverter

Introduction

Electric power quality refers to maintaining at near sinusoidal power distribution bus voltage at the rated magnitude and frequency. Voltage imperfections or disturbances including voltage sags, swells, transients and voltage harmonics in a power system results in very low quality of the power delivered to the loads. Starting of induction motors in industries, energizing large capacitor banks or symmetrical and unsymmetrical faults and lightning on the power system cause voltage sags, swells and transient.As the electrical system recovers after clearing the fault, voltage swells will occur throughout the system for a short period due to redistribution of electrical energy in the network. During a voltage sag, it is not a complete outage of the network, but, however, due to insufficient energy availability, equipmentsfails, shutdown or trip. These activities cause production loss and heavy financial losses [1][2].

The distribution systems connected with numerous nonlinear loads, greatly affect the quality of power supplies. High levels of power system harmonics particularly the 5^{th} and 7^{th}will create voltage distortion, power quality problems and efficiency of machines [3][4]. Power quality disturbance is defined as the deviation of the voltage and the current from its ideal waveform.

IEEE Std519-1992 and IEEE 1159-1995 are two standards used to quantify harmonics level and voltage sag magnitude.Voltage sag range is from 10% to 90% of nominal voltage and with duration from half a cycle to 1 min and swell is defined as an increase in rms voltage or current at the power frequency for durations from 0.5 cycles to 1 min. Typical magnitudes are between 1.1 and 1.8 p.u [5].Range of voltage harmonics should be less than 5 % at the Point of Common Coupling (PCC). Custom power devices are used to protect sensitive loads against power quality disturbances[6][7]. Compared to the Static Var Compensator (SVC), the DVR is still preferred because the SVC has no ability to control active power flow [8]. DVR has a higher energy capacity compared to the Superconducting Magnetic Energy Storage (SMES) and Uninterrupted Power Supply (UPS) devices. Also, the DVR is smaller in size and cost is less compared to the DSTATCOM and other custom power devices. Ferroresonant transformers or constant voltage transformers, operate in the saturation region of their magnetizing curves [9].The ferroresonant transformer could provide output voltage during voltage sag as 30 %, 46 % and 71 %, respectively. Ferroresonant transformer is expensive and unlikely to be applied to large loads.Based on these reasons, DVR is an effective custom power device in mitigating voltage sags, swell and voltage harmonic. The DVR allows control of the real and reactive power exchange between the supply and the load. The DVR system comprises of a PWM voltage source inverter (VSI), a series injecting transformer, a control circuitry and DC source. Among the four components, the VSI is the major component of a DVR. A basic three-level VSI is realized using a full bridge configuration, in which the number of levels in the output voltage waveform is three and therefore, the amount of total harmonic distortion (THD) is very high [10][11][12][13]. With every addition of a full bridge cell to the basic configuration, the number of levels in the output increases by two, resulting improvements in THD. In this research work, a cascaded H-bridge inverter configuration with seven levels is used as VSI in DVR. The seven level configuration is compact in design, low THD level and independent connection to dc source or photovoltaic cell. The seven level provides improved quality of voltage and current with low total harmonic distortion compared to 2-level inverter.

Appropriate switching of the device cell in different levels of the VSI is crucial to obtain the proper functioning of DVR, which is achieved through multicarrier SPWM modulation techniques.

Proposed DVR Topology

Proposed topology is shown in Fig.1[14][15]. An RLC interfacing filter is at the front end between the inverter and injection transformer. Introduction of RLC filter with reduce size of the passive component improves the reference tracking performance and significantly reduces the dc voltage rating and overall rating of the VSI. A damping resistance Rf is connected in series with Lf and in parallel to Cf to damp out resonance and to provide passive damping to the overall system. A 7-level H-bridge connected inverter is used to improve the performance oftheDVR.Unliketheflyingorclampingdiodetypes,forthecascaded H-Bridge (CHB) configuration the input power is distributed among different input sources that make it more efficient. One additional advantage of the CHB inverter isthatifanydevicefailsinthe H-bridges, the inverter can still be operated at reduced power level and, hence, this configuration is fault tolerant [16].The schematic diagram of the proposed DVR is shown in Fig. 2. During a sag or swell, the control circuit of DVR injectsappropriate compensation voltage through the series injection transformer to compensate voltage imperfection across the load.Fig. 3 shows the control algorithm for swell.

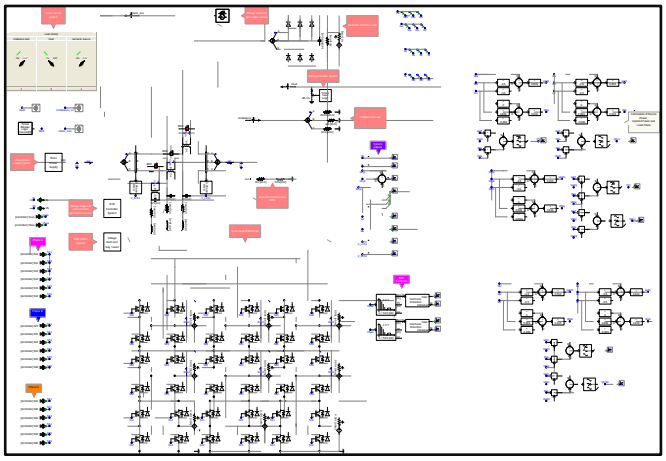

Fig 1. Proposed DVR topology

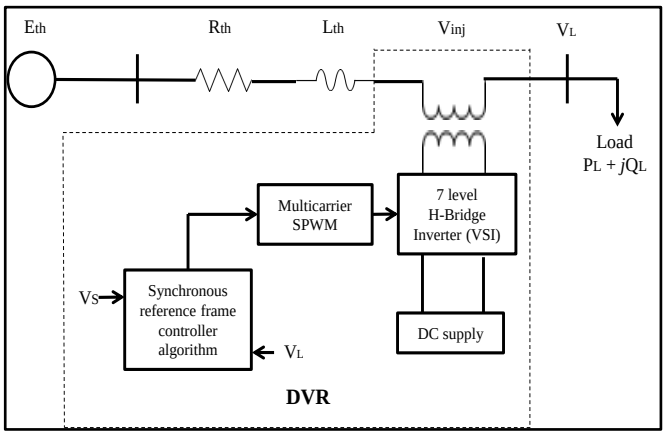

Fig. 2.The schematic diagram of theproposed DVR.

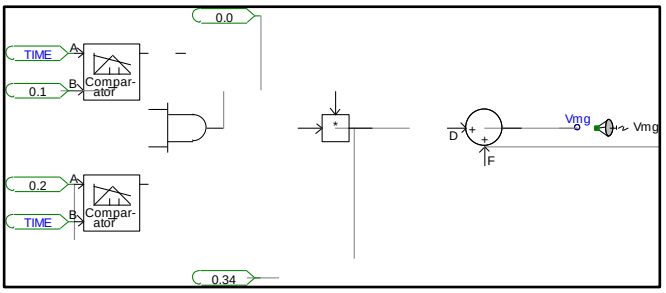

Fig. 3. Control algorithm for swell/sag.

DVR is connected to a feeder distribution system supplying sensitive load as shown in Fig.4.

The series compensator DVR is used as controlled voltage source to protect the sensitive load against voltage imperfections. The voltages Vs, PCC, V_{Load} and V_{inj} denotes for supply, point of common coupling, load voltage, and compensation voltage, respectively, while $i_s$is supply current as shown in Fig.4. The inductor L is 0.9mH acts as alow-pass filter to eliminate the high-frequency componentsof load current, and thus high-frequency harmonic voltagecomponents are filtered off.Sensitive load is 8 ohms and 0.05 mH. The proposed DVR has the following advantages [14][15]:

(a) Each phase is independently controlled.
(b) Each block of H-bridge has its own dc source such that the voltage and current rating of the components are reduced.
(c) Improved compensation capability of DVR.

In this research project, the seven-level cascade multilevel inverter topology and the multicarrier based Phase Shift Pulse Width Modulation (PSPWM) controller strategy are selected to control the DVR module. The PWM control based DVR control is fast due to switching speed of the IGBT power switches and low conduction loss [17]. The PWM technique offers simplicity and good response.

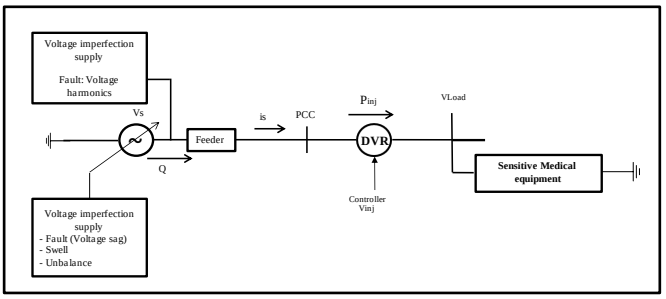

Fig. 4.Distribution system with proposed DVR.

Comparison of DVR compensation technique

Under normal operation, both the supply voltage and the load voltage magnitude are same.When voltage sag or swell occurs, the supply voltage either falls below or over shoots the nominal value and the DVR will inject the compensating voltage $\vec{V}$inj in phase with the load voltage $\vec{V}_{Load}$. Thus

restoring the magnitude of the load voltage back at nominal value. The control technique to be used will depend on the type of sensitive load to be protected and the load charactistic such as phase shift, magnitude or waveshape of the voltage. Fast transients (high dv/dt) will be difficultto correct.Large phase shifts will be difficult to correct andmay require ratings in excess of 1.0 voltageinjection [18].Magnetic contactors are very sensitive to voltage magnitude but not phase shift. Thus, the DVR control will be tailored to minimize voltage and equipment disruption. There are two categories of control techniques:

i) Reactive power compensation [19]

The concept of reactive power compensation technique is theinjected voltage ($\vec{V}$inj,)is in quadrature with the load current$\vec{I}_{\mathrm{L}}$and therefore no active power is provided by the DVR [19]. Theload power factor (pf) plays a significant role and thecompensation ability is limited. The minimum supply voltage that can be boost to the load voltage is

$$\left|\vec{V}_{\mathrm{Sag}}^{\min}\right| = \left|\vec{V}_{\mathrm{Load}}\right| * \mathrm{pf} \quad (1)$$

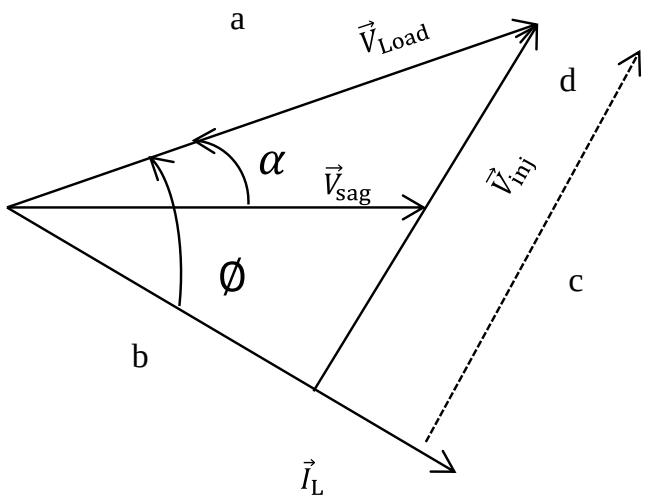

Fig. 5. Compensation technique using reactive power

From Fig. 5,

$$\vec{V}_{\mathrm{sag}} = \vec{V}_{\mathrm{Load}} - \vec{V}_{\mathrm{inj}}$$

$$\vec{V}_{\mathrm{sag}} = \vec{V}_{\mathrm{Load}}\cos\emptyset + j\vec{V}_{\mathrm{Load}}\sin\emptyset - \vec{V}_{\mathrm{inj}}$$

$$\left|\vec{V}_{\mathrm{sag}}\right| = \sqrt{\left|\vec{V}_{\mathrm{Load}}\right|^2 cos^2\emptyset + \left|\vec{V}_{\mathrm{Load}}\right| sin^2\emptyset - 2\left|\vec{V}_{\mathrm{Load}}\right|\left|\vec{V}_{\mathrm{inj}}\right| sin\emptyset + \left|\vec{V}_{\mathrm{inj}}\right|^2}$$

$$= \sqrt{\left|\vec{V}_{\mathrm{Load}}\right|^2 - 2\left|\vec{V}_{\mathrm{Load}}\right|\left|\vec{V}_{\mathrm{inj}}\right| sin\emptyset + \left|\vec{V}_{\mathrm{inj}}\right|^2} \quad (2)$$

If the injectionvoltage is limited to a magnitude of the minimum$\left|\vec{V}_{\mathrm{inj}}^{\max}\right|$the minimum boost of supply voltage to $\vec{V}_{\mathrm{Load}}$ is given as

$$\left|\vec{V}_{\mathrm{Sag}}^{\min}\right| =$$

$$\sqrt{\left|\vec{V}_{\mathrm{Load}}\right|^2 - 2\left|\vec{V}_{\mathrm{Load}}\right|\left|\vec{V}_{\mathrm{inj}}^{\max}\right| sin\emptyset + \left|\vec{V}_{\mathrm{inj}}^{\max}\right|^2} \quad (3)$$

where$\emptyset$ is the power factor angle arccos(pf).The voltageinjection capability is a function of the turns ratio of theseries injection transformer and the ratingofthePWMinverters.For reactive power compensation technique, the injected power by DVR (P_{inj}) is 0. Thus the input power to the DVR P_{in} and the the output power from DVR to the load P_{out} are analysed from from the following equations:

$$P_{\mathrm{in}} = V_{\mathrm{sa}}I_{\mathrm{L}}\cos(\emptyset - \alpha) + V_{\mathrm{sa}}I_{\mathrm{L}}\cos(\emptyset - \alpha) + V_{\mathrm{sa}}I_{\mathrm{L}}\cos(\emptyset - \alpha)$$

$$= (|V_{\mathrm{sa}}| + |V_{\mathrm{sb}}| + |V_{\mathrm{sc}}|)|I_{\mathrm{L}}|cos(\emptyset - \alpha) \quad (4)$$

$$= 3\left|V_{\mathrm{sag}}\right||I_{\mathrm{L}}|cos(\emptyset - \alpha)$$

for balanced fault.

$$P_{\mathrm{out}} = 3|V_{\mathrm{Load}}||I_{\mathrm{L}}|cos(\emptyset) \quad (5)$$

the voltage at sensitive load is balance.

The change of power $\Delta P = P_{\mathrm{out}} - P_{\mathrm{in}} = 0$

$$0 = 3|V_{\mathrm{Load}}||I_{\mathrm{L}}|cos(\emptyset) - (|V_{\mathrm{sa}}| + |V_{\mathrm{sb}}| + |V_{\mathrm{sc}}|)|I_{\mathrm{L}}|cos(\emptyset - \alpha) \quad (6)$$

$$\alpha = \emptyset - \arccos\left(\frac{3|V_{\mathrm{Load}}|cos\emptyset}{|V_{\mathrm{sa}}|+|V_{\mathrm{sb}}|+|V_{\mathrm{sc}}|}\right) \quad (7)$$

$$\alpha = \emptyset - \arccos\left(\frac{|V_{\mathrm{Load}}|cos\emptyset}{|V_{\mathrm{sag}}|}\right) \quad (8)$$

for balanced fault.

The supply voltage and the voltage at the load has taken an angle α for reactive power compensation.

(ii) Real and reactive power compensation

For dynamic compensation of voltage imperfection, compensation is by means of using real power.

(a) Pre-sag Compensation [19][20]

This technique compensates for the differences between the sag or depressed voltage ($\vec{V}_{\mathrm{sag}}$) and the pre-fault voltage ($\vec{V}_{\mathrm{pre\text{-}sag}}$) by restoring the instantaneous voltage to the same magnitude and phase as the nominal pre-sag voltage.

The Phase locked loop (PLL) tracks the positive sequence of the supply voltage and locks the angular frequency of the PLL output during the sag. This technique is used to loads sensitive to magnitude and phase shift such as thyristor based power

supplies. The drawback is capacity of energy storage and voltage injection capability is relatively large. Fig. 6 is the compensation to pre-sag conditions technique.

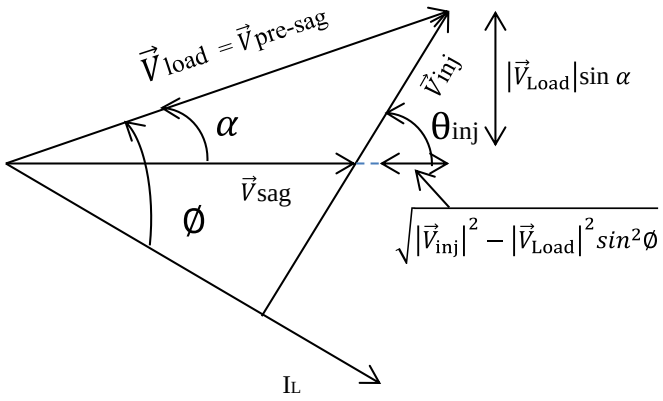

Fig.6. Compensation to pre-fault conditions

From Fig. 6, the minimum supply voltage that can be boosted to $\vec{V}_{Load}$is :

$$|\vec{V}_{Sag}^{\,min}| = |\vec{V}_{Load}|\cos\alpha - \sqrt{|\vec{V}_{inj}^{\,max}|^2 - |\vec{V}_{Load}|^2 sin^2}$$

The required angle of injection $\theta_{inj}$is calculated as:

$$\theta_{inj} = \arctan\frac{\vec{V}_{pre-sag}\sin\alpha}{\vec{V}_{pre-sag}\cos\alpha - \vec{V}_{pre-sag}} \quad (9)$$

The method gives nearly undisturbed load voltage [21].

(b) In-phase Compensation [19][20][21]

In Phase compensation technique is designed to compensate forthe voltage magnitude only. Voltage sag accompanied by phase shift, the supply voltage will have a phase shift with respect to the pre-sag voltage. This technique requires a fast tracking PLL. The minimum supply voltage that can be boosted to $\vec{V}_{Load}$ is:

$$|\vec{V}_{sag}^{\,min}| = |\vec{V}_{Load}| - |\vec{V}_{inj}^{\,max}| \quad (10)$$

Fig. 7 shows the vector presentation for in-phase compensation.

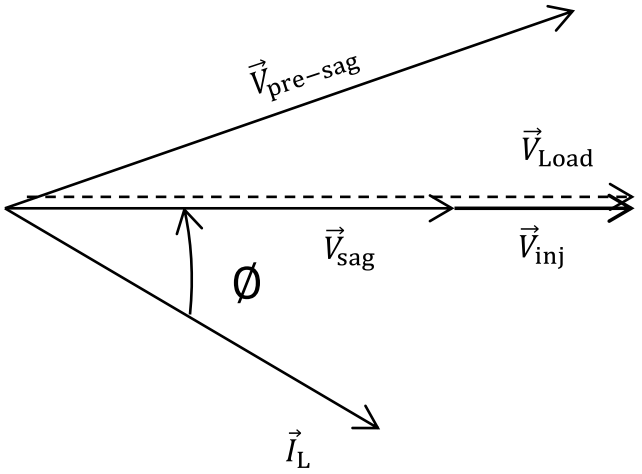

Fig. 7. Vector diagram for in-phase compensation technique

The apparent power by the DVR is:

$$|S_{DVR}| = |I_L|(|V_{Load}| - |V_{sag}|) \quad (11)$$

Assuming for a balanced fault, the real power injection is:

$$P_{DVR} = 3\,|V_{Load} - V_{sag}|I_L\cos\emptyset$$

$$= 3\,|V_{inj}|I_L\cos\emptyset \quad (12)$$

This method is suitable for loadsthat can withstand phase angle jumps, which is a typical case forinduction motor loads which comprise a large portion of theindustrial power system, with no sensitive equipment such asadjustable speed drives or any equipment depending in itsoperation on phase triggered switches. This method is verysimple in implementation, very fast especially in calculating theDVR compensation voltage. The in-phase compensation technique is applied in this research study.

(c) Energy-saving Compensation [19][20][21]

The purpose of energy-saving compensation is to introduce voltage injection to affect a phase-angle adjustment in the load-side voltage($\vec{V}_{Load}$) to maximize the load ride through capability by DVR.

In Fig. 8 the injected voltage ($\vec{V}_{inj\,1}$) have a phase advance β with respect to the supply voltage ($\vec{V}_{sag\,1}$). Compare to in-phase injection scheme, the energy-saving technique reduces the injected real power from V_{inj_p2} I_L to $V_{inj\_p1}I_L$.Correspondingly, the reactive power generated by the inverter increases.

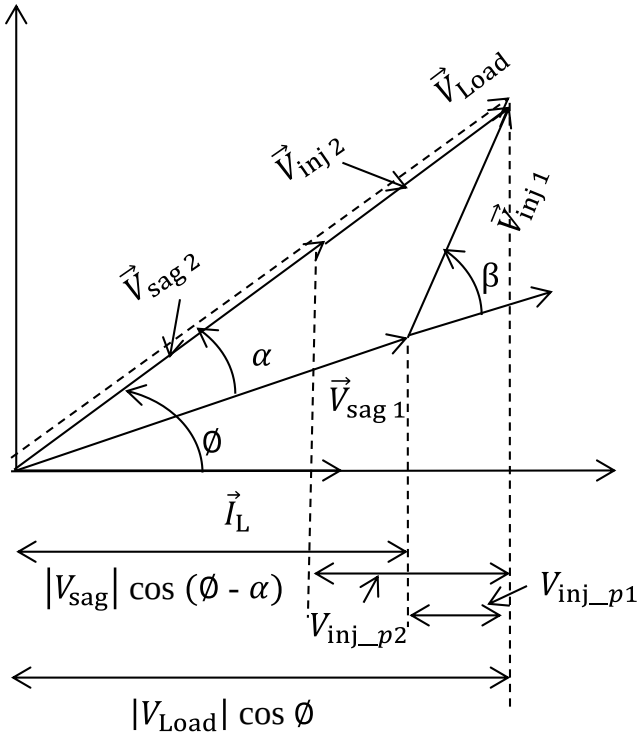

Fig. 8. Vector diagram for energy-saving technique

There is a phase difference between supply voltage phasor ($\vec{V}_{sag\,1}$) and load voltage phasor the voltage injection ($\vec{V}_{inj\,1}$) is larger that used in-phase injection ($\vec{V}_{inj\,2}$).

$$PDVR = |V_{Load}|cos\emptyset|I_L| - |V_{sag}|\cos(\emptyset - \alpha) \quad (12)$$

Fig. 9 is the summary of compensation techniques.

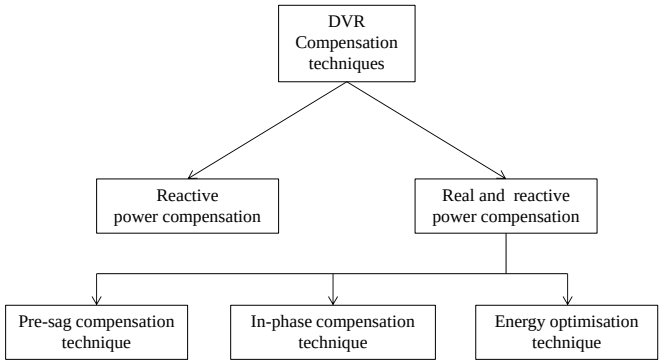

Fig.9.Summary of compensation techniques.

The most significant difference in these three schemes from real and reactive power compensation is the selection of the reference voltage for the control system of the DVR during the restoration process.For the In-phase compensation, the compensated load voltage to be always in phase with the measured supply voltage , regardless of the predisturbance voltage. The reference voltage of the control system will always be in phase with the supply voltage. For pre-sag compensation requires the continuous tracking of supply voltage. By voltage injection is made equal to that of its pre-sag value. The technique uses the pre-sag voltage as the reference signal for its control system. The energy-saving compensation method voltage injection necessitates a phase-angle adjustment in load voltage, ensuring that the magnitude of load voltage is equal to that of its pre-sag value. Thus, load voltage will be phase shifted with respect to its pre-sag value. By changing this phase shift, the injected active power through the DVRcan be controlled so as to maximize the load ride through capability afforded by the energy storage device.The three compensation schemes, assuming that the voltage sag/swell is balanced.

(d) Swell compensation method [23]

The DVR can also beused to restore load voltages during a swell. Long duration and excessive voltage
swell can be damaging to electrical equipment. Power transformers could enter into magnetic flux saturation region during the swell and is subject to high electromagnetic (EM) stress.
During a swell, the DVR will absorb active power from the external system. This will then lead to a voltage rise in the energy storage device within the DVR.

Harmonic mitigation[24]

The approach used in [24] to mitigate the harmonics is described.Power system model is shown in Fig. 10.

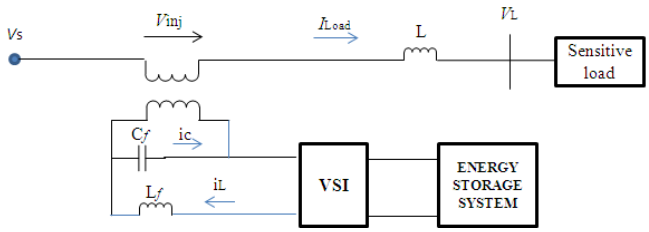

Fig. 10.Single line diagram to describe power quality problem.

In Fig. 10, the distorted supply voltage V_S from the source can beexpressed as :

$$V_{sa} = \sum_{n=1}^{\infty}\left[\begin{matrix}V_{on} + V_{1n}\sin(n\omega_0 t + \varphi_{1n}) \\ + V_{2n}\sin(n\omega_0 t + \varphi_{2n})\end{matrix}\right] \quad (13)$$

$$V_{sb} = \sum_{n=1}^{\infty}\left[\begin{matrix}V_{on} + V_{1n}\sin\left(n\omega_0 t + \varphi_{1n} - 2n\frac{\pi}{3}\right) \\ + V_{2n}\sin(n\omega_0 t + \varphi_{2n} + 2n\frac{\pi}{3})\end{matrix}\right] \quad (14)$$

$$V_{sc} = \sum_{n=1}^{\infty}\left[\begin{matrix}V_{on} + V_{1n}\sin\left(n\omega_0 t + \varphi_{1n} + 2n\frac{\pi}{3}\right) \\ + V_{2n}\sin(n\omega_0 t + \varphi_{2n} - 2n\frac{\pi}{3})\end{matrix}\right] \quad (15)$$

where,
$\omega_0$is fundamental frequency.

n is harmonic order.
$V_{0n}$is zero phase sequence voltage component.
$V_{1n}$and$\varphi_{1n}$are magnitude and hase of positive sequence voltage component.
V_{2n}andφ_{2n}aremmagnitudemand phase of negative sequence voltage component.
Distorted voltage supply at the sensitive load end is undesirable. The desirable voltage $V_L$at the sensitive load comprises the fundamental components as eq.(13)-(15);

$$V_{La}^{`} = V_{11}\sin(\omega_0 t + \varphi_{11}) \quad (16)$$

$$V_{Lb}^{`} = V_{11}\sin(\omega_0 t - 2\frac{\pi}{3} + \varphi_{11}) \quad (17)$$

$$V_{Lc}^{`} = V_{11}\sin(\omega_0 t + 2\frac{\pi}{3} + \varphi_{11}) \quad (18)$$

The injection voltage of DVR will compensate for the difference between V_S and the desired voltage $V_L$described by eq. (16) - (18). The injected voltage by DVR will contain the ac voltage component in series with the distorted supply voltageV_s and contains all theharmoniccomponentaseq (13)-(15). Eq (13)-(15) express in compact form;

$\vec{V_s} = [V_{sa}, V_{sb}, V_{sc}]^T$ and eq. (16)-(18) denoted by

$\vec{V}_{sf} = [V_{La}^{`}, V_{Lb}^{`}, V_{Lc}^{`}]^T$. Hence from eq. (13)-(18), the injection voltage V_{inj} from DVR to compensate would have to be

$$V_{inj} = -V_{Lh} = V_{Lf} - V_L \quad (19)$$

Control algorithm for DVR
The primary function of the of the DVR control unit is to detect/extract the voltage quality problems such as voltage harmonic, voltage sag/swell etc., from the supply side of the DVR model, and to force the VSI to produce and to inject the corresponding compensation voltage through the injection transformer in order to keep the load bus of the sensitive load all the time at the desired value or to keep the sensitive load insensitive to the supply side voltage disturbances.
A new method is proposed for the DVR based on the synchronous reference frame voltage transformation to estimate the reference voltages. The reference voltage signal is derived based on synchronous reference frame theory as shown in Fig.11. Advantage of proposed controller has minimum component assembly and costing.Simplifies the process and stabilizes the control system, ensures a fast response andexcellent dynamic voltage compensation capability. Provide provision for zero sequence voltage for unbalanced fault.

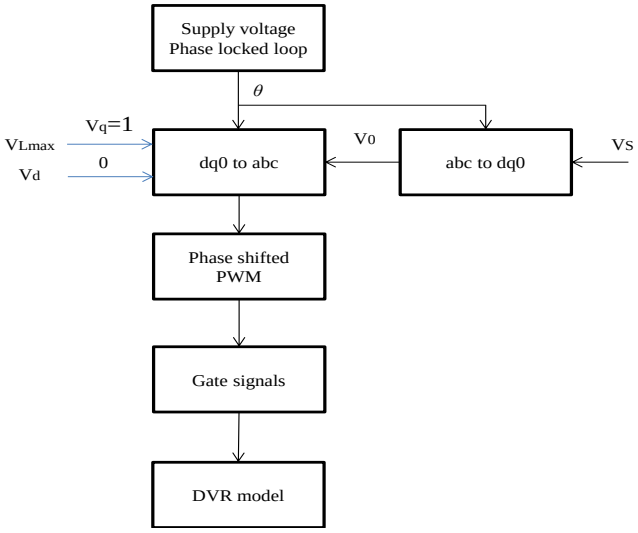

Fig.11.DVR control algorithm

Design of cascaded H-Bridge Multilevel Inverter
The seven-level inverter is shown in Fig.12. The seven-level inverter consists of three series connected H-bridges. Each cell has four power switches with anti-parallel diodes and a dc supply. The CHB inverter in Fig.12 can produce phase voltage with seven voltage levels. When switches S15, S15, S13, S13 and S11, S11 conduct, the

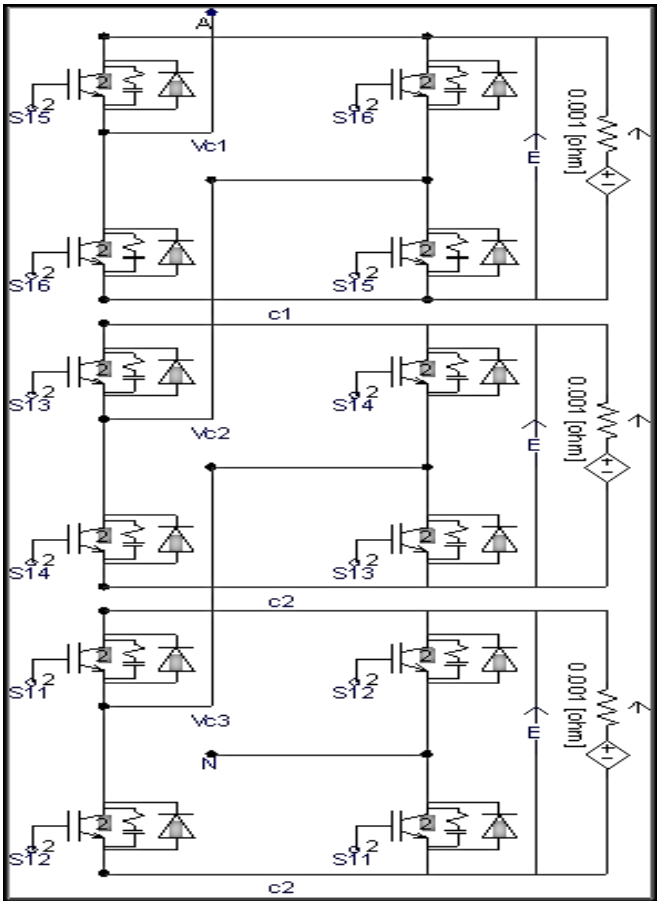

Fig. 12.The seven-level inverter.

output voltage of the H-bridge cells c1, c2 and c3 is Vc1=Vc2=Vc3= E = Vdc, and the resultant inverter phase voltage is Van = Vc1 + Vc2 + Vc3 = 3Vdc, which is the voltage at the inverter terminal A with respect to the inverter neutral N. Similarly, with S16, S16, S14, S14 and S12, S12 switched on, Van = –3E = -3Vdc. The other three voltage levels are +Vdc, +2Vdc, 0, and –Vdc, -2Vdc which correspond to various switching states.Voltage levels in a CHB inverter can be found from

$$m = (2H + 1) \quad (20)$$

where H is the number of H-bridge cells per phase leg. The voltage level m is always an odd number for the CHB inverter.

Phase shifted PWM is implemented in this DVR model.For each module, the reference signal is the same. However, the carrier waveform is triangular waveform for each module is phase shift to ensure

the step characteristic of the output voltage. The bipolar modulation method is chosen, the phase shift between each module is 360/*p*[25], where*p*is the number of modules. For sevenlevel multilevel inverter with bipolar modulation method,*p*is6.Thus each module is phase shifted at intervals of 60 degrees, starting at 0, 60, 120, 180, 240, 300, connecting to gate signals.The gate signals are generated with proper comparison of carrier wave and modulating signal.

For one phase of seven levels multilevel inverter six triangular wave carriers are required with a 60°

phase displacement between any two adjacent carriers. Theadvantage of Phase Shifted Carrier PWM is that the switching frequency andconduction period is same for all devices and rotating ofswitching patterns is not required [26].

The Phase Shifted Carrier PWM is shown in Fig. 13. The phase voltage of cascaded seven-level multilevel inverter is shown in Fig.14.

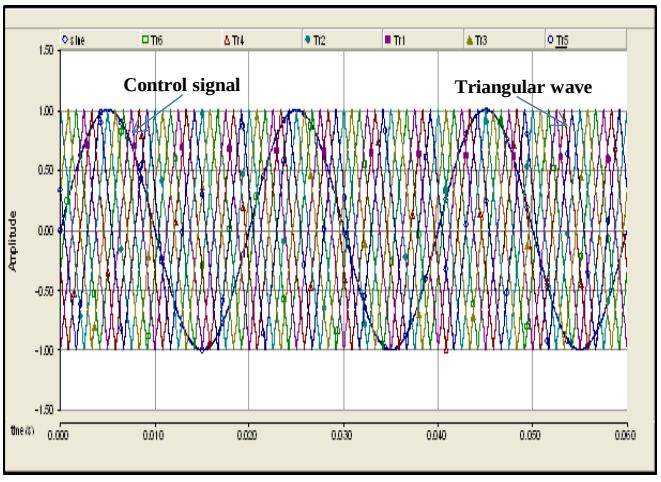

Fig.13. The Phase Shifted Carrier PWM in PSCAD

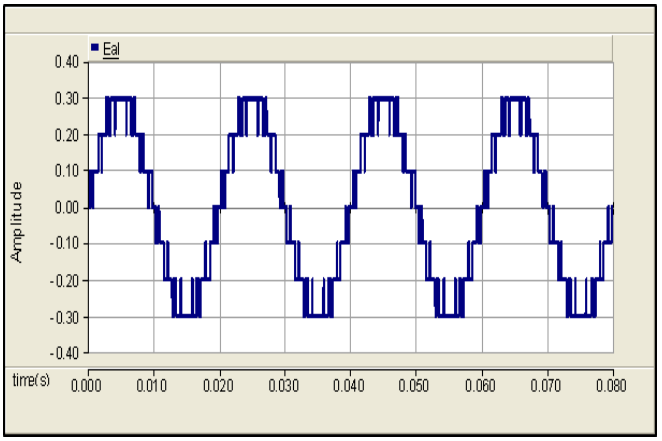

Fig.14. The phase voltage of cascaded sevenlevel multilevel inverter in PSCAD.

The multilevel inverters improve the AC power quality by performing the power conversion in small voltage steps resulted in lower harmonics [22]. The reference voltage and supply voltage are constantly measured using respective measurement modules and the output of these modules, which are represented in a-b-c frame, are transformed into equivalent d-q-0 frame using Park's transformation. The magnitudes of the d-q-0 outputs, which are the representatives of load voltage and reference voltage, are compared and the error is fedto the seven level multilevel inverter.The output is the modulation signal for PWM generator. The output of the multilevel inverter is injected into the bus bar to mitigate the sag or swell and voltage harmonics to maintain the load voltage constant and to protect the sensitive loads. The output of the multilevel inverter is the algebraic sum of the individual outputs of the full bridges.

Verification through simulation

In this section, simulation results are presented to illustratethe effectiveness of the proposed DVR control strategy with 7 level H-Bridge based DVR using multicarrier SPWM techniques inmitigating voltage harmonics and voltage sags and swells.Simulations were accomplished using PSCADEMTDC.

Effectiveness on harmonic mitigation

Fig.15 shows the waveforms of source voltage,harmonic injected voltage andload voltage when DVR is connected online.Fig. 16 shows the corresponding waveforms when the DVR is in service. The DVR is connected at 0.10 to 0.20 sec for 100msec.

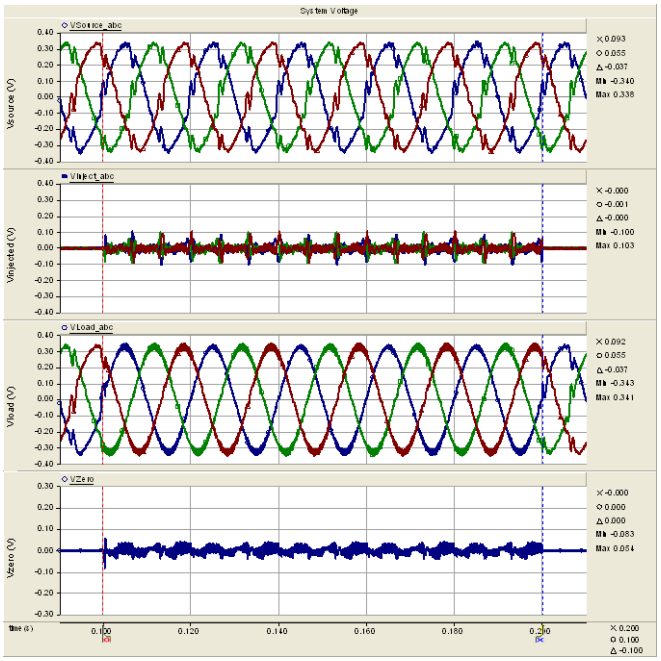

Fig. 15. Voltage harmonic mitigation byDVR

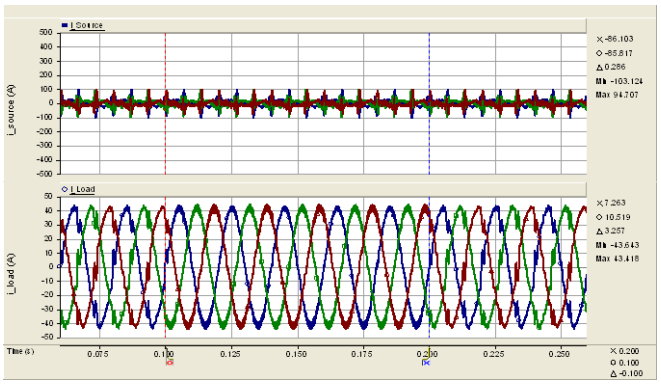

Fig. 16.Source current and load current

Both the load voltage and load current waveform are sinusoidal and at rated value as shown in Fig. 15 and 16, respectively.

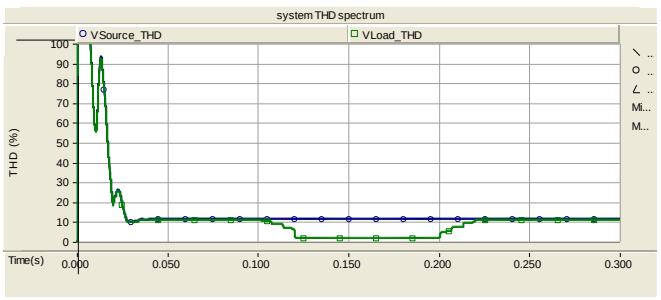

Fig. 17.THD level of voltage at source and load.

It can be shown in Fig. 17 that the source voltage has a THD level of 12.15 %. With voltage harmonics compensation by the DVR,the sensitive load is protected against the voltage imperfection introduced by the nonlinear load and the THD of the load voltage has been significantly reduced to 1.65 %.

Effectiveness on swell mitigation

The simulation started with the supply voltage swell is generated as shown in Fig.18.

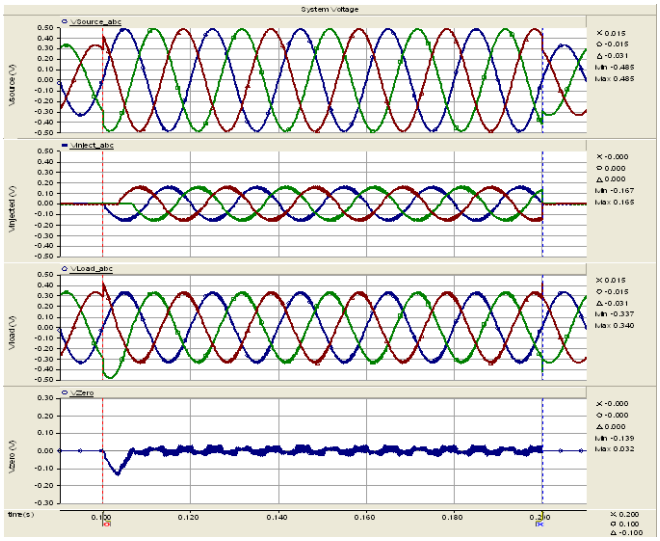

Fig. 18. Swell mitigation by DVR

As observed from this figure the amplitude of supply voltage is increased about 15% from its nominal voltage. Fig.18 shows the injected and the load voltage respectively. The DVR reacts quickly to inject the appropriate voltage component (negative voltage magnitude) to correct the load voltage. As can be seen from the results, the load voltage is kept at the nominal value 340 V by the DVR.

Effectiveness* on sag *mitigation

A balanced three-phase fault (3LGF) was created, resulted in voltage sag of 59 % i.e., bringing down the supply voltage to 200 Volts from 340 Volts peak magnitude, is introduced at 0.1 second, which lasts for 100 milliseconds as shown in Fig. 19.

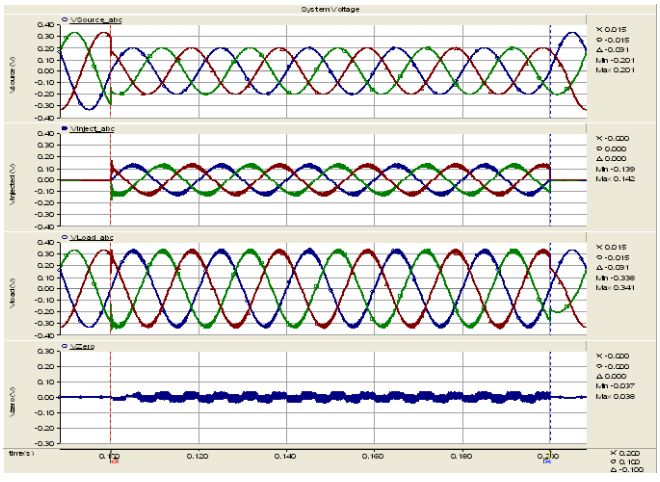

Fig. 19. Three-phase balanced voltage sag

For 100 ms, the DVR starts injecting the required compensating voltage, thus restoring the voltage at the sensitive load to its rated value of 340 Volts and is sinusoidal. The results confirm the improved transient performance of the DVR.

Effectiveness onvoltage sag with harmonics mitigation

A three-phase fault to ground with voltage harmonic is created at 0.1 sec for a duration of 100 ms and is displayed in Fig.20.The supply voltages were distorted with voltage sag and voltage harmonics, which also affected supply voltages of sensitive load downstream. At time 0.1 sec, DVR is put into operation and disconnected at time 0.2 sec.For 100 ms, the DVR starts injecting the required compensating voltage with the harmonics, thus restoring the voltage at the sensitive load to its rated value and sinusoidal.

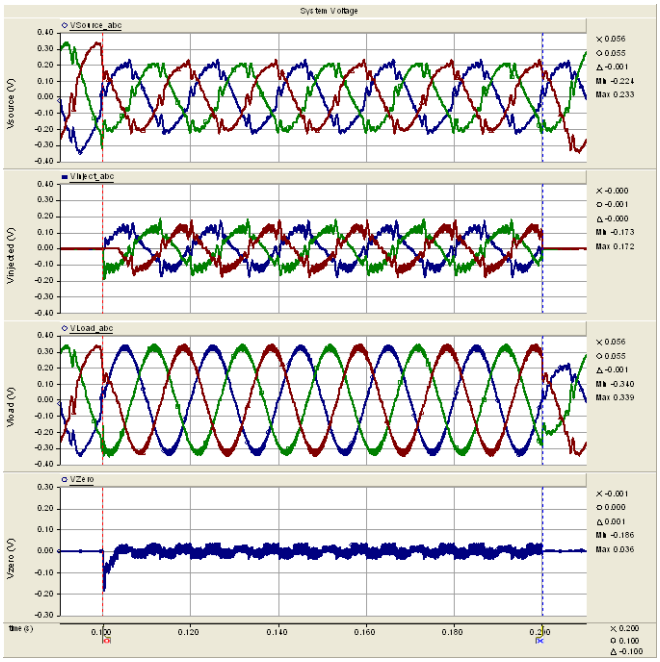

Fig.20. 3LGF with harmonics, showing source voltage, injected voltage, and voltage at sensitive load with DVR online.

Effectiveness on single line to ground fault sag mitigation

A single line-to-ground fault (SLGF) on phase a is created at 0.1 sec to 0.2 sec for a duration of 100 ms and is displayed in Fig. 21.

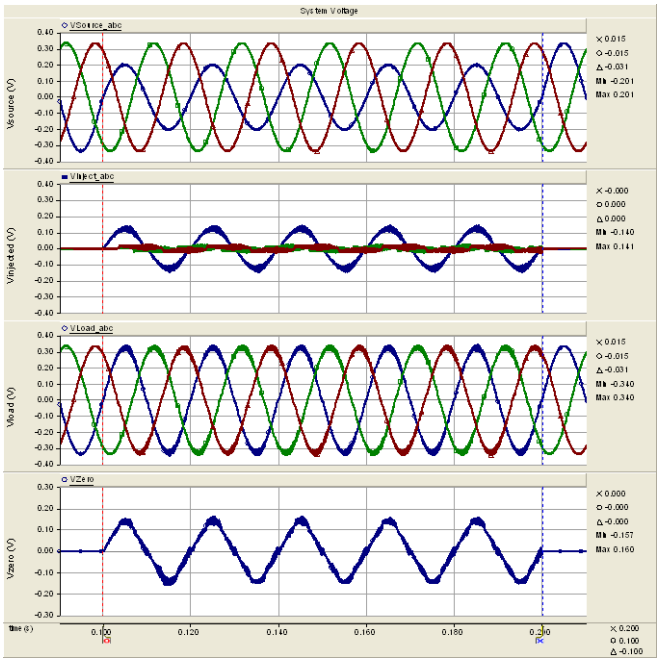

Fig.21.Single line to ground fault voltage sag

The sag resulted in voltage drop bringing the supply voltage on phase a to 200 Volts from 340 Volts peak magnitude. For 100 ms, the DVR starts injecting the required compensating voltage, thus restoring the voltage at the sensitive load to its rated value of 340 Volts and is sinusoidal. The results confirm the improved transient performance of the DVR.

Effectiveness on SLGF voltage sag with harmonics mitigation

A three-phase fault to ground with voltage harmonic is created at 0.1 sec for a duration of 100 ms and is displayed in Fig.22.

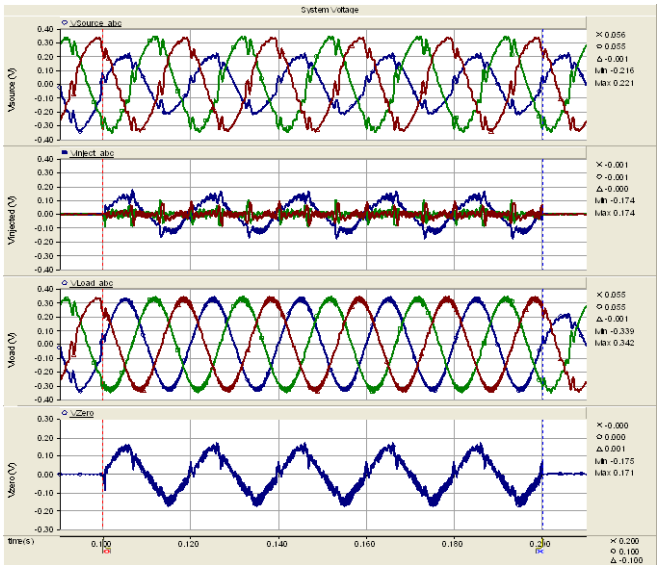

Fig. 22.SLGF with harmonics, showing source voltage, injected voltage,and voltage at sensitive load with DVR online.

The supply voltages were distorted with voltage sag and voltage harmonics, which also affected supply voltages of sensitive load downstream. At time 0.1 sec, DVR is put into operation and disconnected at time 0.2 sec. For 100 ms, the DVR starts injecting the required compensating voltage with the harmonics, thus restoring the voltage at the sensitive load to its rated value and sinusoidal.

Effectiveness ondouble line to ground fault sag mitigation

Double line-to-ground fault is created between time 0.1 sec and 0.2 sec for a duration of 100 ms and is displayed in Figure 23.At 0.1 sec, the supply voltages phases a and b dropped to 200 V, phase c remained at 340 V peak magnitude, which also affected the supply phase voltages at the sensitive load downstream.For 100 ms, the DVR starts injecting the required compensating voltage, thus restoring the voltage at the sensitive load to its rated value of 340 Volts and is sinusoidal. The resultsconfirm the improved transient performance of the DVR.

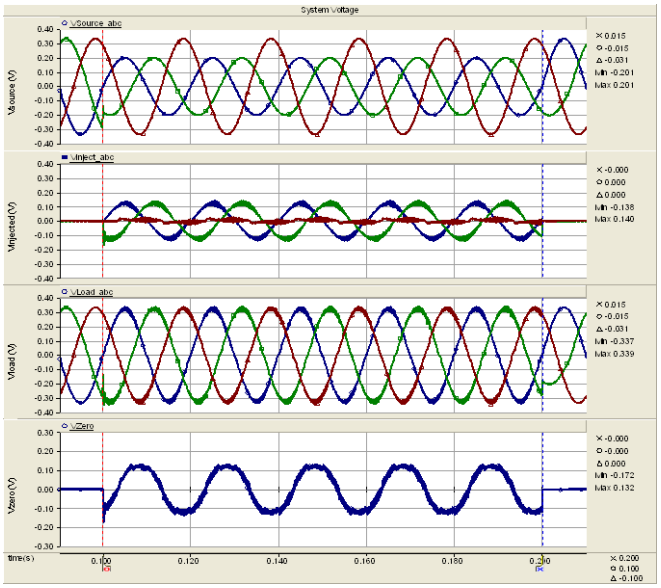

Fig. 23. Double line to ground fault

Effectiveness onDouble line fault sag mitigation

Double line fault is created between time 0.1 sec and 0.2 sec for a duration of 100 ms and is displayed in Figure 24. At 0.1 sec, the supply voltages phases b and c dropped to 240 V, phase a remained at 340 V peak magnitude, which also affected the supply phase voltages at the sensitive load downstream. For 100 ms, the DVR starts injecting the required compensating voltage, thus restoring the voltage at the sensitive load to its rated value of 340 Volts and is sinusoidal. The results confirm the improved transient performance of the DVR.

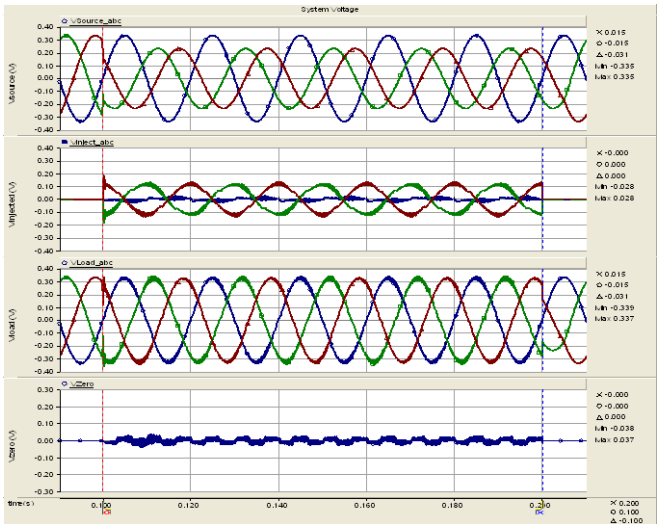

Fig. 24.Double line fault

Performance comparison regarding percentage total harmonic distortion (THD) is illustrated in Table 1.

TABLE. 1. Performance comparison

Description	[27]	[28]	Current Study
Year	2012	2012	2014
Operating voltage and frequency	400 V, 50Hz	400 V, 50Hz	415 V, 50Hz
Inverter type	3-level	3-level	Cascade Multilevel
RMS of the load side voltage after compensation	240 V	240 V	240 V
THD of the load side voltage after compensation	3.9 %	4.35 %	1.65 %

Conclusion

Power quality improvement through DVR with seven level multilevel inverter has been investigated. With nonlinear load, high level of voltage harmonics distortion is observed. An improved performance method to control the injection voltage by DVR so that the DVR is able to mitigate voltage sag, swell and voltage harmonic has been described. With the seven level multilevel inverter, the total harmonic distortion has been greatly reduced below the 5 % level as required. The function of DVR is to control the load voltage of sensitive load. Verification by simulation have confirmed the effectiveness of the proposed method with the DVR, to achieve improved quality of supply at the sensitive load end.

References

[1] V. Khadhikar, A. Chandra, "A Novel Control Approach for Unified Power Quality Conditioner - Q

without Active Power Injection for Voltage Sag Compensation", IEEE International Industry Technology, pp. 779-784, 15-17 Dec. 2006.

[2] S.S.Chooi, J.D. Li, "A Generalized Voltage Compensation Strategy for Mitigating the impacts of Voltage Sags/Swells," IEEE Transaction on Power Delivery, Vol. 20. N0.3, July 2005.

[3] W.M. Grady, M.J. Samotyj, A.H. Noyola, "Minimizing Network Harmonic Voltage Distortion with an Active Power Line Conditioner", IEEE Transactions on Power Delivery, pp. 1690-1697, October 1991.

[4] K.L.Lian, Brian K. Perkins, P.W. Lehn, "Harmonic Analysis of a Three-phase Diode Bridge Rectifier on Sampled-Data Model", IEEE Transactions on Power Delivery, Vol. 23. No.2, pp. 1088-1096, April 2008.

[5] D. S. Dorr, M. B. Hughes, T. M. Gruzs, R. E. Jurewicz, and J. L. McClaine,"Interpreting recent power quality surveys to define the electrical environment", IEEE Transactions on Industry Applications, Vol. 33, No. 6, pp. 1480–1487, 1997.

[6] P.T.Nguyen, TapanK.Saha, "Dynamic voltage restorer against balanced andunbalanced voltage sags: Modelling and simulation", IEEE transactions on Power Delivery, Vol. 1, pp. 639-644, 6-10 June 2004.

[7] John Godsk Nielsen, Michael Newman, Hans Nielsen, Frede Blaabjerg, "Control and testing of a Dynamic Voltage Restorer at medium voltage level",IEEE Transactions on Power electronics,Vol.3, pp. 1248-1253. 15-19 June 2003.

[8] Roy McHattie, "Dynamic Voltage Restorer", IEE Colloqium on Dynamic Voltage Restorer, pp. 1-5, 11 Feb. 1998.

[9] M.F. McGranaghan, D. Muller, "Effects of voltage sags in process industry applications", Power Quality Seminar notes, UMIST 2000.

[10] Ramasamy, M, and S. Thangavel, 2012. Photovoltaic based Dynamic Voltage Restorer (PV-DVR) with Power Saver Capability using PI Controller. Electrical Power and Energy System, 36: 51-59.

[11] A.Venkatakrishna, "Phase Shifted and Level Shifted PWM Based Cascaded Multilevel Inverter Fed Induction Motor Drive", International Journal of Current Engineering and Technology, pp. 350-354, Vol.4, No.1 (Feb 2014).

[12] Rosli Omar, NasrudinAbd Rahim, MarizanSulaiman, 2009. Modeling and Simulation for Voltage Sags/Swells Mitigation using Dynamic Voltage Restorer (DVR). Journal of Theoretical and Applied Information Technology, pp: 464-470.

[13] Benachaiba, C., and B. Ferdi, 2009. Power Quality Improvement using a DVR, American Journal of Applied Sciences, 6(3): 396-400.

[14] K.Chandrasekaran, V.K. Ramachandaramurthy "Voltage harmonic elimination with RLC based interface smoothing filter", IOP Conference Series, Material Science and Engineering, CUTSE 2015.

[15] K.Chandrasekaran,V.K. Ramachandaramurthy, "Power System Harmonic Elimination to Improve Power Quality", IOP Conference series, Journal of Physic, Bali, 2015.

[16] B. Wu, High-Power Converters and AC Drives: Wiley, 2006.

[17] Y. Shakweb, "New breed of medium voltage converters", IEE Power Engineering Journal, Vol. 14, N0.1, February 2000, pp. 12-20.

[18] S.W. Middlelekauff, E.R. Collins, " System and customer impact considerations for series custom power devices", IEEE Transactions on Power Delivery, Vol. 13, N0. 1, January 1998, pp. 278-282.

[19] Changjiang Zhan, V. K. Ramachandaramurthy, "Dynamic Voltage Restorer Based on Voltage Space Vector PWM Control", IEEE Transactions on Industry Applications, Vol. 37 (No.6), pp. 1855-1863. Nov./Dec. 2001.

[20] Md. RiyasatAzim, "A Fuzzy Logic based Dynamic Voltage Restorer forVoltage Sag and Swell Mitigation for IndustrialInduction Motor Loads",International Journal of Computer Applications, Volume 30– No.8, September 2011.

[21] ElShennawy, Abdel-Mon'emMoussa, M. El-GammalandA. Abou-Ghazala, 2010. "A Dynamic Voltage Restorer forVoltage Sag Mitigation in a Refinery with Induction MotorLoads", Am. J. Applied Sci. 3(1), 144-151, 2010.

[22] A.Venkatakrishna, "Phase Shifted and Level Shifted PWM Based Cascaded Multilevel Inverter FedInduction Motor Drive", International Journal of Current Engineering and Technology, pp. 350-354, Vol.4, No.1 (Feb 2014).

[23] S.S.Choi, "A Generalized Voltage Compensation Strategy forMitigating the Impacts of Voltage Sags/Swells",IEEE Transactions on Power Delivery, Vol. 20, No.3, pp. 2289-2297, July 2005.

[24] T.X. Wang, "Series compensation method to mitigate harmonicsand voltage sags and swells", IET Gener.Transm.Distrib., Vol. 1, No. 1, pp.96-103, January 2007.

[25] J. Rodríguez, S. Bernet, B. Wu, J. O. Pontt, S. Kouro "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives" IEEETransaction on Industrial Electronics, vol. 54, no. 6, pp. 2930-2945, December2007.

[26] Bin, Wu, High Power Converters and AC Drives, Jon Willy & Sons. Inc,Hoboken, New Jersey, pp.119-142, 2006.

[27] M. A. Mulla, "A Simplified Control Strategy for Series Hybrid Active Power Filter that Compensat Voltage Sag, Swell, Unbalance and Harmonics" IEEE, pp. 1-6, 6-8 Dec. 2012.

[28] AlirezaJavadi, "A Novel Transformerless Hybrid Series Active Filter", IEEE Industrial Electronics Society, pp.5312- 317, 25-28 Oct. 2012.