

New Modifications of Aggressive Packet Combining Scheme with improved performance

Y. Saring

Assistant Professor, Department of ECE, NIT Arunachal Pradesh, Yupia, Arunachal Pradesh
ys.nitap@gmail.com

Y. Bulo,

Assistant Professor, Department of ECE, NIT Arunachal Pradesh, Yupia, Arunachal Pradesh
yakabulo@gmail.com

Prof. Dr. C. T. Bhunia

Director NIT Arunachal Pradesh, Yupia, Arunachal Pradesh ctbhunia@vsnl.com

Abstract

The wireless network suffers from high bit-error rate. High bit-error rate significantly reduces the effective bandwidth available to users. In order to tackle the high bit error rate & multiple bit errors with low latency (for fast delivery) and also to preserve bandwidth & energy, Aggressive Packet Combining Scheme (APC) was introduced. However APC suffers from two major drawbacks, it fails to correct error when error(s) occur in the same bit location of all received erroneous copies, and secondly it suffers from low throughput. In this paper, few modifications of APC scheme are suggested and proposed to improve the throughput and correction capability. Our analysis shows that the proposed schemes can not only correct multiple bit errors, but also other errors whether random or burst, occurring in the same bit locations of all received erroneous copies, along with improving throughput, without adding any delay or extra bits, thus preserving bandwidth and energy efficiency.

Keywords: Aggressive Packet Combining, Throughput, Bit Error Rate, Correction Capability, Gray Code.

Introduction

The wireless networks suffer from high bit-error rate. In order to transmit data reliably from transmitter to receiver either Forward Error Correction (FEC) or Backward Error Correction (BEC) techniques are used. FEC uses error correction codes, so it uses more check bits and more bandwidth for a particular data size than those required for BEC. BEC uses error detecting codes, and uses feedback path for requesting retransmission of packet or bit in error. BEC is implemented by ARQ protocols in which the packets with errors are discarded, and errors are corrected by retransmission till the packet is correctly received by receiver [1]. BEC is cost effective but suffers from appreciable amount of delays incurred due to retransmission. Wireless channels suffer from high bit error rate [2] in the range of 10^{-2} to 10^{-4} . To transmit data reliably in wireless network, FEC will need a powerful long code and complicated coder-decoder pair, which will be costly and will consume higher bandwidth. Several researchers attempted to apply BEC in wireless communication as it is cost effective [3-6]. Traditional BEC

techniques like ARQ protocol discard and retransmit erroneous packet till the packet is received correctly. But the erroneous packet may contain both erroneous bits and correct bits and hence it may still contain useful information. To extract useful information contain in the erroneous packets, Chakraborty proposed a simple yet elegant technique of packet combining (PC) scheme [7-8]. In PC scheme, receiver will not discard the erroneous copy received, but store it. On receiving another erroneous copy of the packet, it will XOR the two erroneous copies received to obtain the bit location of erroneous bits, thereafter the packet is corrected by bit inversion of located erroneous bits. However PC scheme fail to correct multiple bit errors and when atleast an error occur in the same bit location of both the received erroneous copies. Bhunia proposed modified packet combining scheme (MPC) [9], in which receiver on receiving an erroneous copy of a packet, will not discard, but will retain it and request for retransmission of the packet. On receiving request for retransmission of the packet, transmitter will send i ($i > 1$) number of copies of the requested packet. Receiver on receiving these i copies of the packet, will perform pair-wise XORed of the received copies to locate the error. MPC has better correction capability but at the expense of increased throughput as that of PC. Also if all of the retransmitted i copies of the packet suffers the same link error syndrome as that of first copy that was transmitted, then MPC will fail to correct such errors. To overcome flaws of PC and MPC, the retransmitted packet was reversed and transmitted in packet reversed packet combining (PRPC) scheme [10]. PRPC combining fails when the middle bit of both first copy and the retransmitted copy are erroneous. In order to tackle the high bit error rate & multiple bit errors and also to preserve bandwidth & energy, Aggressive Packet Combining Scheme was introduced by Leung [11], which is a modification of Majority Packet Combining (MjPC) scheme [12]. APC is fundamentally a low latency error correction scheme, in which transmitter will send three copies of packet to receiver. Receiver on receiving three erroneous copies will combine received copies by bitwise majority voting. It checks error on the combined packet, if still it is erroneous, receiver will identify least reliable bits and will search the correct bit pattern for the identified least reliable bits. If still correct copy is not found, it will request for retransmission of the packet.

APC fails when errors occur in the same bit location in all three copies of the packet [13]. Several new modifications of APC are suggested in [14], in which authors have suggested to increase the packet size to improve throughput efficiency of APC. But with increase in packet size, the bandwidth occupancy of the data may rise which may turn expensive for data communication because bandwidth is a scarce resource in data communication [15]. Ferriere et al. [16] proposed simple packet combining (SpaC) scheme for wireless sensor network, in which hybrid ARQ is generalized to multi-hop environment. Dengsheng et al. [17] proposed a packet combining scheme using cross packet coding that can increase code rate, different from previous PC scheme, instead of retransmitting a copy of the packet, a redundant packet obtained from cross packet coding of multiple source packet is retransmitted.

However the packet combining techniques depend heavily on the bit-error behavior in wireless transmission. In [18] authors have made an indepth study of the characteristics of subframe bit errors and their location distribution by conducting extensive experiments on several IEEE 802.11 WLAN testbeds. Their experimental results identify three bit error patterns: slope-line, saw-line, and finger. Slope-line bit error pattern show that a bit near the end of frame is more likely to be received in error than a bit near the beginning of the frame. Miu et al. [19] show that bit errors are clustered within the frame in a regular pattern. Schmidt et. al [20] studied the distribution of errors within erroneous frames for low-power wireless network. Their study show that (i) errors are not evenly distributed, but show bursty tendencies, (ii) coding leads to some bits being more stable than others and (iii) some content is inherently more stable than other during transmission.

Based on the above observations, we proposed new modifications of APC in order to achieve better correction capability and improve throughput. This paper is organized as follows: before discussing the proposed technique, we reviewed Aggressive packet combining scheme and discussed basic idea /Analysis with examples, followed by conclusion.

Review of APC

In the APC scheme transmitter sends three copies of the packet, say $P = 1010$. Say the received three copies at receiver are $P_1 = 1011$, $P_2 = 0010$ and $P_3 = 1011$, as shown in Table 1. Receiver applies bit by bit majority voting on the received erroneous copies to produce combined packet 1011. The combined packet is still erroneous, the 1st and 4th bits from left are identified as the least reliable bits. Receiver will search the correct bit pattern for the 1st and 4th bits. The 1st and 4th bits are 11 in the combined erroneous packet 1011, thus they may be either 00 or 01 or 10. The receiver replaces the identified least reliable bits with these three bit patterns, and performs error detection, and it obtained the correct packet which is 1010.

TABLE 1. An example of APC to recover correct packet, the transmitted packet is 1010

Received Copies	Bit-by-bit Majority Voting	Error Detected	Least Reliable Bits	Search the correct bit patterns	Error Detected
1011	1011	Yes	1 st and 4 th	0010	Yes
0010				0011	Yes
1011				1010	No

APC scheme can correct multiple bit errors, however APC scheme has several flaws, out of which the two major flaws are, firstly, the low throughput of APC, throughput can be defined as the average (N) number of times a packet is transmitted to get the correct copy and it is a very important parameter of measuring the performance of any error correction scheme. In APC, three copies of a packet are transmitted in best condition, thus the throughput of APC is $\eta_{APC} = \frac{1}{3} \times 100\% = 33.33\%$ only. Secondly, APC cannot correct error if error occurs at the same bit location of all received erroneous copies of the packet. The failure of APC to correct error is illustrated with an example in Table 2. The received copies of the source packet has error in the same bit location, so with APC scheme corrected copy cannot be obtained for this packet.

TABLE 2. An example of failure of APC to correct error, the transmitted packet is, the transmitted packet is 1010

Received Copies	Bit-by-bit Majority Voting	Error Detected	Least Reliable Bits	Search the correct bit patterns	Error Detected
1011	1011	Yes	1 st and 3 rd	0011	Yes
0011				1001	Yes
1001				0001	Yes

Basic Idea/Analysis

A. Tackling situation of double bit errors in same locations of all copies in APC with bit-reversed and Gray coded copy

The conventional APC scheme [11] can correct single or multiple bit error, if the errors are not in the same bit location of all the received erroneous copies. But APC scheme fail to handle the situation when atleast double bit errors occur in each received erroneous copy even if the errors are not in the same bit location of the copies. Say data packet '10010011' is received as '10010101','10100011','10011111', where each received copy has double or more bit error. The result of bit-by-bit majority voting is '10010111', APC scheme fail to generate corrected copy of this packet, as the brute force application would be quite complex to determine and search the correct bit pattern.

In order to tackle the situation of multiple bit errors where each received erroneous copy has at-least double bit error, we proposed a new modification of APC scheme. Under the proposed scheme transmitter will send the first copy as it is, second copy will be a bit reversed packet of the original packet, and third copy will be gray coded packet of the original packet. At the receiver side the first copy will be used as it is, second copy will be bit reversed, and the third copy will be converted from Gray coded packet to binary packet. The idea is illustrated with an example. It is assumed that data '10010011' is to be transmitted from transmitter to receiver. Under the proposed scheme first copy is copy₁ = 10010011, second copy is the bit reversed packet copy₂ = 11001001 and third copy is Gray coded of the original packet copy₃ = 11011010. Say the copies are received as copy₁^R = 10010101, copy₂^R = 11001111 and copy₃^R = 11010110. Receiver will bit reverse the second copy, copy₂^R = 11001111 → 11110011 and convert third copy from Gray code to binary copy₃^R = 11010110 → 10011011 and then perform majority voting. The result of majority voting is:

```
10010101
11110011
10011011
-----
10010011 → Correct copy is obtained.
```

With Gray code, double error is reduced to single bit-error. It is found that APC scheme can correct single bit error [13] except the case when errors occur in the bit location in all three copies. In case of odd number of bit errors, Gray code tends to spread the errors rather than reducing them. Thus APC with Gray coded copy may be useful for even number of bit-error only.

B. Tackling burst error in APC with bit-reversed and bit-shifted copy

As stated above the conventional APC scheme fails when error occur in the same bit position in all three erroneous copies received. In [18-19] authors have observed finger bit-error pattern, they show that bit errors are clustered within the frame in a regular pattern. Thus it is likely in wireless transmission that three copies transmitted at a time will have the same link error syndrome resulting into all three copies having error at same bit position(s). Also in [20], author found that the burst error with length 10 is very rare to occur. To detect and correct burst error of variable length, we proposed a new modification of APC scheme, in which the first copy will be the original copy as it is, second copy is bit-reversed packet of the original packet and third copy will be the bit-shifted version of the original copy, we proposed to shift by n/2 or 11 (if $n/2 > 11$) where 'n' is the number of bits in the packet. We would like to illustrate the idea with examples. In our examples considered we have obtained the third copy by left-shifting the original packet by n/2 bits. It is assumed that the data packet '1010' is to be transmitted from transmitter to receiver. Under the proposed scheme the first copy is copy₁ = 1010, second copy is copy₂ = 0101 and third copy is copy₃ = 1010. Say that the packets are received as copy₁^R = 1011, copy₂^R = 0100 and copy₃^R = 1011.

Receiver will bit reversed the second copy, copy₂^R = 0100 → 0010 and left-shift the third copy by 2 bits, copy₃^R = 1011 → 1110. And the receiver will perform bit by bit majority voting as:

```
1011
0010
1110
-----
1010 → Correct copy is obtained.
```

Let us assume that the data packet '11001001' is to be transmitted from transmitter to receiver. Under the proposed scheme, copy₁ = 11001001, second copy is the bit reversed of the original packet copy₂ = 10010011 and third copy is left-shifted by 'n/2=4' bits i.e., copy₃ = 10011100. Say the packets are received as copy₁^R = 11000101, copy₂^R = 10011111 and copy₃^R = 10010000. Receiver will use first copy as it is, bit reverse the second copy i.e., copy₂^R = 10011111 → 11111001 and left-shift the third copy by 4 bits i.e., copy₃^R = 10010000 → 00001001. Then receiver will perform bit by bit majority voting as:

```
11000101
11111001
00001001
-----
11001001 → correct copy is obtained.
```

With the above examples it is illustrated that modified APC with bit-reversed and bit-shifted copy can correct errors which occur in the same bit position in all the received erroneous copies, and also the burst error which occur in regular pattern.

C. Enhancing throughput using APC with selective repeat request

As stated before, traditional APC suffers from low throughput. In order to overcome this limitation, we proposed few modifications to traditional APC. Say transmitter has N number of packets to be transmitted, instead of transmitting three copies of first packet at a time as in conventional APC, in the proposed scheme transmitter will send a copy each of first three packets (say packet1, packet2 and packet3). Receiver will check for error in all three packets received, say one packet (packet1) is received correctly, and rest are erroneous, receiver will request retransmission for packet2 and packet3. Transmitter, on receiving re-transmission request for packet2 and packet3, will understand that packet1 is received correctly. So transmitter will resend a copy each of packet2 and packet3, and also send a copy of packet4. Say all three received copies are erroneous, receiver will perform packet combining scheme separately on received erroneous copies of packet2 and packet3. Say packet2 is corrected with PC scheme. Receiver will request re-transmission request for packet3 and packet4. Transmitter on receiving retransmission request for packet3 and packet4 understand that packet2 is corrected, so transmitter will retransmit copies of packet3 and packet4, and it will send first copy of packet5. At the receiver if all copies are erroneous, it will perform APC on packet3, PC on packet 4. If packet3 is corrected with APC, but PC

scheme fail to correct packet4, receiver will request re-transmission for packet4 and packet5. If packet3 and packet 4 are both corrected with APC and PC respectively, receiver will request for re-transmission of packet5 only. The modified APC scheme is shown in Fig. 1, with the assumption that first copy of packet1 is received with no error, packet2 is recovered with PC scheme and packet3 is recovered with APC scheme. The following analysis can be made for the proposed modified APC scheme:

- i. If any of packet are received correctly in the first transmission, and second packet get corrected with PC scheme, and third packet with APC, then the total number of copies transmitted for three packets will be $1+2+3 = 6$ copies, that is only two copies for each packet. Thus the aggregate throughput will be 50.00%.
- ii. If any of packets are received correctly in the first transmission, and rest packets get corrected with PC scheme, then the total number of copies transmitted for three packets will be $1+2+2 = 5$ copies. Thus the aggregate throughput will be 60.00%.
- iii. If all three packets get corrected with PC scheme, then the total number of copies transmitted for three packets will be $2+2+2 = 6$ copies, i.e., only two copies for each packet. Thus the aggregate throughput will be 50.00%.
- iv. In the case when all packets are corrected with APC scheme, then the total number of copies transmitted for three packets will be $3+3+3 = 9$ copies, i.e., only three copies for each packet. Thus the aggregate throughput will be 33.33%.
- v. One major advantage of APC is low latency. When APC corrects the erroneous copies by majority logic only one propagation time (tp) or Round Trip Transfer (RTT) delay is used. One tp or RTT is at best needed for a corrected packet in APC at best. In the proposed scheme, 3 tp or RTT are needed for 3 data packets, thus in aggregate ($3/3=1$) only one tp or RTT is needed for a packet. Thus modified APC scheme doesn't add any extra delay to the transmission.

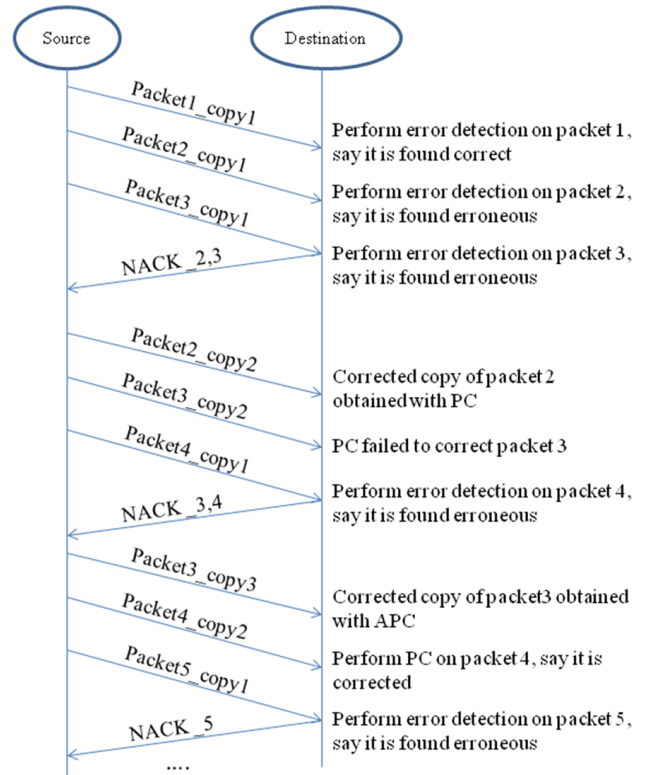


Fig. 1. Modified APC with selective repeat request

D. Combined protocol of APC with bit-reversed s& bit-shifted copy with selective repeat request

In order to further increase the correction capability of modified APC, we proposed to combine modified APC with bit-reversed & bit-shifted copy and APC with selective repeat request. In this proposed scheme, transmitter will send first copy as same as original copy, second copy as bit reversed of the original packet and third copy as 'n/2' bit shifted of original copy. The proposed modified APC scheme is shown in Fig. 2. At the receiver when all the three copies of the three packets are received erroneous, receiver will send a NACK and will not specify the packet number. When transmitter receives only NACK, it will understand that the copies of all three data packets are corrupted, so it will re-transmit copies of the packets, otherwise on receiving a NACK specified with packet number, transmitter will understand that only specified packet are to be re-transmitted along with copies of new data packets. In all case, the throughput of the proposed modified APC will be either better or same as conventional, but it will not be worse.

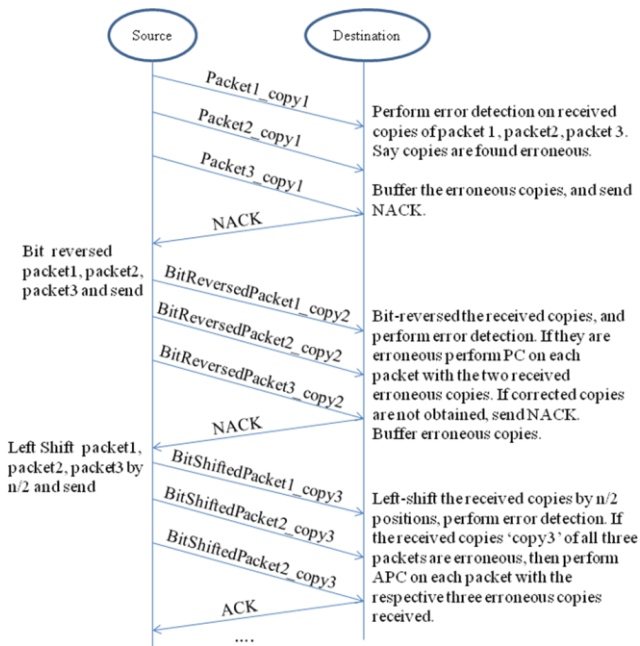


Fig. 2. Modified APC with bit-reversed & bit-shifted copy with selective repeat request

Conclusion

We have proposed few modifications of aggressive packet combining scheme for performance improvement. The capability of the proposed schemes to tackle the situation of double bit errors, regular burst errors are illustrated with examples. The modified APC scheme with bit-reversed and Gray coded copy can correct double bit errors, even if double bit errors are in the same bit location of the received erroneous copies. The modified APC scheme with bit-reversed and bit-shifted copy can correct single bit error when error occur in the same bit location of all received erroneous copies, also it can correct multiple bit errors even if errors occur in the same bit location of all received erroneous copies. The modified APC with selective repeat request scheme will enhance throughput by sending selective retransmission request. The modified APC with bit-reversed & bit-shifted copy with selective repeat request will give the optimum performance out of all the schemes proposed and discussed.

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