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A Gate Level Full Adder Design with Power Saving

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Abstract-Traditional full adder design consists of XOR, AND and OR gates. Model of full adder using multiplexers is proposed in literature. This model consists of XOR, XNOR, AND and OR gates along with multiplexers to realize the full adder. This paper proposes full adder model using XOR and multiplexers. The proposed model is synthesized using Quartus2 tool. The power consumed at gate, multiplexer level shows an improvement of 50% in the proposed model.

Keywords: ALU, Full adder, Power improvement

Introduction

Full adders add three bits producing sum and carryout. The inputs are usually designated as a,b,c. The outputs are designated as sum, carryout. Full adders are found in the ALU of the processor. Usually subtraction is done using two's complement addition which again uses full adders. Many applications involve addition/subtraction. Full adders play important role in computer power consumption. The truth table for the full adder is shown in TABLE.1.[1]. The expression for sum and carry out is given below

sum = $a \oplus b \oplus c$ (1)

carryout = ab + bc + ca (2)

To design full adder two XOR gates , three AND gates and two OR gates are required from (1) and (2). The authors in [2] suggest the CMOS technology to be used in full adder design. The authors in [3], [4] propose full adder model that uses multiplexers. This model gives the c input of full adder with inputs a, b, c as select line to multiplexer. The equations for the sum and carryout are defined as below.

If c=0, sum = $a \oplus b$ carryout = ab (3)

If c=1, sum = $\overline{a \oplus b}$ carryout = a+b (4)

TABLE. 1. Full Adder Truth Table

a	b	c	sum	carryout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The c input drives the multiplexers to realize the circuits for sum and carryout. This model calculates the XOR and XNOR values, AND and OR values for inputs a,b. This model is shown in Fig. 1. Two 2:1 multiplexers are used in this model. The input c drives the multiplexers. Full adder circuit based on majority function is proposed in [5]. It is known fact that the power consumption of digital circuit depends on the number of active components. The number of enabled gates contributes to the power consumption of the full adder in this regard. To save the power consumption it would be ideal to have minimum number of gates active during full adder operation. Designs of low power full adders with structured approach is presented in [6].

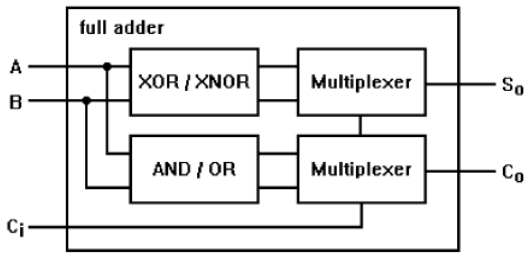

Fig.1. Full adder as proposed in [4]

This paper proposes full adder design based on the comparison of the input values a and b. Expressions for sum and carryout are derived for the various conditions. One XOR gate and two 2:1 multiplexers are required to realize the circuit using Quartus 2 at the schematic level. The total power consumed is calculated as the sum of the power consumed by the active components. The power consumed shows improvement of 50% over the model presented in [3]. There is reduction in number of active gates in the proposed model.

The rest of the paper is organized as follows. The proposed model, simulation, conclusion are given next followed by references.

Proposed Model

From TABLE.1 and equations (1), (2) the following is observed.

1. If a = b, sum = c , carryout = a (5)
2. If a !=b, sum = !c, carryout = c (6)

From (5), (6) above the values of inputs a and b has to be compared. Two 2:1 multiplexers can be used to realize the sum and carryout. The comparison of a and b can be done using comparator or XOR gate. The XOR gate implementation is valid only for two inputs to compare their equality. It cannot be generalized for any n-input circuit as XOR gives one if there are odd number of ones in the input. Based on the implementation, there is reduction in number of

gates and active components in the full adder circuit for the proposed model. The block diagram of the proposed model is shown in Fig. 2

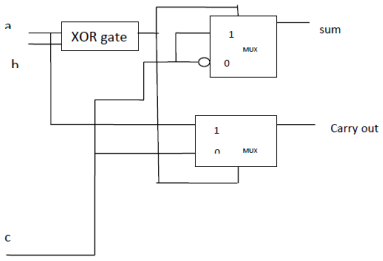

Fig.2. Block diagram of proposed full adder

Simulation

The proposed full adder model is simulated using Quartus 2 tool. Code in Verilog is written for the proposed logic. The code is compiled, synthesized using Quartus 2 tool. The schematic for the proposed model is shown in Fig. 3. The schematic for the model proposed in [4] is shown in Fig. 4. The schematic for the traditional full adder circuit is shown in Fig. 5. The power calculations are shown next.

For Fig. 3, the proposed design has one XOR gate and two 2:1 multiplexers. The power consumed is calculated below.
1. power for XOR gate : 66.99mW
2. power for two 2:1 MUX : 67.14+0.41 mW = 67.55mW
3. Total power : 134.54mW

For Fig. 4 the model proposed in [4] has one XOR, one AND, one OR gates, four 2:1 multiplexers. The power consumed is as below
1. power for XOR gate : 66.99mW
2. power for OR gate : 66.99mW
3. power for AND gate : 66.99mW
4. power for four 2:1 MUX : 67.14 + 3*0.41mW = 68.37mW
5. Total power : 269.34mW

Power savings : 67.81/289.34 = 0.50048 m= 50.048%

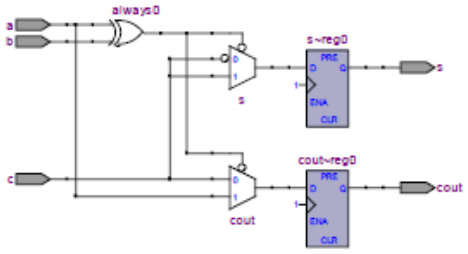

Fig.3. Schematic diagram of proposed design

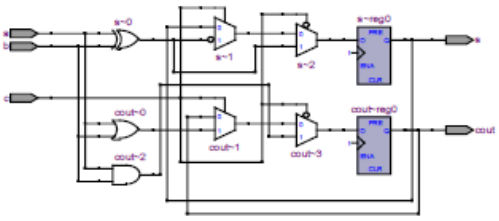

Fig. 4. Schematic diagram of design proposed in [4]

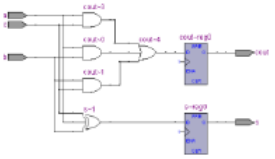

Fig. 5. Schematic diagram of Traditional full adder circuit

The traditional full adder model proposed in [1] is shown in Fig. 5. The model was simulated using Verilog code in Quartus 2. The power consumed is shown as below.

1. power for AND gate: (66.99 + 2*0.4)mW = 67.79mW
2. power for OR gate: 67.14mW
3. power for XOR gate: 67.14mW
4. Total: 202.07 mW

The power saving with proposed model = 67.53/202.07 = 33.42% .

The power calculated in this method shows that the power consumed in [1] is less than the power consumed in [4]. The power saving discussed in [4] is based on the CMOS technology. In this paper the simulations presented are at the logic gate level power consumption using Quartus2 tool for the proposed model and models proposed in [1] and [4]. As can be seen from Fig. 4 there are three distinct gates. In Fig. 5 though there are five gates there are only three distinct gates.

Conclusion

A full adder design with improved power consumption is proposed in this paper. The sum and carryout of the full adder are obtained based on the equivalence of two inputs a and b. The expressions for sum and carry are derived based on this condition. The proposed design is simulated with Quartus 2 tool. The schematic shows decrease in number of logic gates. The power consumed is calculated from power consumed by the active components in the circuit. There is 50% improvement in power savings over the model proposed in [4] and about 30% power saving over the traditional full adder circuit proposed in [1] for the chosen parameters.

References

[1] Morris Mano, "Computer System Architecture", 3rd edition, Pearson Printice Hall, 2007.

[2] A.Shams, M. Bayoumi, "Performance Evaluation of 1-bit CMOS Adder Cells", *Proc. ISCAS*, 1999.

[3] Mariano Aguirre-Hernandez, Monico Linares-Aranda, "CMOS Full Adders for Energy Efficient Arithmetic Applications", *IEEE Transactions on VLSI Systems*, Vol. 19, No.4, pp. 718-721, 2011.

[4] Mariano Auirre, Monico Linares, 2005, "An alternative logic approach to implement high-speed low-power full adder cells", *Proc. of SBCCI*, 2005.

[5] Vahid Foroutan, Keivan Navi, Majid Hagparast,"A New Low Power Dynamic Full Adder Cell Based on Majority Function", *World Applied Sciences Journal*, Vol. 4, pp. 133-141, 2008.

[6] Ahmed M.Shams, Magdy A. Bayoumi, " A Structured Approach for Designing Low Power Adders", *Proc. Thirty First Asilomar Conference on Signals, Systems & Computers*, 1997.