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# Design Of Novel Domino Circuits For High Performance And Energy Efficient Vlsi Implementation

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Abstract-In this work, a new domino circuit is proposed, which has a lower leakage and higher noise immunity without dramatic speed degradation for wide fan-in gates. The technique which is utilized in this work is based on comparison of mirrored current of the pull-up network with its worst case leakage current. The proposed circuit technique decreases the parasitic capacitance on the dynamic node, yielding a smaller keeper for wide fan-in gates to implement fast and robust circuits. Thus, the contention current and consequently power consumption and delay are going to be reduced.The leakage current is expected to be decreased by exploiting the footer transistor in diode configuration, which results in increased noise immunity. The proposed circuits are simulated in detail by performing transistor level simulations.We investigate PVT variations on the performance of the proposed circuits and we compare with the existing techniques.

Keywords- Domino logic, leakage-tolerant, noise immunity, wide fan-in.

## INTRODUCTION

Dynamic logic such as domino logic is widely used in many applications to achieve high performance,which cannot be achieved with static logic styles.However,the main drawback of dynamic logic families is that they are more sensitive to noise than static logic styles .on the other hand,as the technology scales down,the supply voltage is reduced for low power,and the threshold voltage(vth)is also scaled down to achieve high performance.since reducing the threshold voltage exponentially increases the subthershold leakage current,reduction of leakage current,reduction of leakage current and improving noise immunity are of major concern in robust and high performance designs in recent technology generations,especially for wide fan-in dynamic gates which are typically employed in the read path of register files, match lines of ternary content addressable memories, flash memories, tag comparators, programmable logic arrays, and wide multiplexer-flip-flop(MUX)and De-MUX.

However for wide fan-in dynamics gates ,especially for wide fan-in or gates,robustness and performance significantly degrade with increasing leakage current. as a result, it is difficult to obtain satisfactory robustness-performance tradeoffs.

In this paper, a new current-comparison-based domino(CCD)circuit for wide fan-in applications in ultadeep sub micrometer technologies is proposed .the novelty of the proposed circuit is that our work simultaneously increases performance and decreases leakage power consumption.

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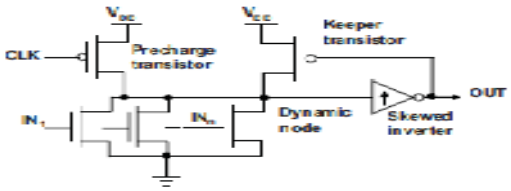
## LITERATURE RIVEW

Domino logic circuit is formed by adding a static CMOS inverter to the output of dynamic CMOS logic. The idea of forming domino logic is to limit charge leakage and charge sharing by feeding back the inverting output. Major drawback of domino logic circuit is more sensitive to noise than static logic families..On the other hand, Power consumption is one of the important factor in present days especially for portable devices.one way to achieve low power is scaling down the supply voltage.as supply voltage reduce, the threshold voltage(vth) of transistors are reduced.however lowering he threshold voltage leads to an exponential increase of subthreshold leakage current.

The most popular dynamic logic is the conventional standard domino circuit as shown in Fig. 1. In this design, a pMOS keeper transistor is employed to prevent any undesired discharging at the dynamic node due to the leakage currents and charge sharing of the pull-down network (PDN) during the evaluation phase, hence improving the robustness. The keeper ratio $K$ is defined as

$$K = \frac{\mu_p \left(\frac{W}{T}\right)_{\text{Keeper-transistor}}}{\mu_n \left(\frac{W}{T}\right)_{\text{evaluation-network}}}$$

Fig1.




SFLD adopted from [4].

Where w and l denote the transistor size,and $\mu_n$ and $\mu_p$ are the electron and hole mobilities,respectively.however the traditional keeper approach is less effective in new generations.Thus,it increases power consumption and evalution delay of standard domino circuits.these problems are more critical in wide fan-in dynamic gates due to the large number of leaky nmos transistors connected to the dynamicnode.

There is trade of between robustness and performance, and the number of pull-down legs is limited. the existing techniques try to compromise one feature to gain at the expense of the others Several circuits techniques are proposed in the literature to address these issues. these circuit techiniques can be divided into two categories. In the first category, circuit techniques change the controlling circuit of the gate voltage of the keeper such as conditional-keeper domino (CKD),high speed domino(HSD),leakage current replica(LCR)keeper domino, and controlled keeper by current-comparison domino(CKCCD) respectively. On the other hand, in the second category, designs including the proposed designs change the circuit topology of the footer transistor or reengineering the evaluation network such as diode-footed domino(DFD)and diode-partitioned domino(DPD).

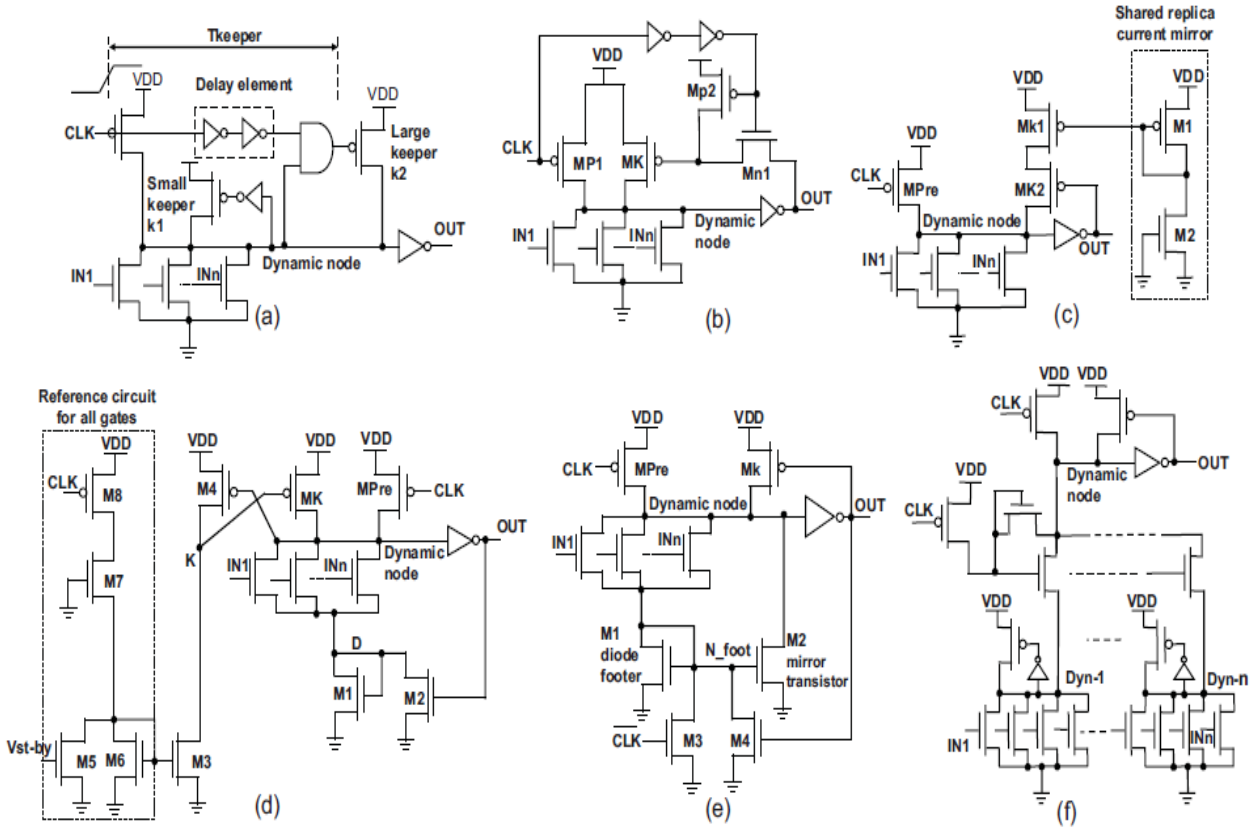



Fig. 2. (a) CKD [5]. (b) HSD [6]. (c) LCR keeper [7]. (d) CKCCD [8]. (e) DFD [4]. (f) DPD [9].

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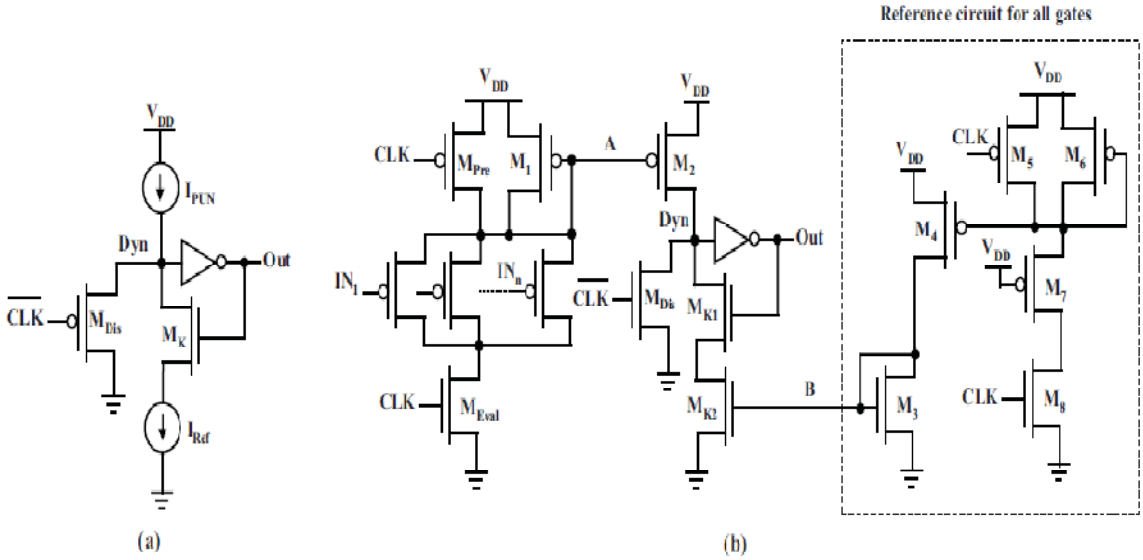


Fig. 3. (a) Concept of proposed circuit (CCD). (b) Implementation of wide OR gate using CCD.

**PROPOSED CCD DESIGN**

Since in wide fan-in gates,the capacitance of the dynamic node is large ,speed is decreased dramatically. In addition, noise immunity of the gate is reduced due to many parallel leaky paths in wide gates. Although upsizing the keeper transistor can improve noise robustness, power consumption and delay are increased due to large contention. these problems would be solved if the PDN implements logical function,is separated from the keeper transistor by using a comparison stage in which the current of the pull-up network(PUN) is compared with the worst case leakage current.

Which utilizes the PUN instead of the PDN.In fact, there is a race between the PUN(which utilizes the PUN instead of the PDN. In fact, there is a race between the PUN and the reference current. Transistor $M_K$ is added in series with the reference current to reduce power consumption when the voltage of the output node has fallen to ground voltage.

An important issue in the generation of the reference voltage, which is the correct variation of the reference current according to the process variations to maintain the robustness of the proposed circuit. Process variations are due to ran- dom and systematic parameter fluctuations . In random variations, parameters of each device vary individually and independent of adjacent devices. However, systematic varia- tions affect the parameters of neighborhood transistors in the same way, yielding a strong correlation between parameters of nearby devices . In this paper, systematic variations are considered. We have assumed that in a given circuit design the threshold voltage of all nMOS transistors varies together and that of pMOS transistors varies together. In the proposed circuit, effects of any threshold voltage variation on the voltage of nodes A and B is important because it directly affects the speed of the gate, and consequently power consumption and noise immunity. The worst scenario is that the threshold voltage of nMOS transistors is decreased and that of the pMOS transistors is increased, i.e., fast nMOS and slow pMOS due to process variations. In the former case, the subthreshold leakage of pMOS transistors of the PUN is decreased, thus the reference current must be reduced and vice versa for the latter case. Therefore, the reference current must be varied

according to threshold voltage variations to maintain robustness in this design. To track process variations in dynamic logic circuits, several solutions are proposed in the literature by using a process variation sensor such as one based on drain-induced barrier lowering (DIBL) effect , rate sensing keeper , and replica keeper current. In the proposed circuit, a replica circuit like that proposed by can be used as a leakage current sensor for proper operation and superior performance, in the worst case of fan-in, i.e., a64-input OR gate because of its maximum leakage current among other gates.

The proposed circuit for generation of reference current for all gates is shown in Fig. 3(b). This circuit is similar to a replica leakage circuit proposed by in which a series diode-connection transistor $M_6$ similar to $M_1$ is added. In fact, as shown in Fig. 3(b), this circuit was a replica of the worst case leakage current of the PUN to correctly track leakage current variations due to process variations. Therefore, the gate of transistor $M_7$ is connected to $V_{DD}$, and its size is derived from the sizes of pMOS transistors of the PUN in the worst case, i.e., a 64-input OR gate, and hence its width is set equal to the sum of the widths of 64 pMOS transistors of the PUN. In the proposed CCD circuit, as shown in Fig. 3(b), current of the PUN is mirrored by transistor $M_2$ and compared with the reference current, which replicates the leakage current of the PUN. The topology of the keeper transistors and the reference circuit, which is shared for all gates, is similar to that proposed in , which successfully tracked the process, volt- age and temperature variations. The proposed circuit employs pMOS transistors to implement logical function, as shown in Fig. 3(b). Using the N-well process, source and body terminals of the pMOS transistors can be connected together such that the body effect is eliminated. By this means, the threshold voltage of transistors is only varied due to the process variation and not the body effect. Moreover, utilizing pMOS transistors instead of nMOS ones in the N-well process, it is possible to prevent increasing the threshold voltage due to the body effect in existence of a voltage drop due to the diode configuration of transistor $M_1$, yielding decreasing the delay.

In other words, one can use nMOS transistors in the P-well process to achieve a higher speed due to their higher mobility. Although slower mobility of pMOS transistors decreases the speed, decreasing the capacitance of the dynamic node in the proposed circuit enables it to increase speed by proper choice of the mirror ratio $M$ . the proposed circuit has five additional transistors and a shared reference circuit compared to standard footless domino (SFLD). The proposed circuit can be considered as two stages. The first stage preevaluation network includes the PUN and transistors $M_{\mathrm{Pre}}$ , $M_{\mathrm{Eval}}$ , and $M_1$ . The PUN, which implements the desired logic function is disconnected from dynamic node Dyn, unlike traditional dynamic logic circuits, and indirectly changes the dynamic voltage. The second stage looks like a footless domino with one input [node A as input in Fig. 3(b)], without any charge sharing, one transistor $M_2$ regardless of the implemented Boolean function in the PUN, and a controlled keeper consists of two transistors. Only one pull-up transistor is connected to the dynamic node instead of the $n$-transistor in the $n$-bit OR gate to reduce capacitance on the dynamic node, yielding a higher speed. The input signal of the second stage is prepared by the first stage. In the evaluation phase, thus, the dynamic power consumption consists of two parts: one part for the first stage and the other for the second stage. As we know the dynamic power consumption directly depends on the capacitance, voltage swing, and contention current on the switching node in the constant condition for frequency, power supply, and temperature. The first stage with $n$-input has a lower voltage swing $V_{DD}$ to $V_{THP}$ and no contention. On the other hand, the second stage has rail-to-rail voltage swing with minimum contention. Although the proposed circuit has some area overhead, it has less dynamic power consumption compared to footless domino.

TABLE.1.Comparision of Normalized FOM in 64 Inputs OR GATE UNDER SAME DELAY

| | Standard Footless domino (SFLD) | CKD | High-speed Domino (HSD) | Diode Footed Domino (DFD) | Leakage Current Replica (LCR) | Diode-partitioned Domino (DPD) | CKCCD | Proposed Domino (CCD) |
|---|---|---|---|---|---|---|---|---|
| No of Transistors | 68 | 79 | 76 | 72 | 69 | 134 | 74 | 73 |
| Standard Deviation of Delay | 0.27892 | 0.31935 | 031488 | 0.33189 | 0.25201 | 0.39703 | 0.32712 | 0.3382 |
| Normalized Standard Deviation of Delay(ps) | 0.26157 | 0.31362 | 0.305 | 0.32412 | 0.25001 | 0.42326 | 0.32984 | 0.33809 |
| Area | 127 | 169 | 137 | 171 | 144 | 223 | 198 | 133 |
| Normalized Area | 1 | 1 | 1.08 | 1.35 | 1.14 | 1.76 | 1.56 | 1.05 |
| Power | 1.77E-06 | 1.44E-06 | 3.10E-06 | 8.64E-06 | 1.75E-06 | 3.39E-06 | 2.14E-06 | 7.48E-06 |
| Normalized Delay | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Transistor $M_1$ is configured in diode connection, i.e., its gate and drain terminal are connected together. In the evaluation mode, the current of the PUN transistors establishes some voltage drop across $M_1$ . This voltage will be low, if all inputs are at the high level and only leakage current exists in the PUN and mirror transistor $M_2$ . Otherwise, if at least one conductive path exists between node A and ground, for example, level of one input becomes low in the OR gate, this voltage drop is raised up, turning on mirror transistor $M_2$ and changing the output voltage.

The voltage drop across transistor $M_1$ causes the gate-source voltage of the off transistors in the PUN to become positive, yielding an exponential reduction in subthreshold leakage due to the phenomenon called the stacking effect. It should be noted that if the body effect is not eliminated due to the unequal voltage of the source and body terminals, the leakage current will be decreased further at the expense of higher deviation due to process variations.

The voltage across the diode footer in other domino circuits that use diode-footed techniques such as and must be decreased to zero in order to lower the dynamic node voltage to zero. But in the proposed circuit, it is not necessary for this voltage to reach 0 V since the current of the diode footer is needed instead of the voltage across it. Therefore, the size of the diode-footer transistor $M_1$ in the proposed circuit is smaller than other DFD circuits. Consequently, a lower leakage current must be compensated by the keeper transistors instead of

The larger one in the other circuit due to the larger size of the footer and mirror transistors. This results in lower delay and power consumption and

area overhead. On the other hand, in the next predischarge mode, the dynamic node is charged from nonzero voltage to power supply voltage, yielding reduction in the power consumption with respect to existence of the large capacitance on the dynamic node in wide fan-in gates, especially wide fan-in OR gates. In addition, since transistor $M_1$ increases the switching threshold voltage of the pMOS transistors, the new switching threshold voltage of the gate is about twice the threshold voltage of the pMOS devices.

Since upsizing of transistor $M_2$ increases the speed, the mirror ratio $M$ is defined as the ratio of the size of transistor $M_2$ to the size of transistor $M_1$With reference to the circuit schematic shown in Fig. 3(b), two phases of the proposed circuit are explained in detail as follows.

### *Presdischharge Phase*

Input signals and clock voltage are in high and low levels, respectively, [CLK = "0", CLK = "1" in Fig. 3(b)] in this phase. Therefore, the voltages of the dynamic node (Dyn) and

node $A$ have fallen to the low level by transistor $M_{\mathrm{Dis}}$ and raised to the high level by transistor $M_{\mathrm{pre}}$, respectively.

Hence, transistors $M_{\mathrm{pre}}$, $M_{\mathrm{Dis}}$, $M_{k1}$, and $M_{k2}$ are on and transistors $M_1$, $M_2$, and $M_{\mathrm{Eval}}$ are off. Also, the output voltage is raised to the high level by the output inverter.

### *Evaluation Phase*

In this phase, clock voltage is in the high level [CLK = "1", CLK = "0" in Fig. 3(b)] and input signals can be in the low level. Hence, transistors $M_{\mathrm{pre}}$ and $M_{\mathrm{Dis}}$ are off, transistor$M_1$, $M_2$, $M_{k2}$, and $M_{\mathrm{Eval}}$ are on, and transistor $M_{k1}$ can become on or off depending on input voltages. Thus, two states may occur. First, all of the input signals remain high. Second, at least one input falls to the low level. In the first state, a small amount of voltage is established across transistor $M_1$ due to the leakage current. Although this leakage current is mirrored by transistor $M_2$, the keeper transistors of the second stage ($M_{k1}$ and $M_{k2}$) compensate this mirrored leakage current.

It is clear that upsizing the transistor $M_1$ and increasing the mirror ratio ($M$) increase the speed due to higher mirrored With reference to the circuit schematic shown in Fig. 3(b), two phases of the proposed circuit are explained in detail as follows.

In this phase, clock voltage is in the high level [CLK = "1", CLK = "0" in Fig. 3(b)] and input signals can be in the low level. Hence, transistors $M_{\mathrm{pre}}$ and $M_{\mathrm{Dies}}$ are off, transistor$1$, $M_2$, $M_{k2}$, and $M_{\mathrm{Evil}}$ are on, and transistor $M_{k1}$ can become on or off depending on input voltages. Thus, two states may occur. First, all of the input signals remain high. Second, at least one input falls to the low level. In the first state, a small amount of voltage is established across transistor $M_1$ due to the leakage current. Although this leakage current is mirrored by transistor $M_2$, the keeper transistors of the second stage ($M_{k1}$ and $M_{k2}$) compensate this mirrored leakage current. It is clear that upsizing the transistor $M_1$ and increasing the mirror ratio ($M$) increase the speed due to higher mirrored current at the expense of noise-immunity degradation. In the second state, when at least one conduction path exists, the pull-up current flow is raised and the voltage of node A is decreased to nonzero voltage, which is equal to gate-source voltage of the saturated transistor $M_1$. This voltage is also equal to drain-source voltage of $M_1$ and depends on mirrored current in transistor $M_2$, thus voltage of the dynamic node Dynamic is charged to $V_{\mathrm{DD}}$, yielding discharging the voltage of the output node and turning off the main keeper transistor $M_{k1}$. By this technique the contention current between the keeper transistor and the mirror transistor is mitigated. The below tables are normalized tables of delay.

TABLE.2. Comparision of normalized UNGs (Under Same Delay)

| Fan_in | Standard Footless domino (SFLD) | CKD | High-speed Domino (HSD) | Diode Footed Domino (DFD) | Leakage Current Replica (LCR) | Diode-partitioned Domino (DPD) | CKCCD | Proposed Domino (CCD) | Fan_in For |
|---|---|---|---|---|---|---|---|---|---|
| 8 | 11.44 | 82.10 | 36.5 | 18.69 | 60.5 | 108.5 | 14.6 | 2.04 | UNG |
| | 1.77 | 14.48 | 7.31 | 9.9 | 8 | 43.9 | 18.8 | 21.31 | NOR..UNG |
| 16 | 11.44 | 82.10 | 36.5 | 18.69 | 60.5 | 108.5 | 14.6 | 2.2 | UNG |
| | 1.77 | 14.48 | 7.31 | 9.9 | 12.51 | 43.9 | 22.82 | 21.31 | NOR..UNG |
| 32 | 11.44 | 82.10 | 36.5 | 18.69 | 60.5 | 108.5 | 14.6 | 2.04 | UNG |
| | 1.77 | 14.48 | 7.31 | 9.9 | 12.51 | 43.9 | 26.56 | 22.54 | NOR..UNG |
| 64 | 11.44 | 82.10 | 36.5 | 18.69 | 60.5 | 108.5 | 19.53 | 2.04 | UNG |
| | 1.77 | 14.48 | 7.31 | 9.9 | 12.51 | 43.9 | 14.73 | 22.94 | NOR..UNG |

## PVT Variations of Proposed Circuits

Process voltage temperature variations of current comparison domino for wide OR gate.

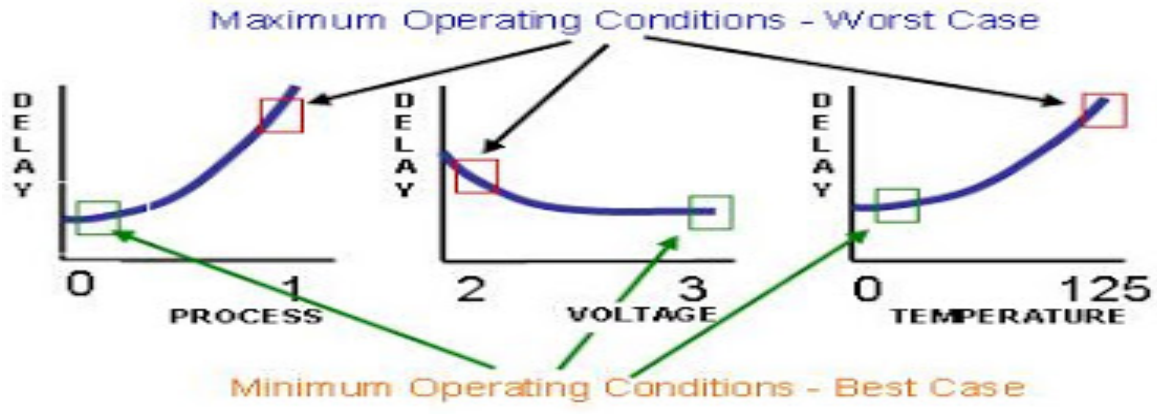

TABLE.3.Voltage Variation

| CCD | | |
|---|---|---|
| SUPPLY VOLTAGE | DELAY | AVG-POWER |
| 0.5 | 20.096n | 6.4058E-07 |
| 0.6 | 20.044n | 1.5396E-06 |
| 0.7 | 20.028n | 3.3360E-06 |
| 0.8 | 30.006n | 6.7457E-06 |
| 0.9 | 30.005n | 1.3255E-05 |

TABLE.4.Tempareture variation

| CCD | | |
|---|---|---|
| TEMPERATURE | DELAY | AVG-POWER |
| 10 | 30.006n | 7.7855E-06 |
| 40 | 30.006n | 7.2372E-06 |
| 80 | 30.007n | 6.8425E-06 |
| 110 | 30.007n | 6.7457E-06 |

TABLE.5.Process Variation

| CCD | | | |
|---|---|---|---|
| THRESHOLD VOLTAGE | | DELAY | AVG-POWER |
| +Vth0 | -Vth0 | | |
| 0.18191 | -0.1862 | 30.006n | 2.6934E-05 |
| 0.28191 | -0.2862 | 30.007n | 6.7457E-06 |
| 0.38191 | -0.3862 | 30.01n | 1.7978E-06 |
| 0.48191 | -0.4862 | 30.015n | 4.3515E-07 |
| 0.58191 | -0.5862 | 30.025n | 1.7300E-07 |

## IV.CONCLUSION

The leakage current of the evaluation network of dynamic gates was dramatically increased with technology scaling, especially in wide domino gates, yielding reduced noise immu- nity and increased power consumption. Thus, new designs were necessary to obtain desired noise robustness in very wide fan-in circuits. Moreover, increasing the fan-in not only reduced the worst case delay, it also increased the contention between the keeper transistor and the evaluation network. A new circuit design that we called CCD was proposed in this paper. The main goal was to make the domino cir- cuits more robust and with low leakage without significant performance degradation or increased power consumption. This was done by comparing the evaluation current of the gate with the leakage current. By using this technique, the proposed domino circuit reduced the parasitic capacitance on the dynamic node and keeper size of very high fan-in gates Using the high-performance PTM V2.1 of 16 nm [3] at a power supply of 0.8 V, wide fan-in 8- to 64-bit OR gate circuits were used as a benchmark. The proposed design plus several existing circuit designs were simulated and compared. Simulation results demonstrated significant progress in leakage reduction and acceptable speed for high-speed applications. Furthermore, they demonstrated that the proposed circuit had a very high UNG for wide fan-in OR gates compared to other designs. Thus, the proposed CCD was especially suitable for implementing wide fan-in Boolean logic functions with high noise immunity, lower area consumption, time delay, and power consumption.

Moreover, a normalized FOM, previously proposed by the authors, was modified to include standard deviation of delay. The proposed circuit demonstrated FOM of 2.76 times its counterparts in footless domino OR gates for the 64-bit OR gate. Therefore, the proposed circuit was superior to existing designs that were studied in detail in this paper, especially for wide fan-in gates.

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