International Journal of Applied Engineering Research ISSN 0973-4562 Volume 10, Number 17 (2015) pp 38214-38218

Design And Implementation Of Resistive Threshold Logic In Dsm Technology

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Abstract- In this project a resistance based threshold logic family which is useful in mimicking brain like large variable logic functions in VLSI is proposed. The concept of resistive threshold logic which minimizes the number of components and design complexity in order to implement large variable Boolean logic functions such as multiplexers, adders is presented. A universal Boolean logic cell based on an analog resistive divider and threshold logic circuit is proposed. Resistive threshold logic comprises of a resistive divider and a threshold logic circuit. The resistive divider is implemented by using active resistors, and provides output voltage as the summation of weighted products of input voltage. The output of this resistive divider is converted as a binary value by a threshold operation, which in turn is implemented by using CMOS inverter. Thus a universal cell structure is presented in order to reduce the overall implementation complexity and in some applications where the number of input variables increases to a very high number this proposed cell is expected to offer an advantage of lesser silicon area, simplicity in designing and enhanced performance when compared to the respective conventional CMOS logic circuits. Experimental results show that this proposed resistive threshold logic features a reliable reduction in circuit area, power dissipation in comparison with CMOS logic design. Synthesis and simulation can be done by using Tanner EDA.

Index Terms-- CMOS logic circuits, active resistors, resistive circuits, threshold logic, multiplexers, adders, DSM technology, Tanner EDA.

INTRODUCTION

Boolean algebraic expressions obtained from truth tables are implemented by using the logic gates. In digital integrated circuits like microprocessors and ASICs with the increase in functional requirements resulted in complex logic state implementations. When these complex set of logic states are represented in the form of a truth table they may result in having a large number of input and output variables. As when the number of input variables increases, it may not be possible to manually reduce these boolean logic expressions to reduce the number of components required for its implementation. For this the most common approach used to reduce the number of components required with a large number of variables is by using logic minimization based on prime implicant logics. Techniques, such as Karnaugh map [1], QuineMcCluskey [2], Petrick's method, Buchberger's algorithm [3], and Espresso minimization algorithm [4], are the most commonly used approaches. But, when there is significant increase in number of inputs, these logic minimization techniques may also be not that efficient. In addition to this, the implementations which are made by using these existing logic families become challenging as they are often restricted by the gate delays, the number of inputs, and the number of components. The common approach employed to implement boolean algebra with a large number (>10) of variables, is to apply the minimization techniques for standard gates with a limited number of inputs (<10). But this always leads to increase in number of circuit elements results in more number of circuit elements than that was possible with gates that could support as many number of inputs as the number of variables. In addition to this issue, from one boolean logic to another, to implement a gate the required components number may vary, thus resulting in increased structural complexity and imparting the difficulties in production scale verification ant testing cycles.

Generic digital circuits, like adders can be used to implement *n*-input boolean logic functions. In order to implement 4bit or 8bit or 16 bit adders inputs to the basic logic gates increases, a typical AND-OR logic will have large number of inputs per each gate for its implementation. Hence in implementing large variable boolean logic functions, we

introduce the concept of resistance threshold logic with which design complexity number of components can be reduced. The proposed resistive threshold logic is made up of a resistive divider and a threshold logic circuit.

PROPOSED CELL

The proposed logic cell, shown in Fig. 1, has a resistive divider and a variable threshold inverter. Digital values which can be equated to the digital logic gate's logic inputs are the inputs to the resistive divider. Depending upon the predefined inverter threshold and the output of the resistive divider, we propose to implement the basic Boolean logic functions.

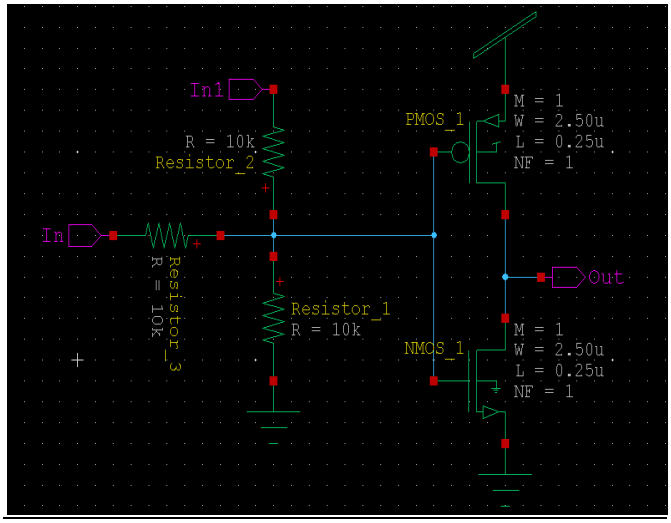

Fig. 1. Circuit diagram of the proposed resistive divider Boolean logic cell that consists of a two input resistive divider and a variable *threshold CMOS inverter*

An *N*-input resistance divider circuit consists of one reference resistor R_0 and *N* input resistors *Ri*. The output voltage V_0 for N-input voltage V_i can be represented as: $V_0 = \sum_{i=1}^{N}(Vi/Ri)/[(1/R0) + \sum_{i=1}^{N}(1/Ri)]$ .The inputs V_i may have either the logical level V_H or V_L representing a binary logic [1, 0]. We keep equal values to R_i's and $R_0 = mR_i$, which results in: $V_0 = (\sum_{i=1}^{N} Vi)/[(1/m) + N]$.

LITERATURE SURVEY

One simple approach to implement the resistors used in the resistive divider circuit is by using semiconductor resistors. These semiconductor resistors are made up of a resistive body which is surrounded by an insulator and is developed over a substrate, two contact terminals are implemented by using conductive metallic strips. The semiconductor resistance value is obtained from the expression, $(\rho L)/(X_j W)$, where ρ is the resistivity, L is the length, X_j is the thickness of the layer, and W is the resistive body width. But when the number of inputs increases while using these semiconductor resistors, the leakage current becomes very high through the semiconductor resistors. Hence to overcome this drawback the semiconductor resistors are being replaced with active resistors [5].

Three terminal transistor the active device, by proper connection it can be converted into a two terminal device resistor called an active resistor. This active resistor can be implemented by simply connecting the gate of an n-channel or p-channel enhancement MOS device to the drain. For the n-channel device the source should be placed at the most negative power supply voltage V_{ss} if possible in order to eliminate the bulk effect, the source of the p-channel device should be taken to the most positive voltage for the same reason.. This active resistors can be used in place of polysilicon7 or diffused semiconductor resistors as they offer small signal resistance and also can be used to produce a DC voltage thus when the number of inputs increases the active resistor usage reduces the area consumption and also the collective forward current through the circuit does not increase significantly when compared to using of semiconductor resistors.

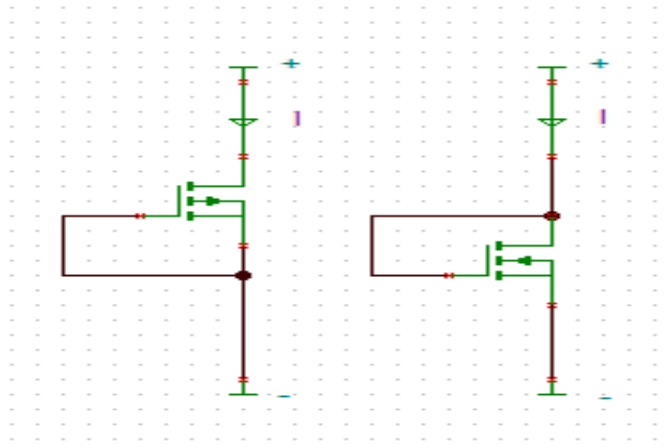

Fig.2. (a) n-channel enhancement active resistor
(b) p-channel enhancement active resistor

TABLE.I.TRUTH TABLE OF TWO INPUT RESISTIVE DIVIDER LOGIC CELL WHEN USED AS NAND AND NOR GATES

Input Voltage (*Vi*)		Output Voltage	NAND	NOR
V_1	V_2	V_0		
V_L	V_L	$2V_L/3$	V_H	V_H
V_L	V_H	$(V_L+V_H)/3$	V_H	V_L
V_H	V_L	$(V_L+V_H)/3$	V_H	V_L
V_H	V_H	$2V_H/3$	V_L	V_L

Threshold range of NAND: $(V_L+V_H)/3 < Vth < 2V_H/3$
Threshold range of NOR: $2V_L/3 < Vth < (V_L+V_{H)3}$

Table.1 shows the truth table of a resistive divider logic cell with two inputs, that implements the NAND and NOR gates by using a predefined inverter threshold Vth. Assuming that V_{DD} = 1V, V_H= 1V, V_L = 0V, from the above table it is clear that if the threshold voltage of the inverter is set between 0V and 1/3V, the cell works as NOR logic and if it is between 2/3V and 1/3V the cell works as NAND logic. That means by varying the threshold voltage of the inverter, NAND and NOR logic can be implemented using a single cell.

Generally the range of threshold voltage, Vth of NOR gate is $(NmV_L/(1 + Nm)) \leq V_{th} \leq (((V_H + (N-1)V_L)m)/(Nm + 1))$, and NAND gate is, $((m(V_L + (N-1)V_H))/(Nm + 1)) \leq V_{th} \leq (mNV_H/(Nm + 1))$. To find the m value, the lower limit of NAND gate threshold range $(m(V_L + (N-1)V_H)/(Nm + 1))$ is equated to $(V_H + V_L)/2$. Now by assuming that V_L= 0V then we get the m value as 1/(N – 2) hence we can say that the threshold voltage of NAND gate must be between $(V_H + V_L)/2$ and $mNV_H/(Nm + 1)$.

The threshold voltage of the MOSFET dependends on many parameters, like substrate bias voltage Vbs, the surface potential φs , and substrate doping concentration. The threshold voltage Vtn of the MOSFET can be varied by changing its substrate bias, Vbs. The dependence of substrate bias and the threshold voltage is expressed as, $Vtn = Vtn_0 + K_1(\sqrt{\varphi s - Vbs} - \sqrt{\varphi s}) + C$ where Vtn_0 is the zero bias threshold voltage, the surface potential $\varphi s = 2(k_B T/q) \ln(Na/n_i)$, K1 is a parameter derived by considering non-uniform doping and short channel effects $K1 = \gamma 2 - 2K2\sqrt{\varphi s - Vbm}$ where $K2 = (\gamma 1 - \gamma 2)(\sqrt{\varphi - Vbx} - \sqrt{\varphi s})/2\sqrt{\varphi s}(\sqrt{\varphi s - Vbm} - \sqrt{\varphi s}) + V_{bm}$, γ1 and γ2 are body bias coefficient when substrate doping concentration is equal to N_{ch} and N_{sub}, respectively. $\gamma 1 = \sqrt{2q \in Si Nch/Cox}$, $\gamma 2 = \sqrt{2q \in Si Nsub/Cox}$ and V_{bm} is the maximum substrate bias voltage. And C shows the effect of narrow channel on threshold voltage. The threshold voltage of the inverter can be represented as, $Vth = ((Vtn + (V_{DD} - |Vtp|)\sqrt{\mu pWp/\mu nWn}) / (1 + \sqrt{\mu pWp/\mu nWn})$, which shows the role of the threshold voltages of the MOSFETs in determining the threshold of the inverter.

APPLICATION DESIGN

The conventional CMOS design of 16-bit full adder [6][7] is compared with the proposed logic and the simulation is performed in Tanner EDA using a feature size of 0.25μm^2.

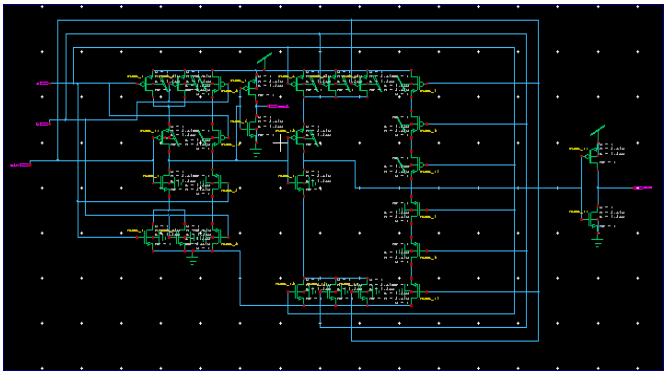

Fig.3. conventional CMOS schematic diagram of Full Adder

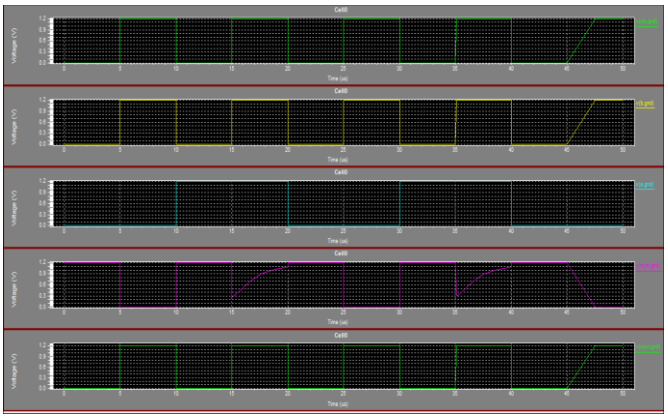

Fig.4. Schematic Wave Form

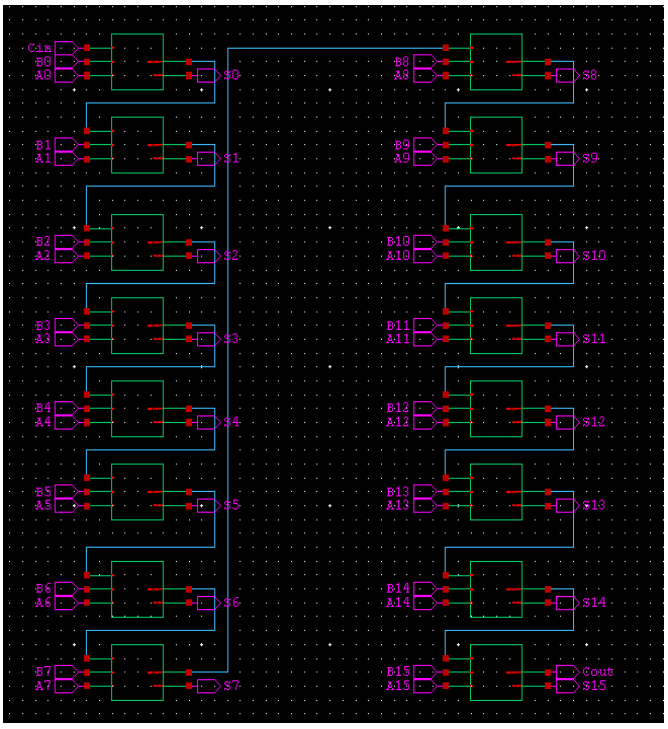

Fig.5. Conventional CMOS schematic diagram of 16Bit Adder

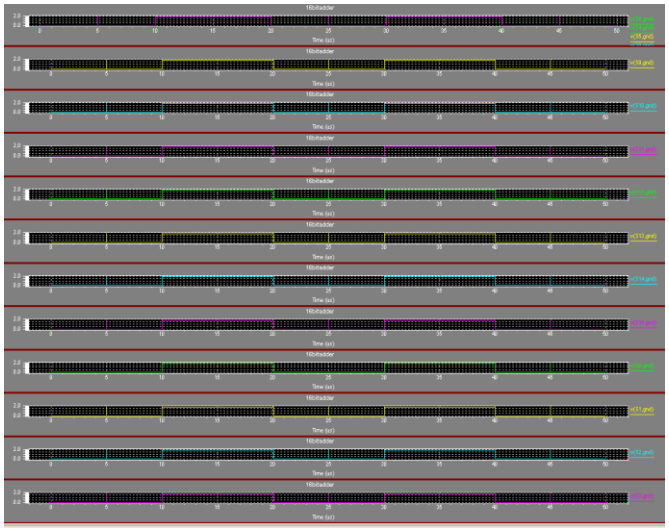

Fig.6. Schematic Wave Form

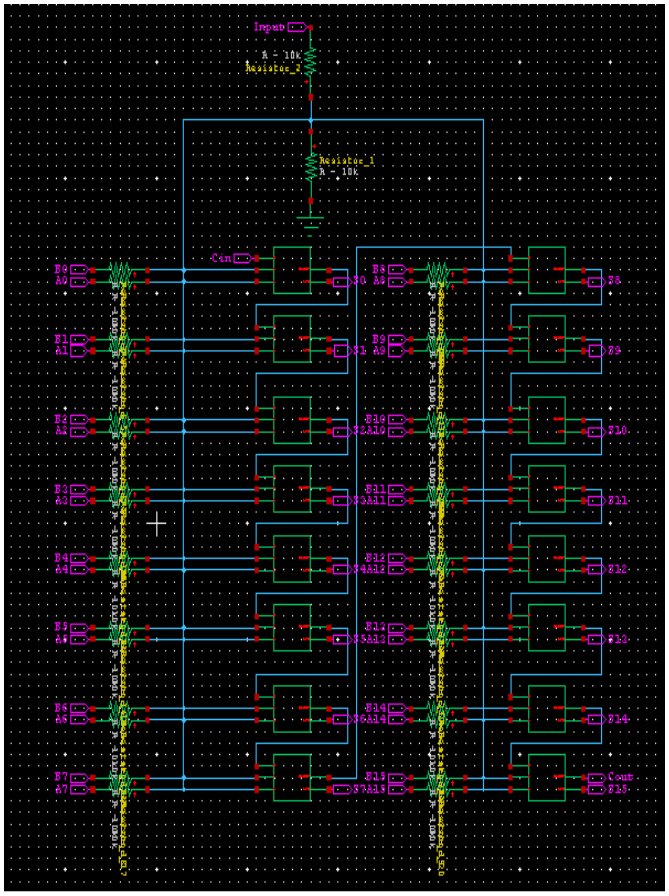

Fig.7. Implementation of 16Bit Adder using proposed logic

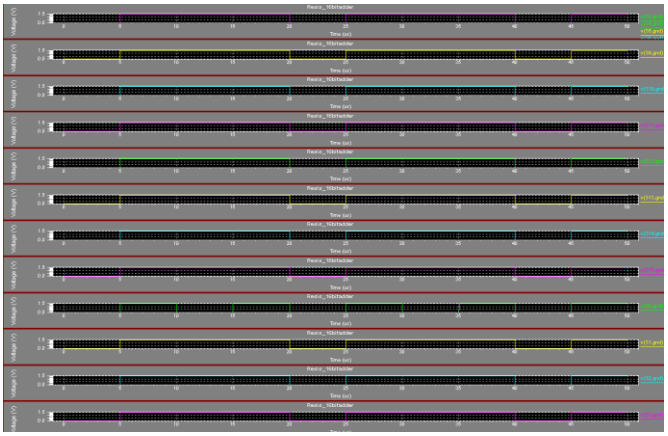

Fig.8. Schematic Wave Form

SYNTHESIS REPORT

TABLE.2.COMPARISON OF 16BIT FULL ADDER CIRCUIT IMPLEMENTED USING RESISTIVE THRESHOLD LOGIC WITH THAT OF CMOS LOGIC

Parameter	**L**ogic Family	
	CMOS logic	Resistive logic
Temperature	25 (deg C)	25 (deg C)
Average Power consumed	4.124579e-006w	4.650816e-003w
Static Power dissipation	6.26122e-002w	4.077555e-002w
Dynamic Power dissipation	5.502783e-007w	2.0389376e-009w
Nodes	36	35
Area	1.680mm^2	1.680mm^2

Table.2 shows the synthesis report of full adder in both the logics, and this table demonstrates that when 16bit full adder is implemented by using proposed logic even though the average power consumption has increased when compared to the CMOS logic but static power dissipation and dynamic power dissipations are reduced which indicates the reduced power dissipation. Area is almost the same in both the logics.

CONCLUSION

The resistive threshold logic concept is presented in an application to implement an adder. This logic because of its ability in supporting the large number of inputs, helps in reducing the design complexity. Although this proposed logic outperforms the CMOS logic implementations of large input gates in performance parameters like power (dissipation), area further developments on low power consumption are required. The resistive threshold logic can be extended to the organic circuits, carbon nanotube technologies. And alsodue to the ability of the proposed threshold logic in producing the logic gates with large number of inputs, this can be considered as a worth early step of advancement for achieving the kind of goals like mimicking brain like large variable boolean logic applications in VLSI where the design complexity and number of components required are the major areas of consideration.

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