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Firefly Optimization and Mixed Tree Based Clock Distribution Network for an Optimal Energy FFT Architecture

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Abstract
With the rapid development of digital applications, the utilization of sequential circuits is increases. Hence, the design of storage element such as Flip Flop (FF) used in sequential circuits requires an important attention. The application of clock signal by a Clock Distribution Network (CDN) to trigger the flip flop is the challenging issue. Several clocking strategies such as resonant, 3 D integration, clock buffers operates in high frequency and high capacitive environment consumes more amounts of power leads to reduction of throughput. A Fast Fourier Transform (FFT) models effectively increases the throughput. But, the numbers of components in FFT are more, which consumes more power and area. This paper proposes a firefly optimization and mixed tree based CDN (FF-MT) for reduction of area, components. Initially, an objective function to describe the connection information of each node participated in FFT architecture for firefly algorithm is formed. Then, the best fitness value related to pulsed latch placement is calculated. The FFs with best fitness value are arranged in a cluster. From the clustered results, the center of cluster is extracted for pulsed latches placement. Finally, the creation of balanced CDN by using coconut tree combined with H-tree to distribute the clock signal to logical components in FF. The proposed FF-MT is tested with various circuits from ISCAS89 benchmark suite. The proposed optimal arrangement of FFs and tree based clock distribution assures the reduction of number of buffers, area consumption and energy consumption. The number of buffer reduction directly reduces the wire length and critical path delay effectively. The comparative analysis between the proposed firefly based CDN and traditional CDN models proves the effectiveness in terms of area, delay and energy.

Index Terms—Clock Distribution Network (CDN), Clustering, Fast Fourier Transform (FFT), Firefly, Flip Flop (FF), Tree based CDN.

Introduction

Memory elements play a vital role in sequential circuits for data storage. On the basis of triggering, the sequential circuits categorized into two types namely, edge triggered and level triggered. With the consideration of timing and convenience, edge triggered circuits which are the combination of edge triggered flip flops leads to Application Specific IntegratedCircuits (ASIC). In ASIC, the utilization of flip flop suffers overhead in terms of delay, area and clock delay. Hence, levelsensitive circuits are evolved which leads to Field Programmable Gate Array (FPGA) with various benefits that ASIC as fast time to market, post fabrication programmability. The power consumption depends upon the routing between the resources participated in the architecture. Verilog-to Routing (VTR)[1] and power aware routing algorithms [2]supports multiple clocks and optimization. The provision of clock signal acts as a reference signal in order to control of dataflow in digital systems. The distribution of clock signal to the sequential circuit is the challenging task in the digital circuit design.

Research works in clock distribution conveys that the various methods such as clock buffer insertion, 3 D integration and repeater utilization are used to design the low power clock network. Due to the high capacitive and high frequency operating nature of clock signal, consumption of power is more. To overcome this problem, resonant clock distribution models for microprocessors evolved. The high frequency of supply voltage affects the energy consumption and efficiency of microprocessors. Adaptive clock distribution offers the proper remedy to instant change in magnitude of supply voltage. The clock skew variation arises in CDN due to the non-uniform temperature profiles. The arrival of clock skew variations leads to functional faults in sequential circuits. Non-tree clock distribution networks exhibits high immunity, Process, Voltage and Temperature (PVT) variations, routing redundancies. Hence, tree based CDN extends the skew management in order to minimize the area and power dissipation. The design of low voltage/power systems helps to reduce the PVT variation termed as energy-optimal design using Fast Fourier Transform (FFT) architecture.

FFT is an alternative to general purpose processors with an aid of technology scaling. The FFT based design effectively reduces the optimum voltage and energy leads to high throughput. FFT integrates with the super pipelining technique enhances the voltage scalability and performance of the system. The New Distributed Arithmetic (NEDA) implements the FFT in FPGA architectures effectively. The employment of FFT to Very Large Scale Integration extends the applicability area as creation of Frequency Division Multiplexing (FDM) baseband transmitter, transfer of message, compressed sensing and signal restoration and bit reversal units. The increase in sensitivity of digital circuits to radiation effects introduces soft error in them. Hence, soft error estimation is an important issue in critical applications. Fault injection model based on FFT is used to estimate the

soft error by injecting Single Event Upset (SEU), Multiple Bit Upset (MBU). Pulsed latches used in this model increase the overhead and power consumption.

The timing verification and an optimization are important aspects in pulsed latches, since they operate based on clock signal. The Pulse Width allocation and Clock Skew scheduling (PWCS) uses PWCS_optimize algorithm to minimize the clock period. The use of local clock trees between latches and pulse generators and global clock trees between pulse generators and clock source requires synthesis. Latch clustering is used for synthesis process. Mesh optimization in clustering process focus on reduction of clock period. Moreover, meshwork addresses the tradeoff between resource requirements and tolerance variation. The use of more than one pulse width allows time borrowing which increases the clock period. Pulse Width Allocation (PWA) schemes combines retiming to achieve the minimum clock period. Traditional works addresses the clock synchronization is an important issue, since all devices are coordinated.

The reduction of area and power consumption is considered as a multi-objective optimization problem in research works. To solve the problem, the bio-inspired optimization algorithms with various features namely, simplicity, robustness and effective solution to complex problems highlighted. Firefly optimization algorithm is one of the methods to solve the complex issues in the design of pulsed latches for sequential circuits. Moreover, firefly algorithms use self-tuning which reduces the tough in parameter tuning of traditional optimization algorithms. The tree based CDN (symmetric and asymmetric) are evolved in order to reduce the wirelength. In this paper, the creation of optimal energy FFT architecture is discussed with the application of firefly optimization and mixed tree (H-tree and coconut tree) based CDN to reduce the wirelength, delay and power consumption.

The major contributions of this paper are discussed as follows:

1. The optimal placement of pulsed latches at the center of clusters by using fire fly optimization algorithm can effectively reduce number of FFs.
2. The mixed tree based structure can asymmetrically handle more number of leaf edges, than the existing tree structures.
3. The merging of FF with best fitness and clock distribution to best fitness FFs reduces the wire length and critical path delay effectively.

Section II presents a description about the previous research which is relevant to the Clock Distribution Networks and its difficulties. Section III involves the detailed description about the proposed firefly optimization based CDN. Section IV presents the performance analysis. This paper concludes in Section V.

Related Work

This section discusses the traditional works related to Clock Distribution Network (CDN) for Flip Flop (FF) design and how optimized energy models using pulsed latches created. Advances in Computer Aided Design (CAD) flow of Field Programmable Gate Array (FPGA) architecture supports multiple clocks timing analysis. An open source placement or routing is an important criterionin multiple clock environments. *Luu et al* presents the Verilog-to-Routing (VTR) which generates the list of post route circuit responsible for detailed simulation [1]. Routing strategies consumed more amount of total power due to the active parts in FPGA. The Power Gating (PG) is one of the techniques to reduce the power consumption. *Hoo et al* uses power gating aware routing algorithm [2] for leakage reduction in PG architecture.

Research work tends towards the design of low power clock based sequential circuits which was an important criteria in 3 D circuits. *Rahimian et al* discussed the design method for 3D resonant clock networks. The resonant operation of pre-bond tests in 3 D ICs reduced the power consumption [3]. The utilization of swing inverters at clock port of 3 D models was more. *Esmaeili et al* introduced the new FF for low swing LC resonant clocking scheme which reduced the swing inverters effectively [4]. The high frequency supply voltage V_{CC}droop in LC models affected the operational performance and energy efficiency when they used in design of microprocessors. The introduction of dynamically adaptive clock distribution models mitigated the effects of high frequency voltage. *Bowman et al*integrated the tunable length delay before clock distribution [5]. The prevention of degradation in timing margin by tunable length delay models allowed the sufficient response time for dynamic adaptation. The functional faults occur in CDN due to the effect of clock skew variations on timing margin. To overcome this problem, *Abdelhadi et al* presented an algorithm which combined the non-uniform meshes and Un Buffered Tree (UBT) [6]. They tested the proposed UBT with the circuits from ISCAS89 benchmark suite and compared with the various mesh optimization works [7-9]. The prioritization of algorithm on critical timing path reduced the area overhead and power dissipation. *Sathe et al*implemented dual mode feature in resonant based microprocessor models for the area and power consumption reduction [10]. *Sassone et al*analyzed the clock skew variations due to the non-uniform temperature profiles in tree based CDNs [11]. The low voltage operation of CDN induced the Process, Voltage and Temperature (PVT) variation problem.

The evolution of FFT architecture in CDN analyzed the PVT problem and provided the high throughput. For a complex FFT designs such as 1024-point value systems, the voltage scalability and performance was poor. *Jeon et al* utilized the super pipelining algorithm [12] reduced the leakage energy and averaging effects of random process. The introduction of reconfiguring models revealed that spectral efficiency was improved. *Whatmough et al* proposed the simplified approach for specific optimization of Spectral Efficient Frequency Division Multiplexing (SEFDM) systems [13]. The signal and image restoration and signal recovery by compressed sensing in Very Large Scale Integration (VLSI) required the sparse recovery models. *Maechler et al*implemented the Approximate Message Passing (AMP) algorithm for sparse signal recovery models [14]. From this analysis, design of FFT was an important issue in CDN. *Mankar et al*reported the architecture of FFT core with New Distributed Architecture (NEDA) algorithm [15]. Moreover, they mapped FFT design with Xilinx FPGA device. The delay time and area

complexities were more NEDA based architecture. *Chen et al* presented the bit reversal circuit by devised form of read and write scheduling algorithm[16]. The modification of an algorithm assured the optimized storage of memory banks. The digital circuits sensitive to radiation effects introduced the soft error. *Ebrahimi et al* utilized the fault injection technique to handle the soft error estimation [17]. The fault injection technique utilized the Single Event Upset (SEU) and Multiple Bit Set (MBS) fault models in FFs and memory units. Good initial clock problem was not addressed by the FFT based architectures.

Clock mesh networks usage was limited due to the high resource requirements. *Rajaram et al*presented the mesh framework achieved the trade-off between the resource requirements and tolerance variation [18]. Latches driven by clock pulses raised the pulsed latches offered the convenience in timing verification and optimization. The allocation of pulse width and skew scheduling are considered as an important problem in pulsed latches. *Lee et al* presented the Pulse Width Allocation (PWA) and Clock Skew scheduling algorithm (PWCS_optimize) [19]. The time borrowing in which more than one pulse used in timing model.*Paik et al* introduced the heuristic algorithm to find the minimum clock period which bring skew as zero [20]. The combination of PWA with retiming achieved the minimum clock period. The application of clock signal to pulsed latches in non-standard uniform cycle.*Teng et al*proposed the algorithms which replaced the flip flops with latches for high performance gains [21]. The power dissipation in modern circuit designs is more due to the maximum size of clock tree. *Lin et al* investigated the use of pulsed latch for power savings. They proposed migration approach for the construction of clock tree with FFs and pulsed latches [22]. Dynamic Voltage and Frequency Scaling (DVFS) was the important method to reduce the energy consumption in mesh based networks. *Harsha et al*synthesized capacitance driven clock mesh and skew variations were studied under DVFS technique [23]. The synchronization of devices was a necessary technique to mitigate the drifts.

The optimization techniques employed in CDN model assure the synchronization to determine the maximum admissible level of heterogeneity. *Carli et al* [24] proposed the distributed algorithm for clock synchronization which was based on consensus algorithm. But, solution to complex optimization problems using distributed algorithms complex.The bio-inspired optimization algorithms evolved and they considered as an alternative to distributed algorithm. *Arora et al*presented the fire fly optimization algorithms. They highlighted rules for the implementation of firefly [25]. The design of CDN involved multiple objectives and complex constraints. Scheduling problems considered as an immediate attention, since they required the generalization of parallel machines in some stages known as NP-hard. *Marichelvam et al* extended the firefly algorithm into discrete firefly algorithm for scheduling the hybrid flowshop. Makespan and mean flow time are two objectives of discrete firefly optimization algorithm [26]. The distribution of clock signal to pulsed latches present in FFs based on discussed in the related works. *Pavlidis et al* employed H tree based CDN for 3 D test circuits. The use of tree based CDN assured the resources availability and number of bonded plane[27]. *Chattopadhyay et al* extended the H-tree architecture in the design of dual reference based serial clock networks [28]. The problems addressed in the traditional works are area storage, more power consumption in the design of CDN. In this paper, an optimal energy model of CDN using firefly optimization algorithm is proposed in order to reduce the wire length, delay and power dissipation.

Firefly Optimization Based Clock Distribution Network

The main idea proposed in this paper is to designoptimal Clock Distribution Network (CDN) for application of asymmetric clock signal to Flip Flops (FFs) organized in Fast Fourier Transform (FFT) architecture. The FFs with best fitness value from firefly are arranged and merged by using clustering process. Coconut tree based clock distribution network is designed in order to carry maximum number of FFs since it handles more number of leaf edges. The block diagram of proposed method is shown in Fig. 1. Initially, the novel objective model corresponds to logical components involved in FFs is formed. An objective function includes the connection information between the logical components and the location. Then, firefly optimization algorithm extracts the best fitness value for each component. Based on the result from firefly optimization, the FFs are grouped in the clusters. For each node (logical components) in the clusters, the pulsed latch is placed to boost up the clock signal and manage the load. The clock distribution is done by using coconut tree arrangement of nodes which reduces the number of buffers and latches in FFT architecture.

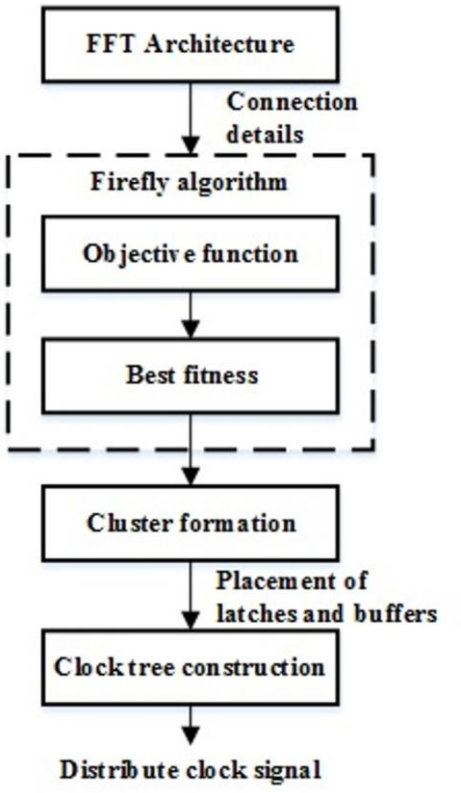

Fig. 1 Flow diagram of proposed method

The operational stages for implementation of proposed method as follows:

- FFT Architecture
- Firefly optimization algorithm
- Clustering
- Clock tree construction

A. FFT architecture

Very Large Scale Integration (VLSI) architecture realizes real time implementation of Fast Fourier Transform (FFT) which supports various data rates and power dissipation requirements. The FFT architecture comprises four radix-4 Processing Element (PE) used to perform the butterfly computations. The PE consists of four modules namely, RAM, address generators, butterfly and twiddle generators (*W)* as shown in fig. 2

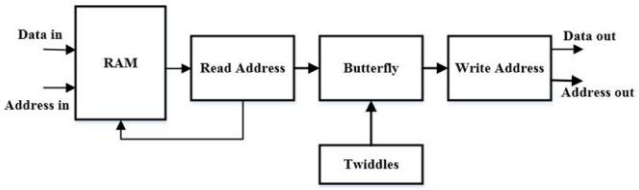

Fig. 2 FFT PE internal units.

i, RAM

The input data required to PE is stored in RAM. Two memory banks are organized internally in RAM. The first bank considers as working bank and the second bank used to store the incoming data.

ii, Address generators

There are two types of address generators namely, read address and write address generators. Read address generator supplies the addresses RAM block for internal processing. Write address generator supplies the addresses for exit data from PE.

iii, Twiddle generators (W)

A simple N-counter architecture refers twiddle generators which fetches the twiddle factors in each data cycle. Max(N) roots of unity decides the maximum size of an architecture. The twiddle factor is defined as

$$W_N = e^{-\frac{j2\pi}{N}} \quad (1)$$

Where, 'N' is the number of samples. The exponential term of the twiddle factor is resolved by the Euler's identity. The twiddle factor exhibits periodicity property and symmetry property.

This is given as

$$W_N^{k+N} = W_N^k \quad (2)$$

$$W_N^{k+\frac{N}{2}} = -W_N^k \quad (3)$$

iv, Butterfly

It performs N-point butterfly computation in following ways

- Read N-point data from RAM sequentially
- Inputs are given to radix-4 PE
- Fetch of twiddle factors from twiddle generator
- Accumulator performs add-subtract of four data parallel manner.

The proposed Register Transfer Level (RTL) based FFT architecture consists of multiplier and two adders by using resistors and transistors as shown in fig. 3.

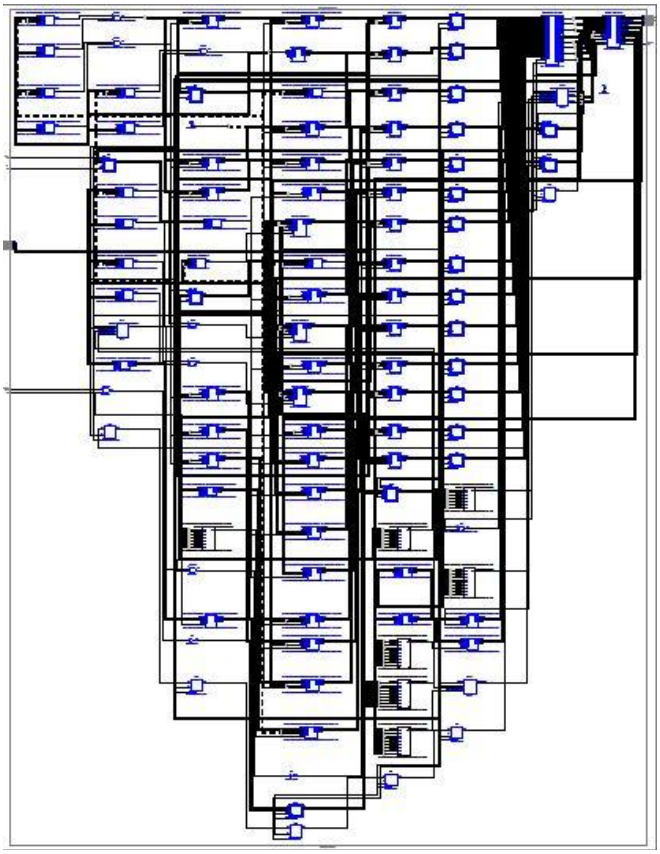

Fig. 3 Proposed RTL based FFT architecture

The multiplier performs complex multiplication of data input and twiddle factor. The first adder sum up the complex product values and the second adder produces the addition and subtraction of butterfly results. The architecture computes FFT computation on the basis of decimation in frequency algorithm. The pipelined architecture of radix-4 PE accepts the data input and the computational results from each PE are transferred to other PE by using broadcast bus. The bus utilization in FFT architecture in two ways.First, bypass the unused data in the exit of each PE. Second, output from each PE is transferred to next radix-4 PE. The result from the final PE is stored in RAM. The power consumption is more due to frame size and parallelism. The unused PEs for small frame size and low degree of parallelism increases the power consumption. Moreover, the clock distribution to the components occupies the maximum area, which also

consumes more energy. To overcome these problems the connection information between the logical components is to be optimized.

B. Firefly optimization algorithm.

The optimization of connection information between the Flip Flops (FFs) determines the best fitness corresponding to the distance. The nature inspired meta-heuristic algorithm called firefly algorithm used for optimization in this paper. The rules for firefly algorithm implementation defined as follows:

- Fireflies holds the connection information are considered as unisex thereby attraction occur irrespective of sex.
- Attractiveness and brightness are directly proportional to each other. Hence, both are decreases as distance decreases.
- Landscape of objective function determines the brightness of a firefly. Brightness proportional to objective functions for maximization problem whereas it is proportional to reciprocal of objective function for minimization problems.

The features such as attractiveness distance and movement decides the firefly optimization flow explained as follows:

i, Attractiveness

The attractiveness (β) between the fireflies depends upon light intensity (I)relates light absorption coefficient(γ), distance (d) and the initial intensity (I_0) as

$$I = I_0 e^{-\gamma d^2} \quad (4)$$

For attractiveness (β) equation (4) modified as

$$\beta = \beta_0 e^{-\gamma d^2} \quad (5)$$

1. Distance

The distance between two fireflies $f_1$and f_2 for connection information $C_{f_1}$and C_{f_2} is defined as

$$d = \left\| C_{f_1} - C_{f_2} \right\| = \sqrt{\sum_{n=1}^{N} \left(C_{f_1,o} - C_{f_2,o} \right)} \quad (6)$$

ii, Movement

The movement of firefly f_1 that is attracted to another firefly f_2 on the basis of randomization parameter α for random number $(rand)$ distributed in the interval [0, 1] defined as,

$$C_{f_1} = C_{f_1} + \beta_0 e^{-\gamma d^2} \left(C_{f_1} - C_{f_2} \right) + \alpha (rand - 0.5) \quad (7)$$

The firefly optimization algorithm on the basis of above features as follows:

Firefly optimization algorithm

Inputs: Connection information $\{C_1, C_2 \dots, C_N\}$
Output: Best fitness

1. Objective function $f(C) = \{C_1, C_2 \dots, C_N\}$
2. Initialize a population of fireflies for $C_i (i = 1, 2 \dots, N)$
3. Determine light intensity $I_i$at $C_i$by using $f(C)$according to equation (4).
4. Define light absorption co-efficient γ
5. While (t<MaxGeneration)
6. For $i = 1{:}N$
7. For $j = 1{:}i$
8. If $I_i > I_j$
9. Move firefly i towards j in all dimensions N according to equation (7)
10. Else
11. Move firefly randomly
12. Attractiveness changes with respect to distance d
13. Determine new solutions and revise light intensity
14. End for j
15. End for i
16. Rank fireflies and find the best
17. Endwhile

Initially, the connection information between the logical components are given as input to firefly algorithm. The populations of fireflies are created for each information. The light intensity is calculated for each firefly. Then, check whether the intensity of i^{th}firefly is greater than j^{th}firefly. The corresponding firefly moved towards$j$, if the condition is satisfied. Otherwise, move the firefly in random fashion. Now, the attractiveness changed and the new light intensity is estimated. Finally, rank all the moved fireflies for N dimension and estimate the best fitness correspond to minimum distance between the logical components. These fitness values are arranged in a group by clustering algorithm.

C. Clustering

The clustering algorithm used to merge the nearest Flip Flops (FFs) having best fitness value. Due to merging, the area of device occupation reduces leads to reduction in wire length and critical path delay. The clustering algorithm for merging as shown below:

Clustering Algorithm

Input:FF's location F_P, fitness values $(f_1, f_2, \dots, f_N)$
Output: Cluster result, 'C_o'
Step 1: Coordinated of FFs, $F_{ij} = \{F_{1,1}, F_{1,2}, \dots, F_{m,n}\}$
Step 2: Extract fitness value for each FF location corresponds and placed in distance tableD_{ij}.
Step 3:Find minimum distance fromD_{ij} table
Step 4: Merge FFs and Update table
Step5:Update coordinates
Step 6: $C_o = F_{ijc}$ //Update Cluster.
Step 7: Repeat Step 2 to 6 until empty of individual FF nodes.

The FFs location and corresponding fitness values from firefly optimization are given as the input to the clustering algorithm. The FFs are coordinated according to the location. The fitness for each location is extracted and placed in distance table denoted as D_{ij}. From distance table, minimum value is calculated. The FF corresponding to minimum distance is merged and the distance table is updated with new location. The coordinates corresponds to distance table are updated. The distance estimation and revised cluster formation are performed until the individual nodes are empty. The updated clusters of coordinated flip flops defined by

$$F_{ijc} = \left\{\left\{\{F_{1,1}, F_{1,2}\}, \ldots, \{F_{m-1,n-1}, F_{m,n}\}\right\}\right\} \quad (8)$$

The FF merging is shown in fig. 4.

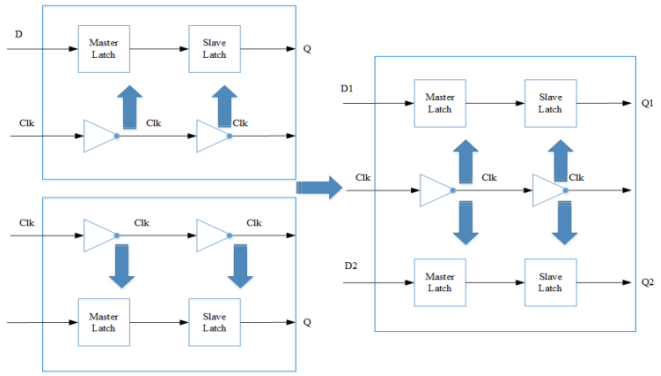

Fig. 4 FF merging

Hence, firefly optimization based cluster formation reduces the number of devices which reduces the area overhead. But, the critical path delay is an important concern since they are pulsed one. The pulsed latches placed at the center of cluster after merging is over. The pulsed latches are triggered by the clock sources, which guided by the tree architecture.

D. Clock Tree construction

The triggering of Flip Flops (FFs) depends upon the clock signal provided by Clock Distribution Network (CDN). Tree based CDN models effectively reduces the wire length and critical path delay due to the multiple leaf handling features. In this paper, the mixed tree based CDN is discussed. The traditional H tree is integrated with the coconut tree ensures that maximum number of FFs handling capability. The formation of H-tree is shown in fig. 5.

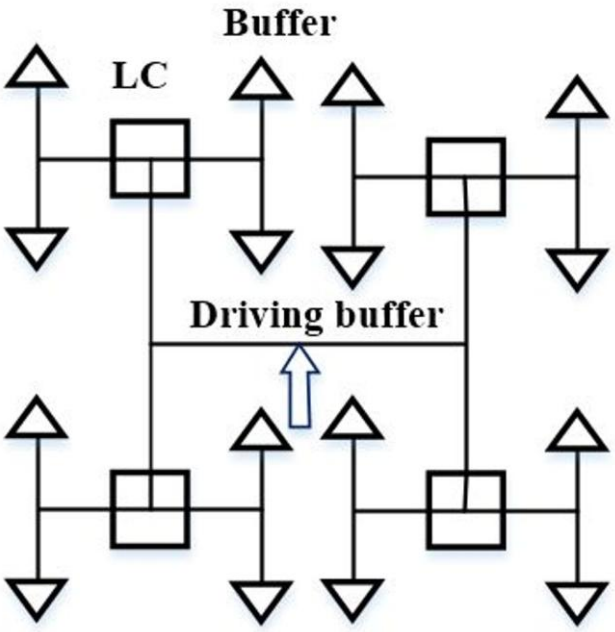

Fig. 5 H-tree architecture.

The H-tree sector consists of set of spiral inductors and capacitors (LC), and driving buffers for clock sectors. The energy alternation due to the resonance nature of inductor and capacitor rather that dissipation reduces the power consumption. The network is divided into sectors of 16 leaves. The formulation of H tree depends upon various parameters as width w_i, length l_i and thickness t_i of each sector (i), clock frequency (f_o) and capacitive load C_l as

$$H = f(w_i, l_i, t_i, f_o, C_l) \forall i \quad (9)$$

The H tree is used to reduce the power consumption effectively. But the number of nodes handling is less. To increase the number of nodes handling, we integrate this traditional H-tree into coconut tree. A coconut tree based CDN is developed to provide the asymmetric clock signal to all components in FFT architecture. H sector model arranged as a leaf nodes in coconut tree. The coconut tree comprises the 20 leaf nodes. For each leaf node, H-sector of 16 leaves is placed. Thereby, more number of logical components are handled. The architecture of coconut tree is shown in fig. 6.

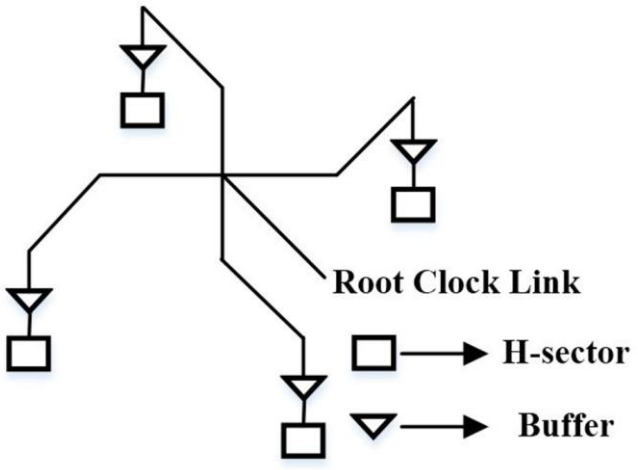

Fig. 6 Coconut tree

The proposed mixed tree (H + Coconut tree) based CDN provides the asymmetric clock signals to pulsed latches and handles maximum number of latches. Thus, the optimal energy based CDN using firefly optimization based clustering and mixed tree formed in order to reduce the wire length, critical path delay and power consumption.

Performance Analysis

In this section, the performance of the proposed method is evaluatedthe parameters of wirelength, critical path delay, and area and power consumption. The circuits from sequential ISCAS89 benchmark suite are considered for analysis of proposed method. The standard cell library called Virage Logic SiWare used for ISCAS 89 design. The proposed firefly optimization and mixed tree (FF-MT) based Clock Distribution Network (CDN) is compared with the traditional Hybrid Mesh/Tree construction (HMT) for non-overlapping polygons [6] in terms of metal consumption. The comparison between proposed FF-MT and the traditional mesh work optimization methodologies [7], [8] and [9] in terms of power consumption and wire length discussed. The analysis of wirelength and power consumption on the basis of experimental parameter termed as relative tolerance measure ξ relates the maximum skew variation ratio $\delta_{max}^{i,j}$ for allowed skew variations $skew_{allowed}^{i,j}$ as

$$\xi = \frac{\delta_{max}^{i,j}}{skew_{allowed}^{i,j}} \quad (10)$$

The skew variation refers the difference in arrival time between two adjacent elements.

$$skew_{max}^{i,j} = \max_{i,j}\left(\left|F_i - F_j\right|\right) \quad (11)$$

The allowed skew variation is bounded by following terms

$$skew_{allowed}^{i,j} = T_{clk} - T_{setup} - T_{PD}^{i,j} \quad (12)$$

The path delay depends upon the clock to output delay of register (T_{CQ}), total delay of logic path between the register(T_{LOGIC}), total delay of interconnect (T_{INT})and the setup time (T_{SETUP}) described as follows

$$T_{PD} = T_{CQ} + T_{LOGIC} + T_{INT} + T_{SETUP} \quad (13)$$

Due to the optimal arrangement using firefly optimization algorithm, the distance between the components is minimum which directly minimizes the delay. The parameters such as clock sinks, logic paths, logic gates and skew regions for ISCAS89 sequential benchmark suite analyzed for proposed FF-MT and listed in table 1.

TABLE 1.Comparative Analysis of HMT and FFMT

\Test Case	s9234		s5378		s13207		s15850		s38584		s35932	
	HMT	FFMT	HMT	FFMT	HMT	FFMT	HMT	FFMT	HMT	FFMT	HMT	FFMT
Clock Sinks	135	127	165	158	500	482	566	552	1426	1385	1728	1541
Logic Gates	5.6K	4.8K	2.8K	2.1K	8K	7.2K	9.8K	8.8K	19.2K	18.3K	16K	14.9K
Logic Paths	3.1K	2.7K	5.4K	4.5K	12.4K	11.1K	18.6K	17.7K	54.5K	52.3K	43.3K	40.2K
Skew Regions	3	3	3	3	4	4	6	5	8	7	6	5

From the table 1, the FF-MT on the ISCAS89 bench mark suite provides 31 % average reduction in metal consumption due to the optimal placement of CDN and FFs.

The design summary for proposed FF-MT algorithm is shown in table 2.

TABLE 2.Design Summary

Design Summary for Proposed FFT architecture			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	273	93120	0%
Number of Slice LUTs	471	46560	1%
Number of fully used LUT-FF pairs	262	482	54%
Number of bonded IOBs	69	240	28%
Number of BUFG/BUFGCTRLs	1	32	3%

Table 2 shows the logic utilization analysis. The utilization rate of the number of slice registers, slice LUTs, fully-used LUT-FF pairs, bonded Input Output Blocks (IOBs), block RAM/First-In/First-Out (FIFO), Global Clock Buffers (BUFG/BUFGCTRL) and Digital Signal Processors (DSP) is illustrated.

The circuit characteristics and the user defined parameter *(T)*decide the large entity skew region. The decrease in threshold value makes the skew regions as fine. The proposed FF-MT based CDN evaluates the relationship between the metal resources, power consumption and relative skew

tolerance parameterξ. For a typical value ($\xi = 1$), the proposed FF-MT effectively reduces the power consumption and wire length compared to traditional hybrid mesh/tree algorithm. The analysis of wire length for FF-MT for typical value ($\xi = 1$) is listed in table 3. The wire length is reduced for each bench mark suite, since the firefly optimization provided the best fitness related to connection information. The distance estimation and clustering of best fitness components effectively reduced the wirelength as shown in fig. 7.

TABLE 3.Wire Length Comparative Analysis

Wire length (μm) at ξ = 1. 0	s9234	s5378	s13207	s15850	s38584	s35932
Mesh[8]	33, 610	31, 009	82, 884	84, 055	256, 567	349, 432
Mesh[9]	27, 177	24, 911	109, 538	100, 778	262, 528	321, 293
Mesh[7]	13, 376	20, 839	51, 443	45, 628	166, 274	239, 342
HMT [6]	11, 713	16, 683	47, 623	46, 139	151, 995	218, 274
FFMT	10, 596	12, 598	38, 902	36, 925	136, 848	193, 229

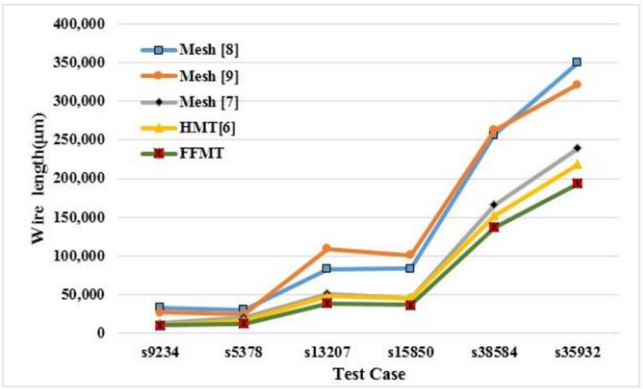

Fig. 7 Wirelength analysis

The analysis of power consumption for FF-MT for typical value ($\xi = 1$) is listed in table 4. The power consumption is reduced for each bench mark suite, since the mixed tree based CDN provided the clock signal. The optimal placement and clock distribution contained an effective skew tolerance managing capability which reduces the power consumption in fig. 8.

TABLE 4.Power Consumption Comparative Analysis

Power (mw) at ξ = 1. 0	s9234	s5378	s13207	s15850	s38584	s35932
Mesh[8]	8	7	21	22	65	74
Mesh[9]	7	7	24	24	61	74
Mesh[7]	5	5	13	14	41	44
HMT [6]	5	5	12	13	37	40
FFMT	5	4	10	11	35	37

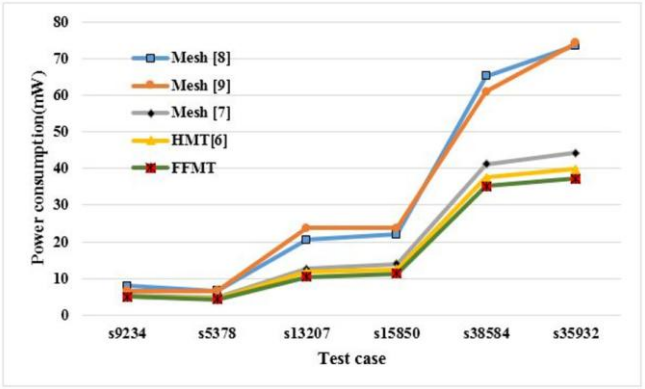

Fig. 8 Power consumption analysis

Conclusion

This paperaddressed challenging issue such that the application of clock signals by a Clock Distribution Network (CDN) to trigger the flip flop. The operation of clocking strategies in high frequency and high capacitive environment consumed more amounts of power leads to reduction of throughput. More number of components in FFT also consumed more power and area. This paper proposed a firefly optimization based CDN for reduction of area, components. Initially, an objective function comprised of the connection information of each node participated in FFT architecture for firefly algorithm is formed. Then, the best fitness value related to pulsed latch placement is estimated. The clusters of FFs with best fitness value are formed. From the clustered results, the center of cluster is extracted for pulsed latches placement. Finally, balanced CDN by using tree is created. The proposed optimal arrangement of FFs and tree based clock distribution assured the reduction of number of buffers, area consumption and energy consumption. The number of buffer reduction directly reduced the wire length and critical path delay effectively. The comparative analysis between the proposed fireflies based CDN and traditional CDN models proved the effectiveness in terms of area, delay and energy.

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