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Analysis of APC and Code of Practice

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Abstract
Aggressive Packet Combining (APC) uses majority logic for correcting errors in the receiver side that encourages, sending multiple copies of same packet to the network by the transmitter. This gives negative effects on nodal delay. Our propose scheme do not send multiple copies for the same packet and uses Forward Error Correction (FEC) to detect erroneous packet and correct the same. The proposed scheme has lesser nodal delay especially processing delay, queuing delay and has lesser packet error rate compared to APC. More over the proposed scheme can handle some levels of burst error.

Keywords—APC, Aggressive Packet Combining, Queuing Delay, Processing Delay, Little's theorem, Latency, Packet Error.

I. INTRODUCTION

Wireless has high bit error rate [1-2] in the range of 10^{-2} to 10^{-4}. In order to get correct packet, transmitter has to transmit multiple copies of the same packet till receiver get correct packet. These consume communication bandwidth as well as import delay in the nodes from source to destination. Bandwidth is a scare resource as many nodes share the limited spectrum and many packets will be discarded as a result of overcrowded of multiple retransmission of the packet from transmitter. It is desirable to reduce number of retransmitted packets so as to utilize the bandwidth and reduce delay in the network by keeping reliability of the packets in wireless network.

In order to achieve reliability in the network many uses BEC (backward error control) for wired network and FEC (forward error control) for wireless network [3-5]. Many error control protocol discard the erroneous packet although it may contain some part of correct bits and some erroneous bit.

Many Aggressive Packet Combining scheme (APC) [6-8] have been studied in the literature for reliable transmission in the network but most of this scheme transmit multiple copies of the same packet, more over they do not address burst error.

We propose to use FEC for reliable transmission of the packet in wireless network. Out scheme avoid sending of multiple copies for same packet and also address some level of burst error. We study the properties of this scheme and evaluate using computer simulator. Simulation result shows that our proposed scheme performs better than other existing scheme.

II. MOTIVATION AND BACKGROUND

Aggressive packet combining scheme [8] is modification of majority logic scheme [6]. In which three copies of the packets are sent and bit by bit majority logic is performed. The working of majority logic is shown in Fig 1.

In MPC(Modified Packet Combining Scheme) when receiver sends NACK then the sender sends i copies of the requested packet. Then XORing all the copies that was received will locate error position in the packet and errors are corrected in the packet [9].

In PRPC (Packet Reversed Packet Combining scheme) [10], when receiver request for retransmission, sender sends the reverse of the previous packet. In receiver side the erroneous packet and reversed packet are XORed. Then by application of the brute force method the packet can be corrected.

In Bit shifting in APC[11], sender sends the second copy by shifting the bit andfirst and third as normal packet. In the receiver side the second bit is shifted in reversed way as done by the sender then applying majority logic will give the correct packet.

In all the proposed APC the sender send multiple copies of the required packet and in receiver side multiple copies received are combined and corrected packet are generated.

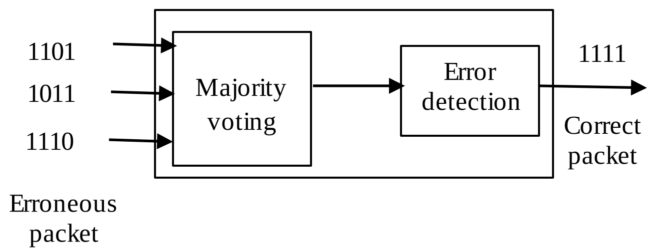

Fig1. Majority packet combining

III. PROPOSED SCHEME

Proposed scheme is for FEC in wireless transmission. In APC multiple copies of the same packet are transmitted by the sender and in receiver side forward error correction is done to generate correct packet. In the proposed scheme required packet is sent only once and receiver on receiving those packets applies code of practice # 3 for FEC. Code of Practice is released under the intellectual property terms of the pro-MPEG Forum WAN Group [12].FEC structure is shown in Fig.2. It uses XORing for generation of FEC.

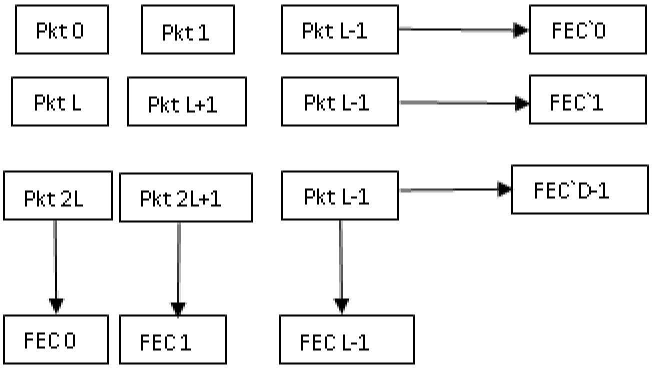

Fig. 2: Duel FEC mode structure

It uses L columns and D rows. The row FEC stream can cope with burst losses up to 'L' in length.

A. *Algorithm*

Start:

Transmitter:

1. Make sets of packets such that number of packets (N) mod 4 is zero where N > 16.
2. Arrange the packets in 4 X (N/4) matrix.
3. XOR all the rows and term it as FEC'.
4. XOR all the columns and term it as FEC.
5. Send all the packets along with FEC' and FEC.

Receiver:

6. Collect all packets that have been received and arrange in 4 X (N/4) matrix.
7. XOR all the rows and term it as FEC1'.
8. XOR all the columns and term it as FEC1.

Error Detection:

a. If (FEC1'==FEC' && FEC1==FEC)
then packet has been received without error.

b. Else, find FEC1'(i) != FEC' (i) && find FEC1(j) != FEC (j).
c. Matrix (i,j) is erroneous
9. If (FEC1'==FEC' && FEC1!=FEC)
Then FEC has been erroneous, ignore FEC and consider FEC1 as FEC.

Error Correction:

a. To correct the erroneous packet contain in matrix(i, j) , XOR FEC(j) with correct packet of column (j). The generated answer gives the correct packet.
End:

Case 1: (FEC != FEC1 && FEC' !=FEC1')
Consider N= 16. In transmitter, arrange packets as shown in Fig 3and find the FEC and FEC' by XORing the packets.

					FEC'
	1110	1111	1110	1101	**0010**
	1110	1011	1010	1001	**0110**
	1010	0101	1110	0101	**0100**
	0100	0001	1010	0101	**1010**
FEC	**1110**	**0000**	**0000**	**0100**	

Fig 3: Generation of FEC and FEC'

Let us consider that the first packet was corrupted during transmission as shown in Fig 4. In receiver side packets are arranged as below and find the FEC1 and FEC1'.

					FEC1'
	1010	1111	1110	1101	**0110**
	1110	1011	1010	1001	**0110**
	1010	0101	1110	0101	**0100**
	0100	0001	1010	0101	**1010**
FEC1	**1010**	**0000**	**0000**	**0100**	

Fig 4: First packet is erroneous

Comparing FEC with FEC1 and FEC' with FEC1' it is found that FEC1(0) and FEC1' (0) does not match. Thus the packet in the matrix (0, 0) is erroneous.
To correct the erroneous packet XOR FEC with connect packets in column (0).
$1110 \oplus 0100 \oplus 1010 \oplus 1110 = 1110$

The generated answer is the corrected packet.

Case 2: (FEC != FEC1 && FEC'==FEC1')
If FEC !=FEC1 but FEC' ==FEC1 or vice versa, this shows that FEC is erroneous and packets are received in correct form. So discard the FEC.

IV. SIMULATION AND RESULT

We compare the queuing delay and processing delay of the nodes with APC and proposed scheme.

A. *Processing delay*

Processing delay is the time to process the packets header. Firstly nodes scan content of the header to check for bit-level errors in the packets and then search the table to determine the packet's next destination. Time taken to read the header depends on the hardware composition of the node depending upon the technology used it may vary but it will be constant value for particular node. Let α be the constant value to read the header. For APC,

$$PD = \alpha * 3 * no\_packets \qquad \text{I}$$

Since in the proposed scheme the extra overhead is FEC and FEC' thus,

$$PD = \alpha * no\_packets + rows + columns \qquad \text{II}$$

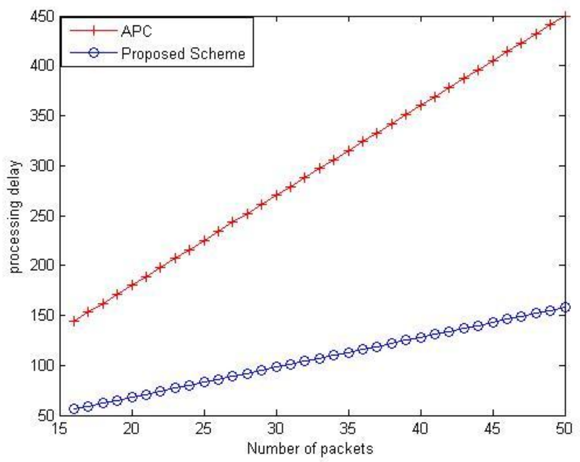

Fig. 5 : Processing delay of APC and proposed scheme

Run of equation I and II is shown in Fig. 5 it clearly shows that the proposed scheme has less processing delay. It shows the nodal processing delay.

B. ***Queuing Delay***

Queuing delay is the time the packet is in a queue before actual transmission starts. The time in the queue depends on the number of packets ahead and the rate they are removed from the queue.

$$T = \frac{N}{\lambda}$$

Where T is the average waiting time in the queue, N represent number of packets in the queue and λ represent rate at which packets are removed from the queue.
For APC the queuing delay

$$T = \frac{3N}{\lambda} \quad \text{III}$$

Queuing delay for proposed scheme is

$$T = \frac{N + row + column}{\lambda} \quad \text{IV}$$

Run of equation III and IV is shown in Fig. 6. It shows that proposed scheme has less queuing delay than APC. The value N is assumed as 16 and above, the rows are 4 and columns are also considered as 4.

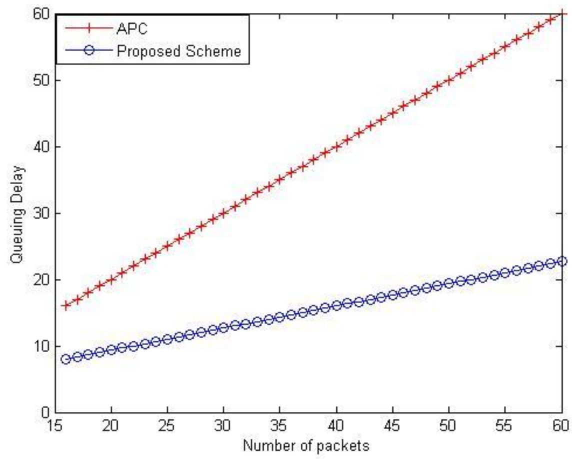

Fig. 6 : Queueing delay of APC and proposed scheme

C. Packet Error Rate

In APC single packet is sent three times so the probability of packet error rate (PER) is high. PER for APC is given by:

$$PER = \left(1 - (1-\alpha)^n\right)^3 \quad \text{V}$$

Where α bit error rate and n is the number of bits sent
Packet error rate of the proposed scheme is

$$PER = \left(1 - (1-\alpha)^{n+rows+columns}\right) \quad \text{VI}$$

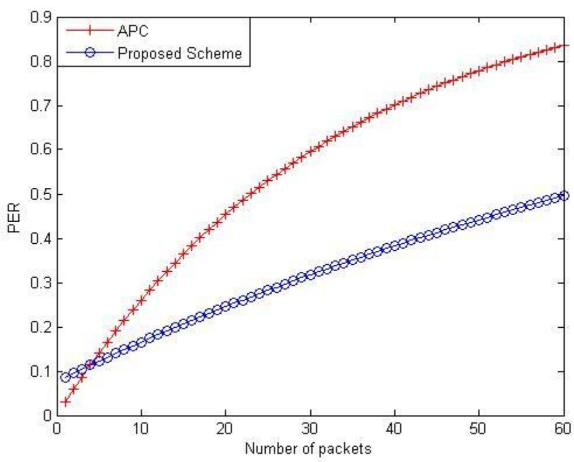

Fig. 7: comparison of PER of the APC and proposed scheme

Fig. 7 shows the comparison of APC and proposed scheme, value for α is taken as 0.01. The Fig. 7 shows that the packet error rate is higher in APC as compared to proposed scheme.

V. CONCLUSION

APC uses erroneous packets to generate correct packet. For that transmitter transmit same packet multiple times. Thus it increases the queuing delay and processing delay of the nodes also packet error rate is high as number of bits that are transmitted is high. We proposed a scheme that uses FEC for error detection and correction. Simulation result shows there is significant decrease in queuing delay, processing delay and bit error rate as compared to APC in proposed scheme as it uses less number of redundant bits.

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