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A Low Noise Chopper Stabilized CMOS Fully Differential OP-AMP with CMFB Amplifier for Biopotential signals Monitoring

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Abstract- Bio potential signals monitoring in biomedical field add more precise way of handling human/nonhuman signals. Operational Amplifier plays a key role in Analog circuits of which biomedical application is the key area. We have opted for a CMOS (Complementary Metal oxide Semiconductor) design with fully differential Operational Amplifier having CMFB (Common Mode Feedback) circuit to decrease the noise content present in Bio potential signals measured. Bio potential signals are low frequency, low amplitude range signals. Hence the noise present in the Operational Amplifier is flicker noise at low frequency it dominates other frequencies, hence effectively filtering out the flicker frequency components forms the crux in noise removal. The fully differential Operational Amplifier is drawn from single differential Operational Amplifier to get low noise levels. The beauty of our project lies in the modified architecture of Operational Amplifier. The circuit with fully differential Operational Amplifier and CMFB helps in scaling down of noise to 0.34nv/√Hz at corner frequency of 10 Hz with 1v of power supply which performed better than the Fully Differential Operational Amplifier [1]. The Modified design in this paper has been implemented in Cadence 90nm technology.

Index Terms- *flicker noise, CMFB, corner frequency.*

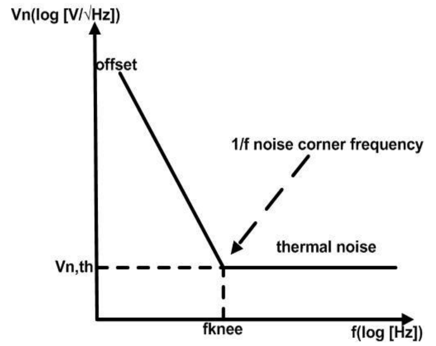
1. Introduction

Noise is the major tradeoff among the design of any amplifier circuit along with Power, Area and other essential parameters. It resembles the signal and gets amplified when original signal is amplified by the OP-AMP (Operational Amplifier).we cannot differentiate between the original signal and the noise signal which is amplified at low frequency of operation. Generally noise is calculated by the average power spectrum signal of the device standard noise power spectrum of CMOS Operational Amplifier as shown in Fig.1 [2].in the figure where 1/f noise converges, the thermal noise is termed as 1/f noise Corner frequency f_{knee}. In higher frequencies, noise is independent of frequency and this is termed as thermal noise floor. Below the corner frequency is the flicker noise, the power of which increases linearly as frequency starts decreasing. Noise is the random phenomenon present in the analog circuitry which will affect the throughput of the device. Basically many noises are present out of them two noises are most predominating like Thermal Noise, Flicker noise (1/f noise) [3].Thermal noise is due to the random motion of electrons in a semiconductor device. Noise in the resistor was indicated by equation 1 of which K is Boltzmann’s constant, R is resistor T is at absolute temperature, and Δf is the bandwidth calculated where the noise is measured.

$$Vt = \sqrt{4KTR\Delta f} \tag{1}$$

Flicker noise is due to the breakage of dangling bonds are formed by the interfaces of gate oxide and silicon substrate at low frequency. Flicker noise is calculated like thermal noise and for this we require modeling of the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) devices by

$$\overline{V_n^2} = \frac{k}{c_{ox}W L}.\frac{1}{f} \tag{2}$$



Noise Of standard CMOS operational Amplifier

These types of signals create trouble when input is low frequency, low bandwidth and low Amplitude such as Bio potential signals. In this Biopotential signals like Electroencephalogram (EEG), Electrocardiogram (ECG) and Electromyogram (EMG) etc which are of systems represented to calculate human/non human signals related to brain, heart and nerves etc,which are listed in the table I [4].

Table I. Properties of several Biopotential signals

Devices	Measurement Range(Volts)	Gain(db)	Frequency range(Hz)
EEG	25-300µ	50-72	DC-150
ERG	5-900 µ	41-86	DC-50
EGG	10-1000 µ	40-80	DC-1
ECG	0.5-4m	28-46	0.01-250
EMG	0.1-5m	27-60	DC-500

Human /nonhuman signals are different and are in micro to milli volt ranges so in order to identify the original signals from the duplicate signals there are different techniques [5] that are employed namely Auto zeroing (AZ), Correlated double sampling (CDS) and Chopper stabilization (CHS) each and every one of them have their own advantages and disadvantages among them the chopper stabilized technique is most suitable one. First two techniques indicated are of sampling type while the last technique employs modulation. Modulation transposes low frequency signals of noisy signals to the higher frequency, the demodulator at end will demodulate the signal along with the low pass filter we can recover the original signal from the noisy signal present at very low frequency .The following sections are classified accordingly as in section II will explain the difference from present architecture and the modified architecture, section III shows the Implementation and Results. Section IV, V will be conclusion and future work.

2. Architecture

In Fig.2, the total architecture of our noise limiting Amplifier which consists of an Operational amplifier.OP-AMP is the main heart in amplifying the signal from the chopper Amplifier, and the output of the Opamp is directed towards another chopper circuit which is acts as a demodulator that demodulates the signal. The other block is the integrator functioning as a low pass filter for noise removal at high frequencies, thus effectively shielding the rest of the circuit from the noise, As we make the noise to shift to higher frequencies through chopping and passing through low pass filter we remove the high frequency and noise components.

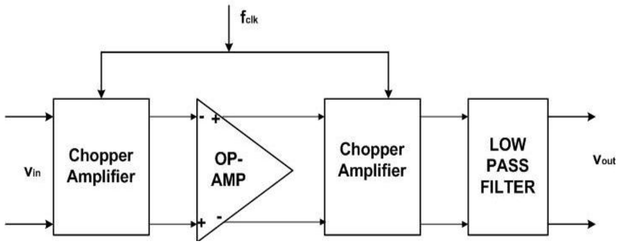


Fig.2. Block diagram Flicker noise is the specific noise present in the CMOS technology and is exhibited at low frequency due to the imperfection in the silicon substrate and gate oxide in the technology manufacturing.

This type of noise is reduced by the Chopper stabilized technique than the other sampling techniques. Flicker noise is less in PMOS(P-Channel Metal Oxide Semiconductor) transistor than the NMOS (N-Channel Metal Oxide Semiconductor) transistor due to the mobility of electrons is more than mobility of holes by order of 2-3.in our design of OPAMP we used PMOS as the input to signal at both stages. We designed a fully differential Opamp with high gain, high swing voltage and which can handle good CMMR.

A. Operational Amplifier Design

The operational amplifier design is key to the entire Analog design circuit as it is the key for building the amplifier and integrator hence selection of the operational amplifier has to be done quite carefully. The key parameters for its design include high gain for smoother integration and a large bandwidth for effective transmission of the signal, the remaining parameters of op-amp that are essential are high input impedance, gain margin and low output impedance. A two stage CMOS op-amp design has been implemented in this paper with a fully differential pair and a current source placed above the single stage. It is essential that appropriate sizing of the transistors must be done as it impacts the performance of the operational amplifier. It impacts not only operating region but also the gain and the drain current values. As it is employed in the integrator design it is expected to have high gain for smoother integration with large bandwidth to pass better number of harmonics. Comparing both of the architectures with respective of present architecture and modified architecture shown in fig 3 & 4, by the two stage Opamp the single stage [6] is directed towards input to the PMOS device of second stage it contains miller capacitances for the single stage to second stage and also the addition of nulling resistor improves the stability of OPAMP . When it is operated in closed loop, nulling resistor value is chosen according to the inversely proportional to the transconductance ($1/g_{mp}$) [7]of the second stage PMOS transistor. Fully differential OPAMP has an advantage of having less voltage drop, less immunity to interface and also having less stray interface.

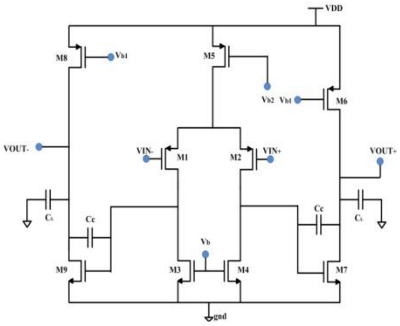


Fig.3. Previous Architecture of Fully Diff OPAMP

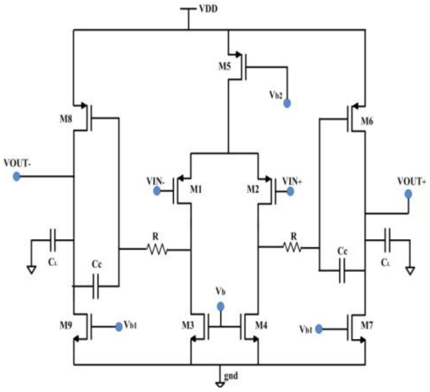


Fig.4. Modified Architecture of Fully Diff OPAMP

B. CMFB

Common Mode Feedback (CMFB) circuit exhibit large transconductance and it doesn't resistively load with the load of OP-AMP to avoid mirror poles, greater output swings, thus achieving a higher closed-loop speed. In order to get good CMMR in both differential, common mode signal we need CMFB technique. In this implementation we have many circuits that can provide feedback for our circuit. For this a design logic is to be considered which is if the voltage has to be directed to PMOS we need to apply common mode signal and the differential output of two stage Opamp to the NMOS transistors similarly vice versa for other case . CMFB helps in avoiding device level mismatch in chip level design in order to maintain proper region of operation of the two stages of Opamp [8]. In these circuits we are having resistor divided method, switched average method and Differential difference amplifier method among them one occupies large chip area due to large resistors present and also reduce the gain of open loop gain. Another has clock injection due to switch presence.

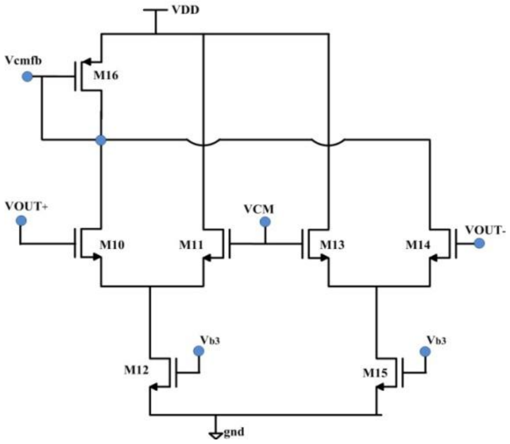


Fig.5. CMFB circuit

Recent papers have controlled through bulk terminal to avoid mismatches Differential difference amplifier [9] is therefore best suitable for this which has been implemented as shown in fig 5.we can easily calculate slew rate and settling time of this if we are operating in the proper region of operation.

C. Chopper Circuit

Chopper circuit in figure 6 shown will acts as both modulator and demodulator in our block design. Chopper stabilized technique fundamentally uses a pulse (carrier) to perform amplitude modulation on the input signal. Chopping technique requires pulse with period $T=1/f_{chop}$ where f_{chop} is the chopping frequency. In order to perform the analysis without any aliasing signal it is band limited to half of the chopper frequency [10]. Generally Amplitude modulation uses carrier transposing the signal higher frequency, where flicker noise is less in those frequencies and in the end we have a demodulator which will have the original signal. Mostly the signal is directed to the input of integrator where greater than half chopping frequency will be removed so mostly our signal is present only in lower frequencies.

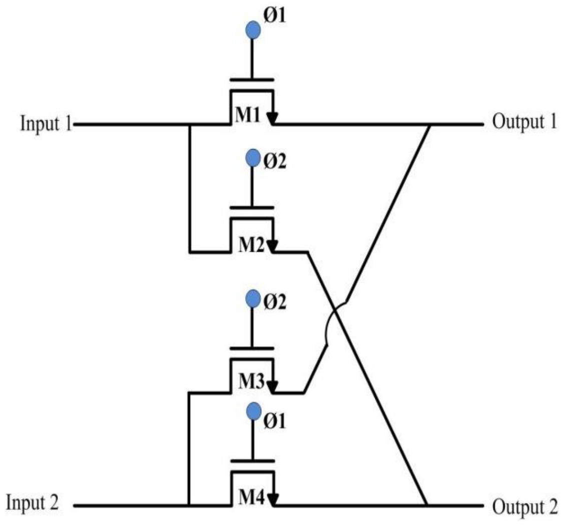


Fig.6. Chopper circuit

D. Low pass Filter

The operational amplifier selection has to be done to suit primarily the low pass filter (integrator). The change at the output voltage is a integration of the input voltage and where it is function of the resistance and the capacitance in the feedback path. The second input of the integrator is connected as the other terminal we used fully differential Opamp for our design. Integrator also is important for further designing of the as number of integrators decides the order of the modulator even though higher order modulators promise linear operation at lower frequencies. More number of integrators might result in instability, but we don't require higher order modulator.

3. Implementation & Results

Implementation of architecture is done by combining each and every component from two stages Opamp, chopper circuit and low pass filter. Opamp which we have designed for our method has been done by mingling of modified architecture with CMFB circuit. In the operation of transistor in saturation region ,which makes MOSFET to amplify the input signal we have considered simply common source amplifier and replicating it helps in building the two stage fully differential Opamp with CMFB circuit. In the first stage we have M_1-M_5 where M_5 is the current source present over the tail current source which provides the current from drain current of which it is equally divided among the two replicate half circuits. In the next stage we have the PMOS transistor as common source in the second stage.

Opamp to be operated in the closed loop we require stability of two stage Opamp. for this we consider the nulling resistance with miller capacitance which will be providing necessary gain and the Phase Margin for the Opamp which is obtained as more than 60 degrees and gain of 57db with unity gain bandwidth of 190Mhz, and f_{3db} of 267.502KHz.which is shown in fig 7.and the load capacitance of the Opamp must be high in order to drive the next device connected to it so we have load capacitance of 1pf.

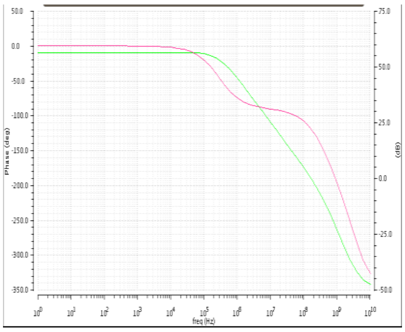


Fig.7. Ac gain of Opamp

When the signal is passed from the input to chopper modulator having two non overlapping phases of clock with 1KHz of pulse signal, if the pulse has low input then inversion is possible. When signal is high then no inversion takes place in this switch are indicated in fig 8 where transistors operated in linear region, cutoff region to be operated as switch. Input to the chopper modulator is low frequency and low amplitude signal, noise of the Opamp circuit is shown in fig 9 and in fig 10 shows log scale of the input referred noise of Opamp.

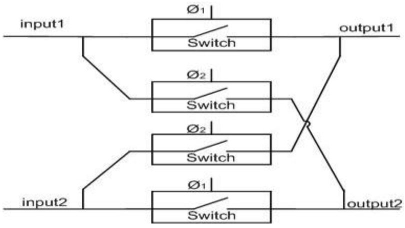


Fig.8. Chopper circuit

Input to the chopper modulator is low frequency and low amplitude signals, noise of the Opamp circuit is shown in fig 9 and in fig 10 shows log scale of the input referred noise of Opamp.

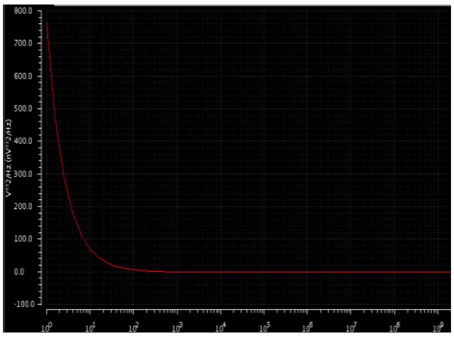


Fig.9. Noise of the Opamp

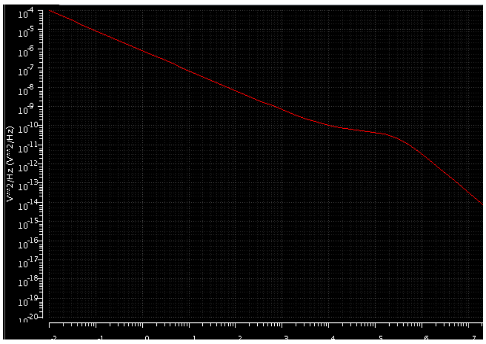


Fig.10. log scale noise in Opamp without chopping.

The inversion of signal by chopper takes place when $Ø_1$ is off and $Ø_2$ is on, MOSFET to be operated exact opposite of BJT transistor, when original signal is carried by noise. Chopper modulator circuit transposes the noise to the high frequency and Opamp will amplify the signal. Chopper demodulator demodulates Opamp output and the low pass filter shown in fig 11 removes the noise from the signal where we are left with the original signal as required.

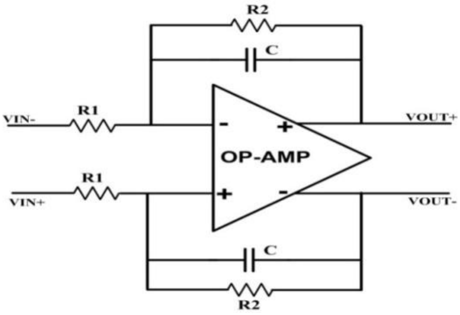


Fig.11. low pass filter

Fig 12 shows the output waveforms of the chopper amplifier where the input of the chopper and the chopper output in second row and final output in third row which is amplified by 100 times due to the gain present by operation of our Opamp.

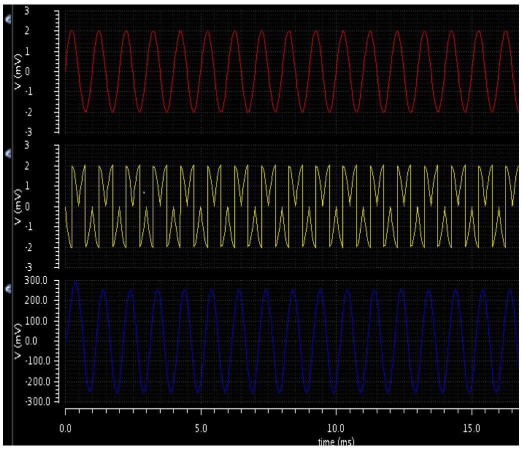


Fig.12. waveform of the circuit

In closed loop with capacitive coupled capacitance present in feedback shown in the below fig 13 circuit with gain in equation 3.

$$Gain = \frac{C_{in}}{C_{fb}} \quad (3)$$

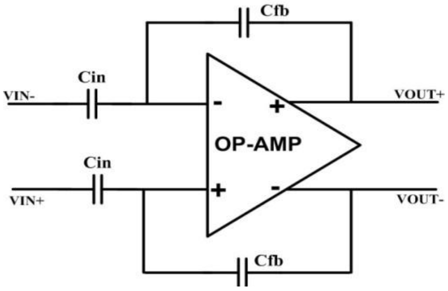
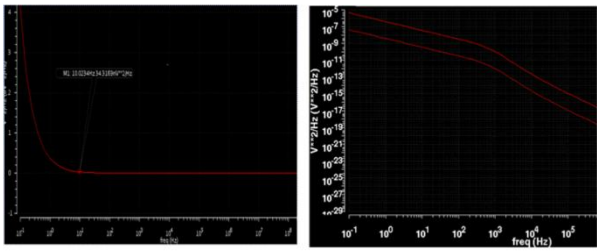


Fig.13. closed loop

Opamp Noise output of Chopper fully differential Opamp along with nv/√Hz with frequency along x axis is shown in fig 14.



(a) (b)

Fig.14. Noise output (a) refers to the noise total by chopping. (b) log scale of both output referred and input referred noise by G=100.

Finally the difference between the noise of Opamp and same Opamp operated with chopper modulator and demodulator is shown in fig 15 and table II shown the Implementation results which we have done so far. Above line indicates before chopping of Opamp referred noise and bottom line indicates after chopping referred noise.

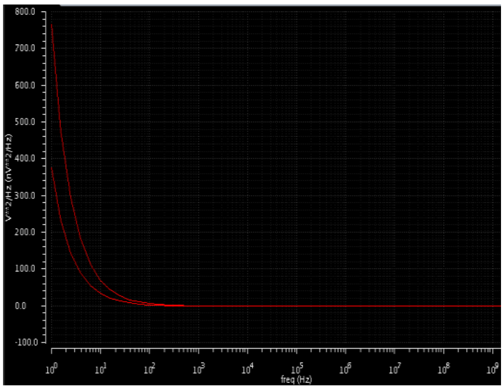


Fig.15. difference between Opamp and chopper referred noise

Table II. Implementation results

Technology	90nm
Voltage	1v
Input referred noise	38nv/√Hz
Phase margin	>60
Open Loop Op Amp Gain	57db
Slew rate	28V/µs

4. Future Work

Power is one of the trade-off for any design. Low power techniques for operational amplifier can also be considered and hence minimizing the power. Sub threshold region of operation to draw minimum current in order to minimize the power consumption will be considered rather than saturation region of operation.

5. Conclusions

A chopping modulation technique has been designed for signals of low frequency, amplitude signals. The two stage CMOS operational amplifier has been used to design both for amplifier and integrator circuit. The output is a continuous sinusoidal signal as the input signals which our Opamp has High CMRR greater than 90 db, and input referred noise of total circuit is 0.34nv/√Hz at 10Hz frequency. When signal is fed to a low pass filter, upon sufficient removal of the higher frequencies provided at the pre determined frequency provides the required original signal.

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