International Journal of Applied Engineering Research ISSN 0973-4562 Volume 10, Number 14 (2015) pp 34352-34356

Analysis of low power unsigned array multiplier architecture

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Abstract- In recent years, power dissipation is one of the biggest challenges in VLSI design. Multipliers are the main sources of power dissipation in DSP blocks. Power optimization has to be implemented on all components of the processor. In this paper, the design and power comparison of the low power unsigned Array Multipliers (AM) is proposed and analyzed using different adder units. The fundamental units to design multipliers are adders and shifters. The proposed AM gives 8 to 20 % of total area reduction and 9 to 14 % of power consumption. The AM architecture is carried out using .18µm technology. The experimental TSPICE result shows that the transistor count and the power consumption are significantly reduced in the proposed design.

Keyterms- *BRAUN multiplier, unsigned multiplication algorithm, full swing 16T full adder, 12T XOR.*

1. Introduction

Very Large Scale Integrated (VLSI) circuit technology is the rapid growing technology for a wide range of innovative devices and systems that have changed the world today. In the past, the major concerns of the VLSI design are to reduce area, improve performance, and reduce cost and reliability. Power was mostly one of the secondary important. Now a day the primary focus is to reduce power dissipation than the area and speed. The explosive growth in laptop and portable systems and in cellular networks has intensified the research efforts in low power electronics. High power systems often may lead to damage several circuits. Low power leads to reduction in power supply technology and to introduce low power batteries with good life time.

The multiplier circuit is a core component of most of the present day digital signal processors. Therefore, the demand for multiplier-performance improvement is increasing. Multipliers are a major source of power dissipation. Reducing the power dissipation of multipliers is key to satisfying the overall power budget of various digital circuits and systems.

In this paper, power reduction for unsigned multipliers was analyzed and power comparisons of BRAUN multipliers are obtained. The AND logic is replaced with the NOR logic for the power reduction. The power dissipation and the transistor count are reduced in the proposed half adder unit. The Sections is organized as follows: In section II describes unsigned multiplication algorithm. Section III describes with the conventional array multiplier architecture. In section IV the designs of different adders are discussed. Section V the proposed multiplier design is discussed. Section VI experimental results and conclusion are discussed, which validate the proposed method.

2. Unsigned multiplication algorithm

Utilizing AND gates and full adders, multiplication can be implemented on the processor in the same way as it is done by hand: multiply each digit of the multiplier by the multiplicand, thereby generating partial products and then sum up the respective partial products in order to generate the final result. Assume that X and Y are two n-bit unsigned numbers, where X is the multiplicand and Y is the multiplier. They can be expressed as follows:

$$X = \sum_{i=0}^{n-1} X_i 2^i \quad (1)$$

$$Y = \sum_{j=0}^{n-1} Y_j 2^j \quad (2)$$

$$P = \sum_{i=0}^{n-1} \sum_{j=0}^{n-1} X_i Y_j 2^{(i+j)} \quad (3)$$

The product of X and Y is P and it can be written in the following form:

Each of the partial product terms $P_n = X_i Y_j$ is called the summand. All the partial products then get added up to generate the final product [7].

3. Existing architecture

Array multipliers are high speed parallel multipliers. Unsigned array multipliers are also known as Braun multipliers or Carry Save Array Multipliers [7] [8].This multiplier is restricted to performing multiplication of two unsigned numbers. It consists of an array of AND gates and adders arranged in an iterative structure that does not require logic registers. This is also known as the non-additive multiplier since it does not add an additional operand to the result of the multiplication .Architecture of a nxn bit multiplier requires n(n-1) adders and n^2 AND gates.

Each of the $X_i Y_j$ product bits is generated in parallel with the AND gates. Each partial product can be added to the previous sum of partial products by using a row of adders. There is no horizontal propagation of carry in it. The brain multiplier performs well for unsigned operands that are less than 16 bits. The half adders used in the existing multiplier is the 28 transistor conventional CMOS adder. The design of conventional XOR gate of 22T and the conventional full adder of 28T, that are used in the existing array multiplier are given in figure 2 and figure 3 respectively.

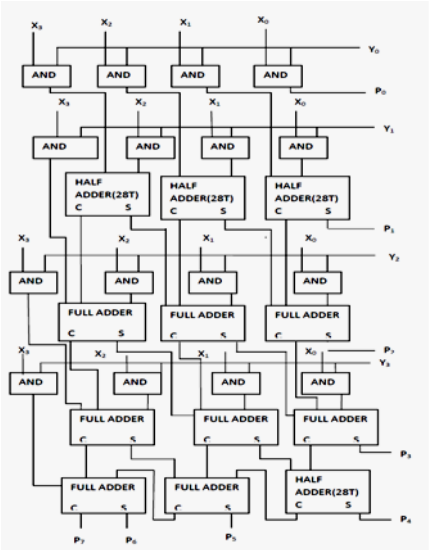

Fig 1 Conventional unsigned array multiplier

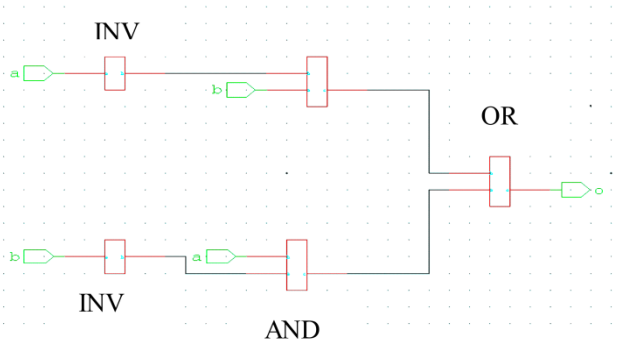

Fig 2 XOR gate (22T)

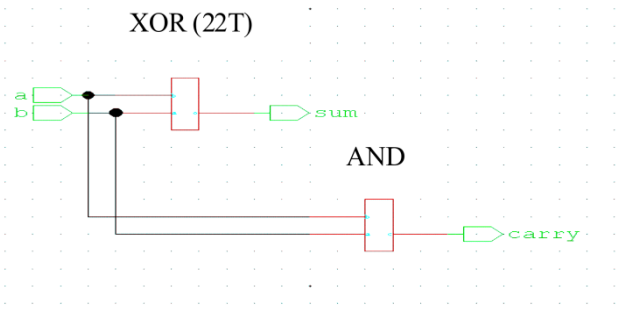

Fig 3 Conventional half adders

4. Design of Full Adders

Conventional CMOS full adder with 28 transistors is a robust, high power and area full adder, which has been designed, based on standard CMOS topology [9]. New-14T, Fig. 1 (c), is an improvement from 14T which has simultaneous XOR and XNOR signals. Feedback transistors provide rail-to-rail outputs in XOR-XNOR module. However, they prompt high delay [10].

The existing and proposed array multiplier are designed, The power analyzed for different full adders structure like CMOS normal full adder with 28 transistor, 16 transistor, 14 transistor and 10 transistor models are obtained.and comparison of power results are obtained by each full adder the optimized multiplier design is found out.

Four different full adders are used for analysis. The first one is the normal CMOS full adder [8] in figure 4 which is having 62 transistors with two half adder structures.

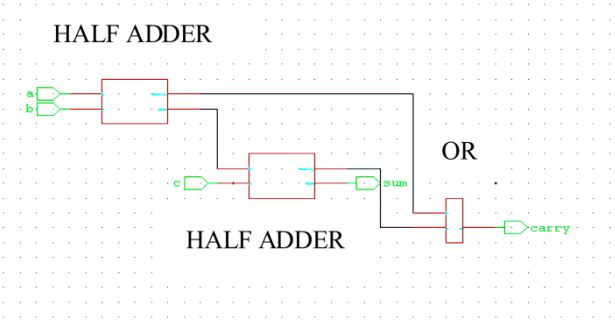

Fig 4 CMOS full adder (62 T)

The second full adder is the 16T full adder [4] which is having full swing and is having low power consumption than the transmission gate full adder as discussed in [2], [3] is shown in figure 5.total of 16 transistor were used to design the full adder structure .The power dissipation when compared to transmission gate full adder is 15 % less.

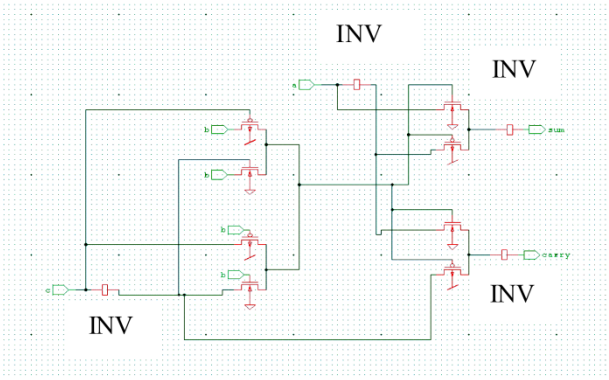

Fig 5 full swing 16T full adder

A 14T full adder [5] is discussed in the literature that is used for the analysis and it is better than the conventional adder design [7] and it is shown in the figure 6.

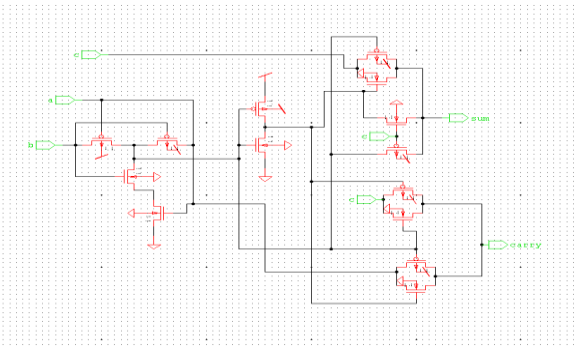

Fig 6 new 14T full adder

Static energy recovery full adder [6] is the fourth one which is having 10T and it is having low power than the conventional 10T full adder[7] is shown in the figure 7.

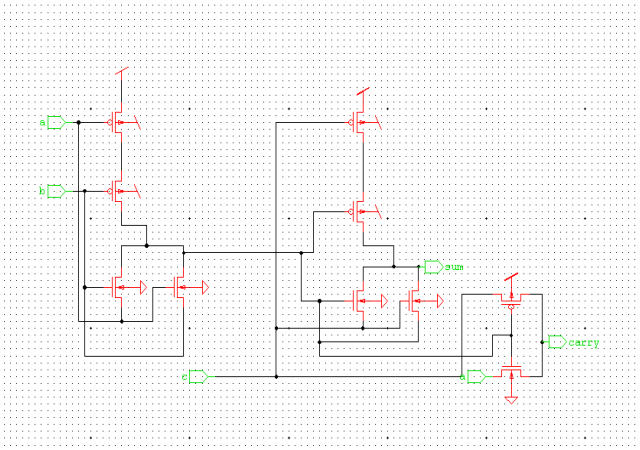

Fig 7 8 T full adder

5. Proposed Architecture

The process of array multiplication which follows the unsigned algorithm, the multiplication is done by AND operation of multiplicand and multiplier bits, the output of the AND operation is termed as partial product. The partial product is again added by the adder units to obtain the multiplication output. In the existing design the AND gate is replaced with an NOR logic by using the De- Morgan' s Law The design of AND gate in CMOS logic will have a transistor count of six where as to design an NOR gate in CMOS logic will have a count of four transistor. The input to the NOR gate is also inverted in order to obtain the accurate result.

A.B = (A'+B')' (4)

Thus, for a m* n multiplier, the proposed method introduces m + n extra inverters along with changing m * n AND gates to m * n NOR gates, effectively saving ((m * n) – (m + n)) inverters and 2 * ((m * n) – (m + n)) transistors For example a 5*5 multiplier 10 inverters are initially required, 25 AND gates are replaced with 25 NOR gates, thus in total when compared to conventional multiplier structure 80 transistors are saved. According to demorgans law it makes necessary to use inverted input these reduces the inverter in the proposed multiplier.

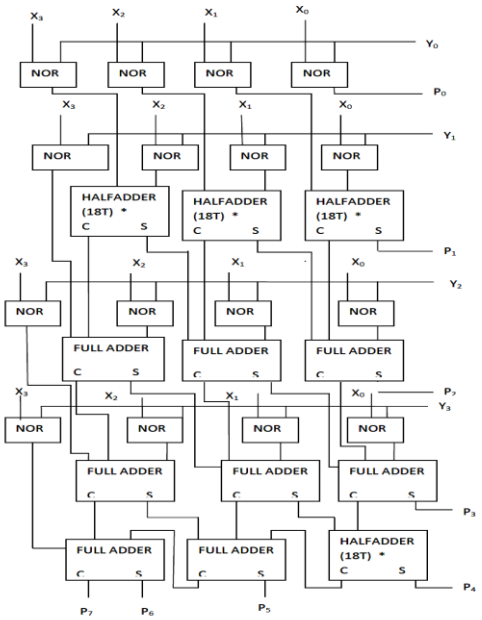

Fig 8 Proposed unsigned array multiplier

The number of transistor is reduced from the conventional multiplier architecture, thus the area required when compared to as mentioned in above architecture is reduced. The area constrain for the design of multiplier is achieved. Further the generated partial product is to be added with the combination of full adder and half adder structures only. The analysis part is done to obtain the low power by reducing the transistor count in the adder structure also. The half adders used for the proposed design are with 12 transistor XOR gate. The proposed multipliers uses the proposed 12 transistor half adder structure and with different full adder transistor count. The 22T XOR gate half adder is replaced with 12T XOR gate half adder. The 12T XOR gate is in figure 9.

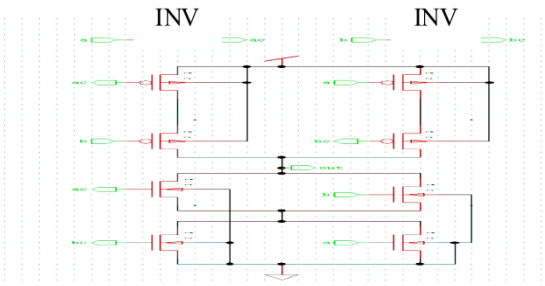

Fig .9 12T XOR

6. Results and Discussion

The designs are done with 120 µm technology file using TANNER S-EDIT 12.0 tool. The transistor count is calculated for the existing and proposed multipliers and the result are tabled in table 1. .The 29% power improvement is

achieved by using only XOR gate based transistor model as shown in figure 10. The power comparisons of half adder unit with respect to their transistor count is about 58 % improvement for a single bit operation as shown in figure 12 only by using XOR logic The figure 13 shows the full adder style of design with different transistor count . A table 1 showing transistor count is also obtained for existing and proposed array multipliers.

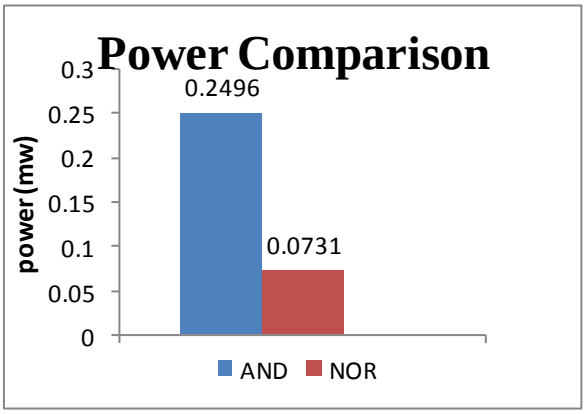

Fig 10 Power comparison of AND (6T) gate and NOR (4T) gate

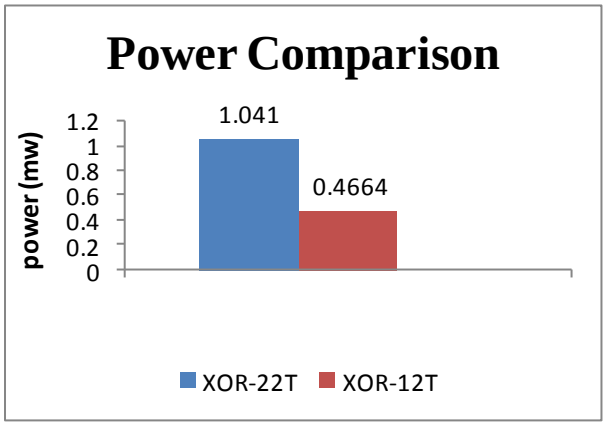

Fig 11 Power comparisons of 22T XOR and 12T XOR gates

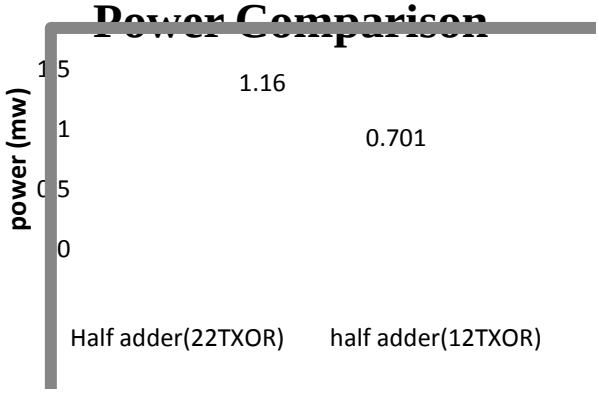

Figure 12 Power comparisons of 22T XOR half adder and 12T XOR half adder

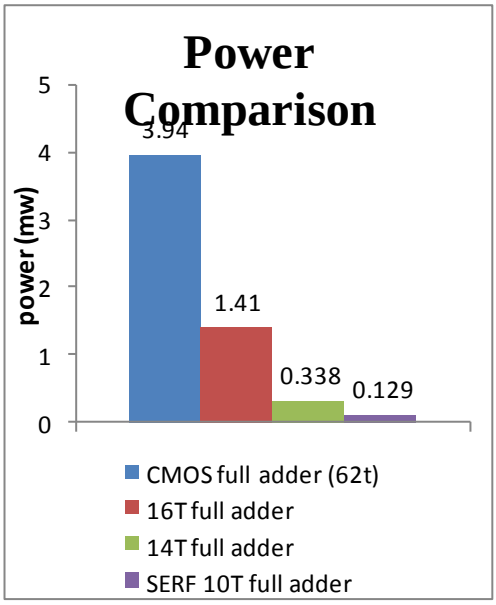

Fig 13 Power comparisons of different full adders

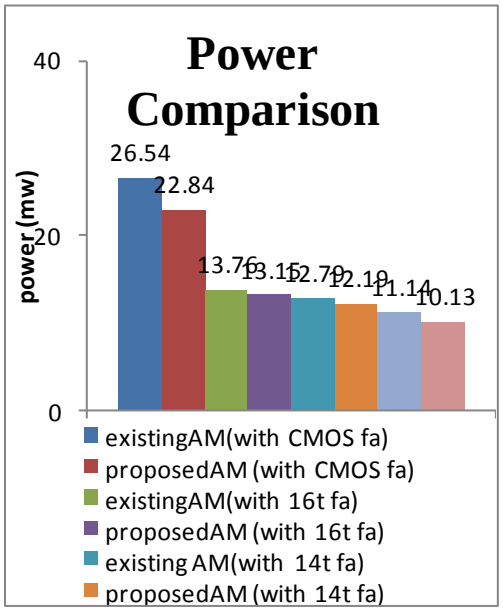

Fig 14 Power comparisons of different array multipliers (AM).

Table 1 Transistor count of different array multiplier

Array multiplier(AM)	No.of transistor	Improvement
Existing AM (with CMOS fa)	704	8 %
Proposed AM(with CMOS fa)	648	
Existing AM (with 16T fa)	336	16 %
Proposed AM(with 16T fa)	280	
Existing AM (with 14T fa)	320	17.5 %
Proposed AM(with 14T fa)	264	
Existing AM (with SERF fa)	288	19.4%
Proposed AM(with SERF fa)	232	

7. Conclusion

In this paper, a new approach for the design of parallel unsigned array multipliers has been suggested. AND gates in the existing designs have been replaced with NOR gates. the power results are analysed and compared with different adder units using Tspice. It is therefore found that the proposed array multipliers have transistor count and power range less than that of existing multipliers. Proposed Multipliers with the CMOS full adder have 8% reduction in transistor count and about 13.9% power reuction than the existing. Multipliers with 16T full adder have 16% and 4.4% reduction in transistor and power consumption than the existing.Transistor count reduction and power reduction are 17.5% and 4.6% respectively for the proposed multiplier with 14T full adder than the existing multiplier with 14T full adder.Finally the proposed multipliers with SERF have 19.4% reduction in transistor count and 9% power reduction than the existing multiplier.Therefore it is found that the proposed multiplier with SERF have better results than the other multipliers.

8. References

[1] Ronak Bajaj, Saransh Chhabra ,Sreehari Veeramachaneni and M.B.Srinivas, "A Novel Low Power Array Multiplier Architecture," ISCIT, pp. 119-123, 2009.

[2] Nan Zhuang and Haomin Wu, "A new design of the CMOS full adder," IEEE Journal of Solid State Circuits, Vol.27, No.5, pp.840-844, May 1992.

[3] Ahmed M.Shams, Magdy A.Bayoumi and Tarek K.Darwish, "Performance Analysis of Low-Power 1-Bit CMOS Full Adder Cells,"IEEE Transactions on VLSI Systems,vol.10,No.1,pp.20-29,February 2002.

[4] M.H.Ghadiry, M.Miryahyaei and M.Nadisnejani, "A New Full Swing Full Adder Based on a New Logic Approach," World Applied Sciences Journal 11 (7), pp. 808-812, 2010.

[5] E. Abu-Shama and M. Bayoumi, " A New Cell for Low Power Adders,". IEEE Int. Symp. on Circuits and Systems, pp.49-52. [doi:10.1109/iscas. 1996. 541898], 1996.

[6] E. John , L.K. John and R. Shalem, "A novel low power energy recovery full adder cell, " Proc. of GLSVLSI, pp.380-383,1999.

[7] K.Roy and S.C. Prasad, "*Low Power CMOS VLSI Circuit Design*," Wiley , 2000.

[8] Neil Weste and Kamran Eshranghian, *Principles of CMOS VLSI Design*, Addison Wiley, 2000.

[9] Navi, K., M. Maeen, V. Foroutan, S. Timarchi and O. Kavei, 2009. A novel low power full-adder cell for low voltage, Integration the VLSI J., 42(4): 457-467

[10] Shams, A.M. and M.A. Bayoumi, 2000. A novel high performance CMOS 1-bit full adder cell, IEEE Trans. Circuits and Systems-II: Analog digital Signal Process, 47(5): 478-481.