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Radiation Induced SEU Impact on DG-SOI FINFET based Class E RF Power Amplifier

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Abstract
This paper puts forward two class E power amplifier implementations in 30 nm DG-SOI FINFET technology. The first configuration using a single transistor has a PAE of 92% that provides a power gain of 37.017 dB. The second configuration is a cascode class E amplifier that has a PAE of 85.16% by giving a power gain of 20.86 dB. The cascode amplifier circuit configuration has been used in order to reduce the voltage stress and thus increases the reliability of RF communication systems. Both the circuits operate at 10 GHz frequency range, by providing an output power of 26 dBm. m. For the single device and cascode configuration, 0.5 mA and 2 mA is the threshold current amplitude above which SEU impact is observed.

Index Terms— Cascode Configuration, DG-SOI FINFET, Multi-Gate transistor, Power Added Efficiency.

1. INTRODUCTION

Scaling of device dimensions has become an indispensible as well as an inevitable part of the IC manufacturing and fabrication in recent years. As the shrinking continues, speed and operating frequency of CMOS circuits increases and hence time has come up for integrating every section of a communication system onto a single chip. Needless to say, the scaling of CMOS technologies beyond sub-micrometer range has helped a lot in integrating different sections. However, CMOS technology scaling has also seen many fundamental roadblocks owing to the increase in leakage currents and short channel effects considerably. As a result, many 3-D engineered devices came into picture as a consequence of these issues. Many circuits that use MOSFET or BJT as the active device are now being replaced with 3-D engineered devices such as double (DG), triple (TG) or quadruple MOSFETs or FINFETs. The short channel effects as well as the problems related to the leakage current and the supply voltage are found to be much lower than the conventional CMOS technologies [1]. A large number of recent works suggest that double gate (DG) SOI based devices are promising substitutes to MOSFET structures [2].
The double gate structure has an advantage that it is simpler for 3D structural optimization and relatively easier to fabricate [3]. Such a structure can be built using a modified (two gates separated and independently accessed) FINFET device architecture. One of the major limitations of this device is that it requires additional routing for the second (back) gate connection. However, the performance gained by introducing a double gate has certainly outweighed its limitations [4]. Many digital circuits have already started witnessing this shift. Since Ion/Ioff ratio of this device is much larger than that of their CMOS counterparts, most of the currently using digital logic families have started using FINFET device architectures [5, 6, 7, 8].
RF domain has also seen a tremendous change in recent years. Recent investigations and papers have mainly focused on the RF performance of FINFET based devices [9, 10]. The DG devices can show better RF behavior due to the volume inversion effects at low gate bias and better scalability. Many RF circuits are now being replaced with multi-gate transistors thus improving the performance and efficiency of the wireless communication systems.
One of the most important problems that is being faced by RF wireless systems in space applications is the radiation effects caused from particles such as neutrons and pions. Power amplifiers, being an important component in such systems, are prone to soft errors such as Single Event Upset (SEUs) effects. The output voltage and hence the output power may get distorted for a very short period of time, degrading the circuits' performance considerably. A lot of research work has been done in this field finding out how much threshold current level such systems can handle so that their performance may not get affected [16,17].
In this paper, we have focused on developing a moderately linear, highly efficient class E power amplifier in 30 nm DG-SOI based FINFET technology. Circuit simulations of both single-stage and cascode implementations are carried out in order to show the compromise between efficiency and reliability. Analysis results and performance figures for the implemented power amplifiers are done in Cadence Virtuoso Analog Design Environment (ADE). SEU effect on the implemented Class E Power Amplifiers has also been studied and performance analysis has been done.
The organization of the paper is as follows. Section I gives an introduction to DG-SOI FINFETs. Section II tells about BSIM-CMG model and its transfer characteristics. Section III explains the single stage class E amplifier configuration using this model and its performance analysis. Section IV gives the design of cascode class E amplifier and its performance analysis. SEU effects on the implemented Class E Power Amplifiers are discussed in Section V, followed by conclusion and references.

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2. DG-SOI FINFET DEVICES

BSIM-Common Multi-Gate (CMG) 107.0.0 compact model is used for simulation and analysis of both the circuits. The model has captured all the required multiple-gate transistor behaviors [11]. Here we have used double gate FINFET based Verilog-A model for simulation and analyses. SOI based mode has been selected by setting the parameter BULKMOD to 0. An un-doped or lightly doped body eliminates threshold voltage (Vt) variations due to random dopant fluctuations and thus enhances carrier transport resulting in higher on current. Fig.1 shows the transfer characteristic plotted logarithmically. Ion/Ioff ratio has been found to be about $10^{8.1}$ which is much higher than that of conventional CMOS structures. Some of the default parameters that were already given in the model are listed in Table 1.

TABLE I DEFAULT PARAMETERS AND CORRESPONDING VALUES

Symbol	Parameter	Values
L	Gate length	30 nm
CDSC	Coupling Capacitance between S/D and Channel.	7 mF/m^2
TFIN	Fin thickness	15 nm
NFIN	Number of fins	1
EOT	SiO2 equivalent gate dielectric thickness	1 nm
PHIG	Gate work-function	4.61 eV
TOXP	Physical oxide thickness	1.2 nm
VSAT	Saturation velocity for the saturation region	85000 m/s
NSD	S/D doping concentration	2e26 m^{-3}
CJS	Unit area source-side junction capacitance at zero bias	0.0005 F/ m^2
CJD	Unit area drain-side junction capacitance at zero bias	0.0005 F/ m^2
BVS	Source diode breakdown voltage	10.0 V
BVD	Drain diode breakdown voltage	10.0 V
TNOM	Nominal temperature	27 C
PCLM	Channel length modulation parameter	0.013

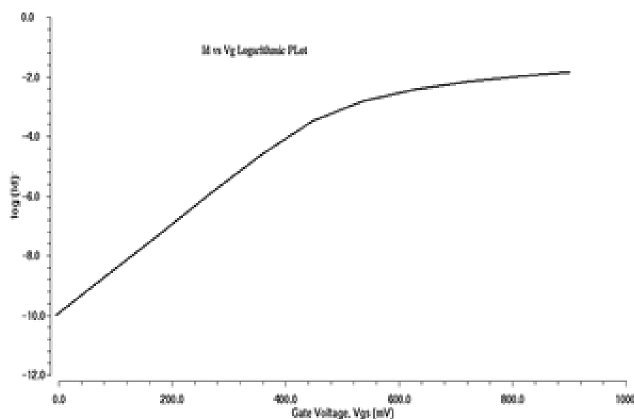

Fig 1. Drain current versus gate voltage logarithmic curve. I_{on}/I_{off} ratio is about $10^{8.1}$ which is much higher than that of CMOS device.

3. SINGLE DEVICE CONFIGURATION

3.1. Analysis and design

As mentioned, the paper puts forward two class E RF power amplifier configurations in 30 nm technology. The driver stage and the impedance matching stage have been neglected in order to carefully study the performance figures of DG-SOI FINFETs when employed in designing power amplifier configurations. Analysis of single stage as well as cascode type implementations have been carried out in order to study the trade-off between efficiency and reliability. The circuit diagram showing class E amplifier using a single device is given in Fig. 2.

The width and the number of fingers were increased to 10um and 500 respectively in order to attain the required RF characteristics. Front and back gates were shorted and an input pulse waveform with voltage of 0.9 V and a frequency of 10 GHz was applied to the gates. The device thus switches between off state and the saturation, providing a very high voltage at the drain node.

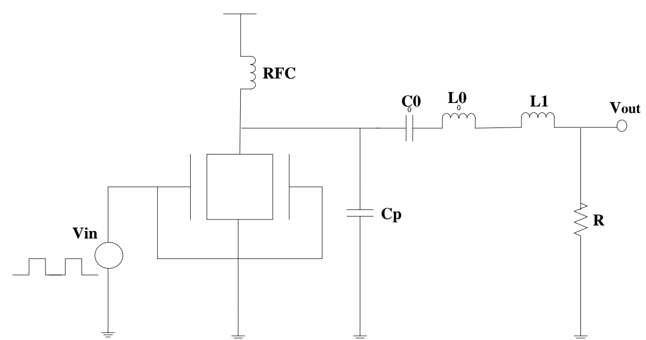

Fig 2. Circuit Diagram showing single device class E amplifier configuration with back gate shorted to front gate.

The component values required for the circuit were taken according to the design equations. A dc feed inductor of 500 pH is employed to limit ac ripples. The voltage at the drain node is given by the equation

$$V_{ds} = 3.562V_{dd} \quad (1)$$

Since 30 nm gate length is used, nominal drain voltage of 0.9 V is used as V_{dd} [15]. Drain voltage obtained to be around 3.17 V which is close to theoretical predictions. The graph representing the output voltage waveforms is given in Fig. 3. A tank circuit of high Q-factor 30 was used to get a moderately linear output across the 1 ohm resistive load.

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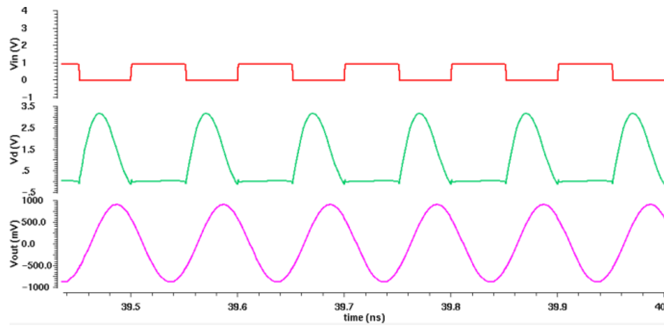

Fig. 3. Output voltage waveforms of single device class E amplifier circuit. Voltage at the drain node is equal to 3.17 V.

3.2. Performance Analysis

Periodic Steady State Analysis (PSS) is performed to obtain the required performance characteristics. An output power of 26.55 dBm is obtained at 10 GHz as shown in Fig. 4. The power gain at this frequency has been found to be 37.0172 dB which is being shown in Fig. 5.

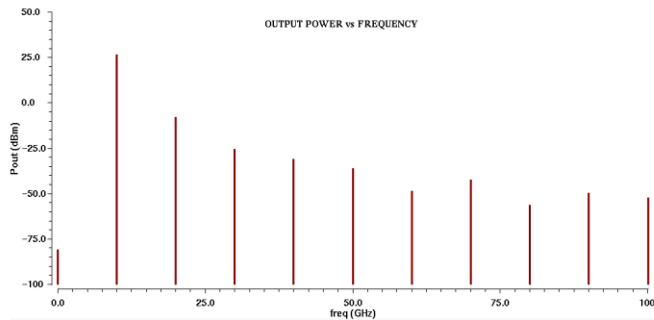

Fig. 4. Output power spectrum for single device configuration. At 10 GHz, maximum output power of 26.55 dBm is obtained.

High value of the input pulse waveform is varied from 0 to 0.9 V in order to obtain the efficiency curve. The graph showing the power added efficiency (PAE) versus input voltage in Fig. 6 implies that almost 92.9 % PAE can be obtained by using this model. As the input voltage crosses the threshold value, PAE rises abruptly. Maximum value is obtained when the device is in the saturation region.

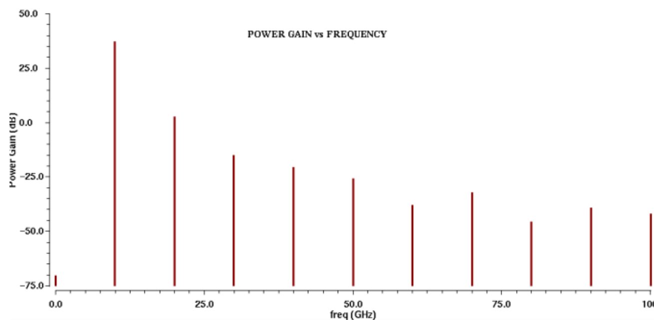

Fig. 5. Power Gain spectrum showing maximum power gain at 10GHz.

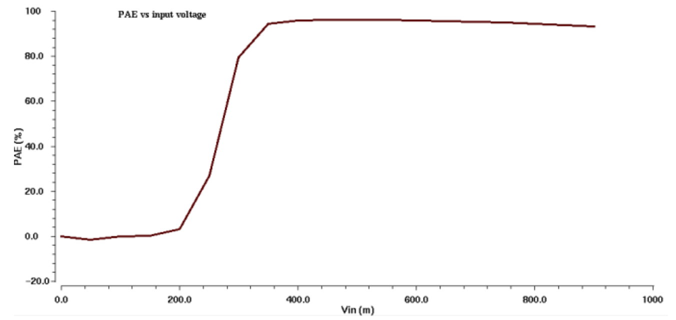

Fig. 6. Power Added Efficiency plotted against input voltage showing 92.9% PAE at 900mV.

4. CASCODE CONFIGURATION

4.1 Design and Simulation

As compared to single transistor circuit, cascode transistor implementation has many advantages. The voltage stress developed across the transistor in the previous circuit has been shared by another DG-SOI FINFET connected in cascode. Thus this structure is found to be much more reliable and can be used where continuous availability of RF power is required. However the reliability of the amplifier is compromised by the efficiency since the output power is reduced as compared to the previous configuration.The circuit diagram of the cascode implementation is shown in Fig. 7.

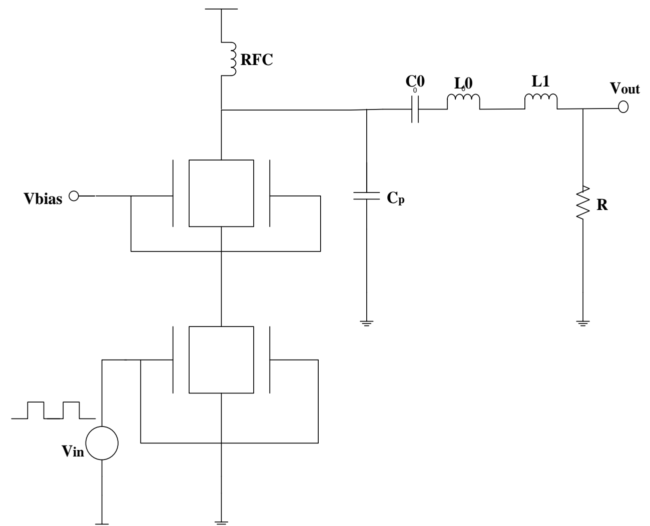

Fig. 7. Circuit Diagram showing cascode implementation of class E amplifier using DG-SOI FINFET.

The component values taken were similar to that of the previous circuit. The width of the cascode transistor was kept at 10 um for getting the maximum possible output voltage. The gate of the cascode transistor has been biased at 0.9 V in order to keep the transistor in saturation.

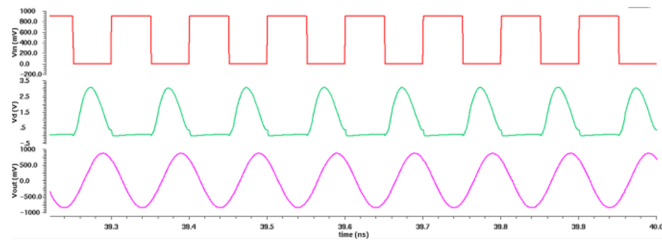

Fig. 8. Voltage waveforms of cascode implementation. A maximum value of 3.056 V is obtained at the drain node.

The width and the number of fingers of the bottom transistor were kept at 10 um and 500 respectively. As similar to the previous case, since 30 nm technology is employed, a 0.9V, 10 GHz square waveform of 50% duty cycle is applied to the front gate of the bottom transistor. The output voltage waveforms are given in Fig. 8. Maximum drain voltage of 3.0584 V has been obtained.

4.2. Performance Analysis

Similar to single device implementation, performance analysis has been carried out in order to show the efficiency and power gain variation with respect to frequency. An output power of 26.35 dBm is obtained at 10 GHz as shown in Fig. 9. Power Gain versus frequency plot has been given in Fig. 10, which shows that 20.86 dB can be obtained at 10 GHz frequency. Power Added Efficiency curve which is plotted against input voltage, in Fig. 11 shows that a PAE of 85.16% can be obtained using this model.

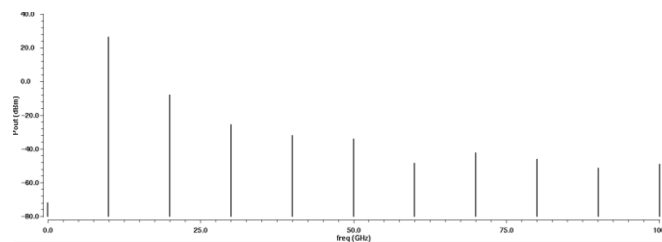

Fig. 9. Output Power Spectrum showing 26.3551 dBm at 10 GHz.

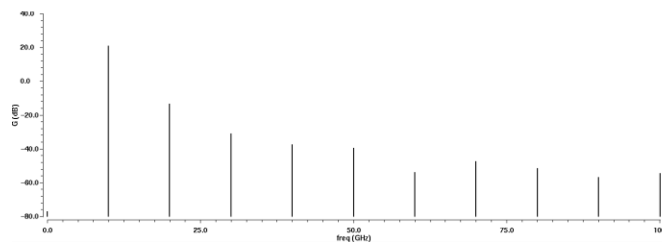

Fig. 10. Power Gain spectrum showing a gain of 20.8601 dB at 10GHz.

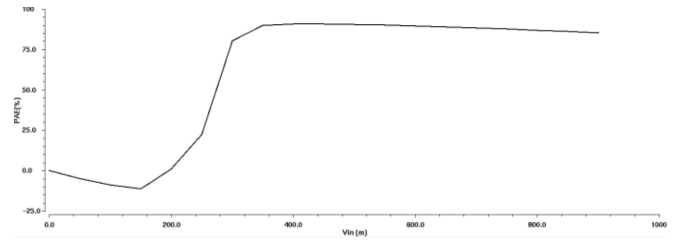

Fig. 11. Power Added Efficiency Plot versus input voltage. A PAE of 85.16% has been obtained at 900mV input voltage.

TABLE II PERFORMANCE COMPARISONS OF DIFFERENT CLASS E PAS

Ref.	Tech.	Architecture	Freq(f) (GHz)	PAE (%)	P_{out} (dBm)
[12]	180 nm CMOS	Single device Configuration	2.4	73	23
[13]	130 nm CMOS	Two stage cascaded	2.5	65	23
[14]	65 nm CMOS	Cascode configuration	2	60	30
This work (Sec.III)	30nm DG-FINFET	Single device Configuration	10	92	26
This work (Sec.IV)	30nm DG-FINFET	Cascode Configuration	10	85	26

5. SEU EFFECTS IN POWER AMPLIFIERS

Single event Upset (SEU) effects are one of the most predominant types of soft errors that occur in RF wireless communication systems when used in space applications, especially in satellite networks. Such effects can degrade the performance of the system in such a way that the output may get distorted or the functioning may get affected. Power amplifiers, being an important part of such systems are also prone to such effects. When a power amplifier is subjected to an SEU, the output voltage distorts and hence the output power reduces considerably resulting in a larger power loss.

SEU effect in the implemented class E power amplifiers has been investigated by striking a double exponential current pulse to the drain nodes of both the amplifiers. The amplitude of the pulse has been varied from 1A to 0.5 mA in order to study the variation in the output voltage. It has been found that the distortion reduces with decrease in the amplitude of the current pulse in both the circuits. For the single device structure, it has been found that the threshold current amplitude is 0.5 mA below which the circuit output voltage is unaffected as shown in Fig. 12 and Fig. 13.

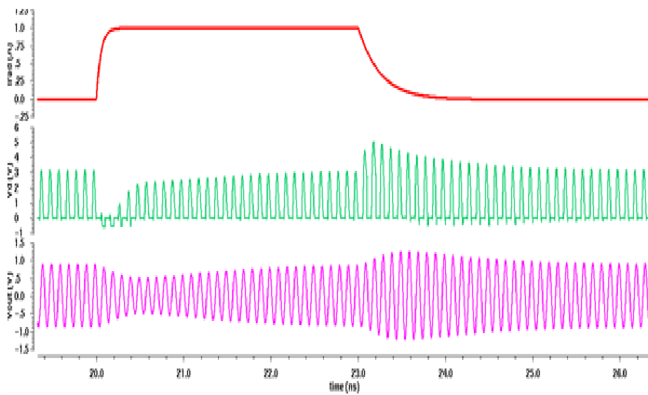

Fig. 12. SEU effect on single device structure with amplitude 1A.

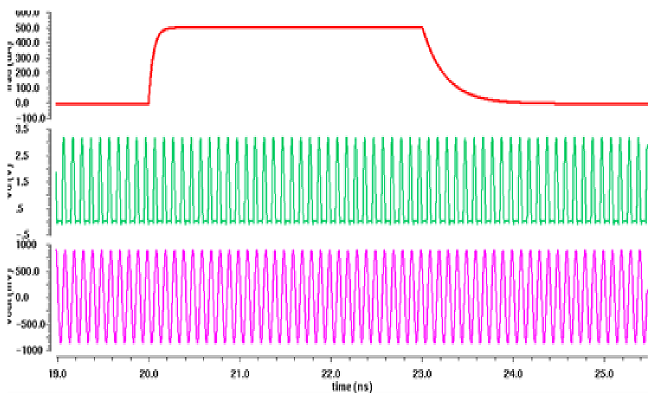

Fig. 13. SEU effect on single device structure with amplitude 0.5mA.

For the cascode structure, the current threshold amplitude has been obtained to be around 2 mA below which there is no reduction in circuit performance (Fig. 14 and Fig. 15). Thus it can be inferred that cascode amplifier is much more stable and hence reliable as compared to the single device structure.

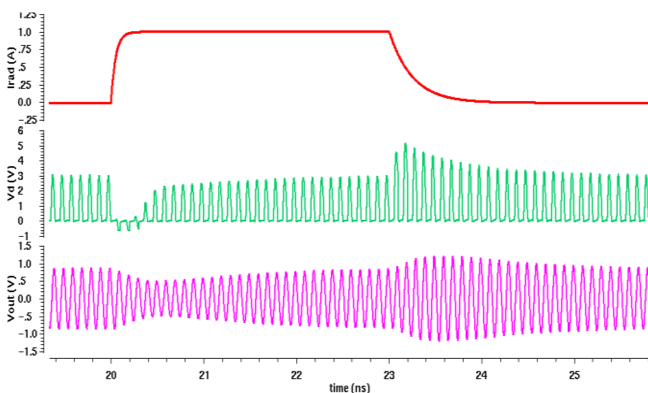

Fig. 14. SEU effect on cascode structure with amplitude of 1A.

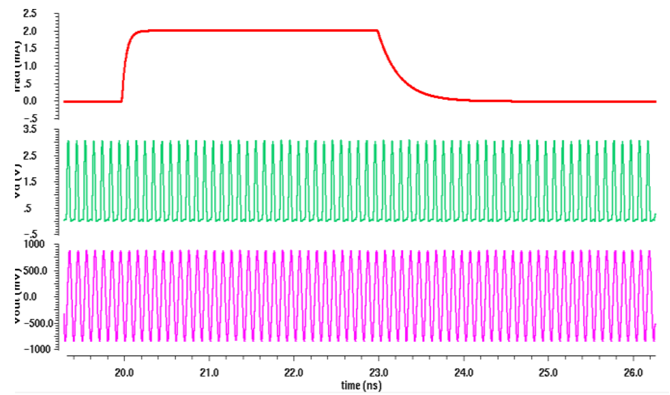

Fig. 15. SEU effect on cascode structure with amplitude of 2mA.

6. DISCUSSION AND CONCLUSION

The performance comparisons of different Class E Power Amplifiers in different technologies are given in Table 2. PAE of 85.16% for cascode configuration suggests that power gain of 20.86 dB can be obtained at the output at a frequency of 10 GHz. Maximum power gain of 37.018 dB has been obtained for the single device configuration by providing a PAE of 92.9%.Thus single device configuration can be used in applications where maximum efficiency is required and in areas where more reliability, reduced efficiency is needed, cascode configuration can be employed.

In conclusion, the work has proved that 3 D engineered devices can be an excellent substitute for the CMOS technology in terms of its efficiency, performance, and ultra-compact designs. The design can also be used as a motivation for upcoming power amplifier FINFET based configurations.

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