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An FPGA implementation of Phase-locked loop (PLL) with self-healing VCO

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ABSTRACT:
The objective of this paper is to develop phase-locked loop (PLL) with a self-healing prescaler and a self-healing voltage-controlled oscillator (VCO) which can overcome the problem occurred due to variability and leakage current in nanoscale CMOS technology. The design has been implemented by using VERILOG HDL and also implemented on Xilinx SPARTAN 3E FPGA. The project involves two phases such as simulation and synthesis of the Verilog codes using Modelsim SE and Xilinx Synthesis Technology (XST) of Xilinx ISE design suite.

Keywords: Voltage controlled oscillator (vco), Phase locked loop (PLL), FPGA, Verilog HDL.

1. INTRODUCTION

On one side the improvement of the microelectronics processes especially for complementary metal oxide semiconductor (CMOS) technology which allowed a drastic reduction of the power consumption and an increase of the maximum operating frequency at which active devices can operate. These two combined factors allowed the integration on a single silicon die of both digital signal processing at base-band and radio frequency signal conditioning, a filtering and amplification at frequencies up to several gigahertz. Hence the possibility of integrating all the functionalities of a full wireless transceiver on a single chip allowed a consistent cost scaling and a reduction of the silicon die area compared to compound semiconductors technologies. Therefore, the newest wireless applications (like high-quality video streaming) are extremely demanding in terms of bandwidth. Thus to face this problem, a allocation of new frequency bands has been necessary and the frequency spectrum in the multi gigahertz range has been allocated. Into this category of new frequency bands, a 7 GHz wide spectrum around 60 GHz (IEEE 802.15 WPAN standard) is one of the newest and more promising one. The recent scaling of CMOS processes down to 90-65-45 nm allowed the operation of standard Si-CMOS processes at frequencies above 60 GHz. In the overall transceiver system architecture, a frequency synthesis from a fixed reference frequency is an essential building block. Due to its better noise performances compared to other solutions and channel selection availability through the loop division ratio modulation, a phase lock loop (PLL) frequency synthesis is the natural choice for such an application. Considerably, the design of a self healing pre-scaler and a self-healing VCO for a PLL frequency synthesizer is taken into consideration. The purpose of the presented design is to overcome the drawback of leakage current in PLL.

2. PHASE-LOCKED LOOP (PLL)

A phase-locked loop (PLL) is a feedback control system that generates a signal that has a fixed relation to the phase of a reference signal. The design responds to both the frequency and the phase of the input signals by automatically raising or lowering the frequency of a controlled oscillator until it is matched to the reference in both frequency and phase.

3. PLL COMPONENTS AND BASIC OPERATION

A PLL consists of five main blocks:-

- ☐ Phase Detector or Phase Frequency Detector (PD or PFD)
- ☐ Low Pass Filter (LPF)/Loop Filter
- ☐ Voltage Controlled Oscillator (VCO)
- ☐ Divide by N Counter

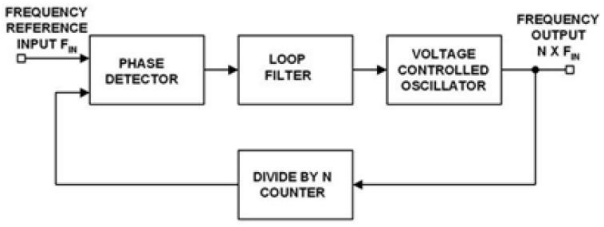

Fig. 1: Block diagram of PLL

3. 1. Phase frequency detector:

The phase difference between the reference and feedback signal is measured by the phase frequency detector (PFD). If there is a phase difference between the two signals it generates up or down synchronized signals to the charge pump/ low pass filter. While if error signal is an up signal then obtained difference is given to low pass filter which increases the control voltage Vctrl. Thus if the error signal from the PFD is a down signal then the LPF decreases Vctrl. Output of

LPF is the control voltage Vctrl which is the input to the VCO.

3. 2. Loop filter:

The loop filter is the heart of a PLL. A PFD/CP/LPF combination contains a pole at the origin and VCO also contains a pole at the origin. While the loop gain has two poles at the origin the instability arises. Thus, in order to stabilize the system we must modify the phase characteristics by adding a resistor in series with the capacitor.

3. 3. Voltage controlled oscillator:

An oscillator is an independent design system that generates a periodic output without any input. Voltage-Controlled Oscillator (VCO) is an electronic oscillator designed such that its oscillation frequency is controlled by a voltage input. In this the frequency of oscillation is controlled by the applied DC voltage, by modulating signals may also be fed into the VCO to cause frequency modulation or phase modulation. Hence the frequency of oscillation must be tunable for the phase of a PLL to be adjustable. A self-healing VCO have been realized by four stages a bottom-level detector and a current compensator.

3. 4. Self-healing Prescaler:

To realize a wide-range PLL the divider following a VCO should operate between the highest and lowest frequencies. Thus, when a PLL works at a higher frequency where the static circuits cannot operate so the dynamic circuits are needed. For this type of PLL a true-single-phase-clocking (TSPC) divider is widely. A TSPC prescaler must work over a wide frequency range to cover the process and temperature variations. So undesired leakage currents may limit the TSPC pre-scaler frequency. For clock generation mostly reference frequencies are limited by the maximum frequency decided by a crystal frequency reference. Thus the main purpose of a divider's is to scale down the frequency from the output of the voltage controlled oscillator so that the system can operate at a higher frequency than the reference signal. Thus, the VCO has to be designed such that the output of VCO is equal to N times the reference frequency. Such that, the output of the VCO is passed through a divide by N-counter and feedback to the input signal. For this particular application the D flip flop based divider has been chosen because of practical reasons.

4. RESULTS

4. 1. Simulation Results:

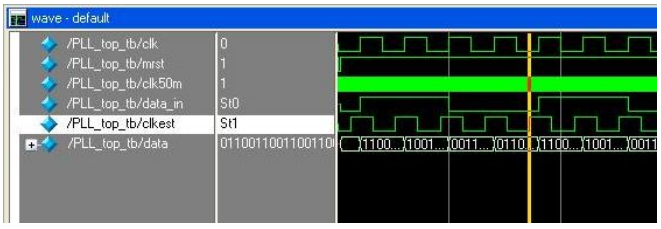

Fig.2: Simulation result of PLL

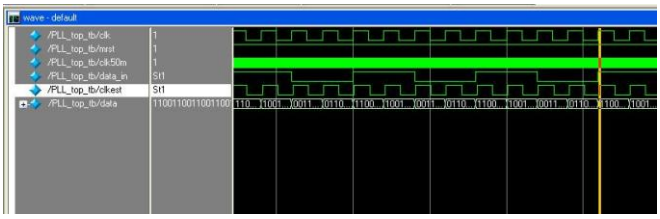

Fig.3: Simulation result of PLL with synchronized clocks

4.2. Synthesis Results

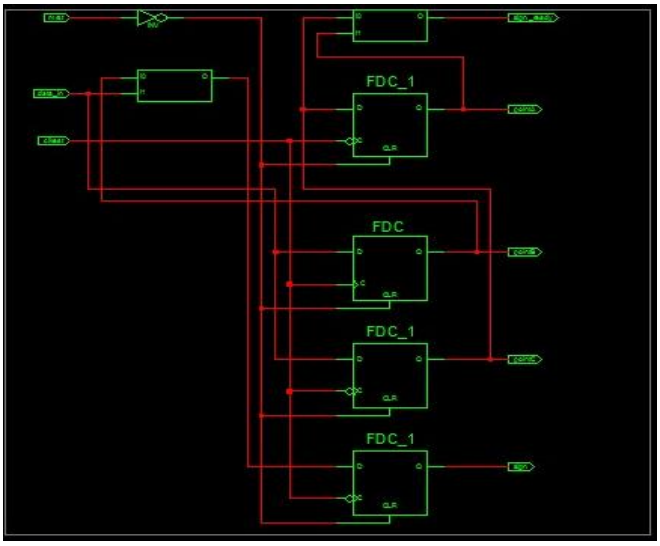

Fig.4: RTL schematic of PLL

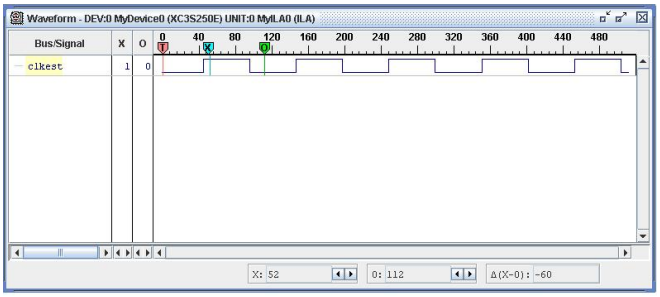

Fig.5: Chip-scope result of PLL

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		52
Vccint 1.20V:	15	19
Vccaux 2.50V:	12	30
Vcco25 2.50V:	2	4
Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco25	0	0
Signals:	0	0
Quiescent Vccint 1.20V:	15	19
Quiescent Vccaux 2.50V:	12	30
Quiescent Vcco25 2.50V:	2	4

Fig.6: Power and Current results of PLL

5. CONCLUSION

In this work we have designed a PLL with self-healing prescaler and a self-healing VCO using a Verilog HDL. The design module was simulated by Modelsim simulator and synthesized by using a XILINX XST tool. And also implemented the designed module on a XILINX SPARTAN 3E FPGA device and observed the hardware results by using CHIPSCOPE software. By this we have seen the results of PLL which have been more improved when compared to the existing method.

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